CONTROL DATA

60455690

CDC®
FA211-A/B FIXED MODULE DRIVE CONTROLLER
FV662-A CHANNEL ACCESS OPTION
FV670-A/B 844 DRIVE OPTION
FV671-A/B FOUR FMD OPTION

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS

VOLUME 1 OF 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Preliminary edition. This edition may change without notice.
02	Manual updated. Previous edition obsolete.
A (03-30-79)	Manual released. Includes Engineering Change Orders 39837 and 39914. This revision obsoletes all previous editions.
B (08-21-79)	Manual revised; includes Field Change Order 40179. Pages revised by Field Change Order: 5-52, 5-101 through 5-106, 7-6, 7-15, and 8-25. Miscellaneous changes made to: x, xiv, xvi, xvii, xviii, 1-1, 2-2, 2-4, 3-7, 3-8, 3-9, 3-10, 3-11, 3-12, 3-13, 4-15, 4-32, 4-42, 5-17, 5-23, 5-25, 5-27, 5-29, 5-33, 5-35.0, 5-37, 5-44, 5-47.1, 5-47.2, 5-49, 5-51, 5-68, 5-80, 5-88, 5-139, 5-157/5-158, 5-194, 5-199, 7-2 through 7-15, 7-18, 7-19, 8-118, 8-127, and 8-128. Pages added: 3-14, 6-3, 6-4, 6-5, and 6-6.
C (05-01-80)	Engineering Change Order 40935. No change to manual.
D (05-01-80)	Manual revised; includes Field Change Order 40624. Pages 17D4, 17D8, 20E1/E2, 20E13/E14, 20F1/F2, 20H5, 21B1/B2, 21B3/B4, 21B5/B6, 21B7/B8, 21G5/G6, 22D11/D12, 22E1/E2, 22E3/E4, 22E5/E6, 22E7/E8, 22E9/E10, 22E11/E12, 26D2, 26D3, and 27C13 are revised.
E (06-09-80)	Manual revised; includes Engineering Change Order 41289, publications change only. Pages 18F3/F4.
F (12-12-80)	Manual revised; includes Field Change Order 41224. Grid locators 17E8, 17E9, 17E10, 17E11, 17F1/F2, 17F3/F4, 20H5, 21B1/B2, 21B3/B4, 21B5/B6, 21B7/B8, 26D2, and 26D3 are revised. Grid locators 17B6 and 17B7 are deleted.
G (04-28-81)	Manual revised; includes FA211-B and Engineering Change Orders 41792 and 41114. This edition obsoletes all previous editions.
H (10-23-81)	Manual revised; includes Engineering Change Order 42928. Frames 17B4, 17F8, 19H1/H2, card placement in frames 13/14 of every row on fiches 20 through 26.2, 22E7/E8, 23C9/C10, 26D3/D4, 26.2D1/D2, 27E1, 27E2, and 27E8 are revised.
J (07-30-82)	Manual revised; includes Field Change Order 43256. Frames 17B1, 17B3, 17B4, 17B5, 25D3/D4, 25E3/E4, 26C1/C2, 27E1, 27E8, 27E12, 28F10, 28G5, 28I4, 28I6, 28J9, and 28E13 are revised.
K (07-30-82)	Manual revised; includes Engineering Change Order 43505. Frames 17F8, 17F9, 27C3, 27C11, 27D7, 27E4, 28F10, 28G5, 28I4, 28I6, 28J9, and 28E13 are revised.
L (08-26-82)	Manual revised; includes Engineering Change Order 43862. Frames 17B4 and 17B6 are revised.
M (03-11-83)	Manual revised; includes Engineering Change Order 44047. Frames 17B3, 17B4, 17B5, 19H2, card placement in frame 14 of every row on fiches 20 through 26.1, 21B3/B4, 21C1/C2, 21D1/D2, 21E1/E2, 21G5/G6, 22C1/C2, 22C3/C4, 22C5/C6, 22C7/C8, 22D1/D2, 23C3/C4, 23D7/D8, 23F9/F10, 25D9/D10, 25F3/F4, 26B5/B6, 26B7/B8, 26C1/C2, 26.1D1/D2 through 26.1D9/D10, 26.1E1/E2 through 26.1E9/E10, 26.1F1/F2 through 26.1F11/F12, 26.1G1/G2, 27C3, 27D7, 28.2B3/B4, 28.2D2 through 28.2D9, 29B2 through 29B9, 29C5/C6, 29C11/C12, 29E2 through 29F13, 29G3/G4, and 29G5/G6 are revised.
N (04-01-83)	Manual revised; includes Engineering Change Order 44481. Frames 17B4, 27F2, 28E13, 28F10, 28G5, 28I4, 28I6, and 28J9 are revised.

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REVISION LETTERS I, O, Q, S, X AND Z ARE NOT USED.

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or use Comment Sheet in the back of this manual.

REVISION RECORD

REVISION	DESCRIPTION
P (05-05-83)	Manual revised; includes Engineering Change Order 44130. Grid locators 17B4, 17B5, 19H1/H2, 20-26.2B13/B14, 20-26.2C13/C14, 20-26.2D13/D14, 20-26.2E13/E14, 20-26.2F13/F14, and 22B1/B2 through 22B7/B8 are revised.
R (12-21-84)	Manual revised; includes Engineering Change Order 45185. This edition obsoletes all previous editions.
S (12-21-84)	No change to manual.
T (12-21-84)	Manual revised; includes Field Change Order 44747. Pages 5-1 and 5-211 through 5-227 are revised.
U (12-21-84)	Manual revised; includes Engineering Change Order 45987. Manual converted to hardcopy format.
V (06-03-85)	Manual revised; includes Engineering Change Order 47019. Front Cover and page 3-5 in volume 1; front cover, 9/10, 8-1/8-2, 8-24, 8-31, 8-36, 8-52, 8-53, and 8-62 in volume 2 are revised. Divider (FV670-A/B) and 8-170.1 are added.
W (10-03-86)	Manual revised; includes Engineering Change Order 48108. Pages 5-29 and 5-76.1 through 5-79 in volume 1 are revised. Page 5-76.2 in volume 1 is added.

Publication No.
60455690

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FA211-A	A01	-	Released
	A02	EC039837	
	A03	FC040179	
	A04	FC040624	
	A05	FC041224	
	A06	EC044130	
FA211-B	B01	-	Released
	B02	FC044047	
	B03	EC044130	
FV662-A	A01	-	Released
	A02	FC040624	
	A03	FC041224	
	A04	EC044130	
FV670-A	A01	-	Released
	A02	FC043256	
FV670-B	B01	-	Released
	B02	FC043256	
FV671-A	A01	-	Released
FV671-B	B01	-	Released

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Front Cover	-
Title Page	-
2	W
3/4	R
5/6	W
7/8	R
9	R
10	R
11	R
1-1	R
1-2	R
1-3	R
2-1	R
2-2	R
2-3	R
2-4	R
2-5	R
2-6	R
2-7	R
3-1	R
3-2	R
3-3	R
3-4	R
3-5	V
3-6	R
3-7	R
3-8	R
4-1	R
4-2	R
4-3	R
4-4	R
4-5	R
4-6	R
4-7	R
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4-9	R
4-10	R
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4-15	R
4-16	R
4-17	R
4-18	R
4-19	R
4-20	R
4-21	R
4-22	R
4-23	R
4-24	R
4-25	R
4-26	R
4-27	R
4-28	R
4-29	R
4-30	R
4-31	R
5-0.1	R
5-0.2	R
Divider	-
5-2	R
5-3	R
5-4	R
5-5	R
5-6	R
5-7	R
5-8	R
5-9	R
5-10	R
5-11	R
5-12	R
5-13	R
5-14	R
5-15	R
Divider	-
5-16	R
5-17	R
5-18	R
5-19	R
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5-21	R
5-22	R
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5-26	R
5-27	R
5-28	R
5-28.1	R
Divider	-
5-29	W
5-30	R
5-31	R
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5-33	R
5-34	R
5-35	R
5-36	R
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5-37	R
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5-40	R
5-41	R
5-42	R
5-43	R
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5-46	R
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5-66	R
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5-71	R
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Divider	-
5-76.1	W
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5-77	W
5-78	W
5-79	W
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5-109	R
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5-135	R
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5-218	T
5-219	T
5-220	T
5-221	T
5-222	T
5-223	T
5-224	T
5-225	T
5-226	T
5-227	T
5-228	R
5-229	R
5-230	R
5-231	R
5-232	R
Comment Sheet	W
Back Cover	-

This manual provides hardware maintenance information for the following CDC® equipments.

Equipment	Nomenclature
FA211-A/B	Fixed Module Drive (FMD) Controller
FV662-A	Channel Access Option
FV670-A/B	844 Drive Option
FV671-A/B	Four FMD Option

The FA211-A/B controller transfers data between a peripheral processor (PP) and up to four dual-spindle, fixed-module drive (FMD) units. The FA211-A has one PP channel interface while the FA211-B does not include a PP channel interface as standard equipment.

The FV662-A option provides a data and control interface for one PP channel. Up to three FV662-A options can be added to an FA211-A controller and up to four can be added to an FA211-B controller.

The FV670-A/B and FV671-A/B options allow data transfer between the controller and either fixed- or removable-media drives. The FV670-A/B provides an interface for eight BR308/BR312 (844) removable-disk drives while the FA671-A/B provides an interface for additional BZ703 (885) fixed-module drive units. The FV670-A and FV671-A options are field installable; the FV670-B and FV671-B are factory installed.

Other manuals necessary to maintain and understand these equipments are listed below.

Control Data Publication	Publication Number
7155 Disk Storage Subsystem Hardware Reference Manual	60455860
CYBER 70 Models 72/73/74, 6000 Computer Systems Input/Output Specifications	60352500
CYBER 170 Models 171 through 175 Computer Systems Input/Output Specifications	19983600
ECL 10,000 Series Microcircuits Manual	60417700
BR30x Disk Storage Unit Maintenance Manual	70618400
BR30x Disk Storage Unit Diagrams and Wire List	70618500
BR30x Disk Storage Unit Parts List	70618600
BZ703 CYBER Disk Storage Hardware Reference	83322880
Hardware Maintenance Manual Volume 1	83322860
Hardware Maintenance Manual Volume 2	83322870
Microcircuit Handbook, Volume 1	15006100

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The Fixed Module Drive (FMD) Controller is the controlling element in a disk storage subsystem consisting of the controller and 885 CDC CYBER Serial Fixed Module Drives. In addition, 844 Disk Storage Units can be added to the subsystem. The subsystem provides random access mass storage for CDC 6000 series; CDC CYBER 70 Models 71, 72, 73, 74; and CDC CYBER 170 Models 171 through 175 and 720 through 760 computers. A peripheral processor (PP) provides the computer/subsystem connection.

NOTE

The controller and its associated options must be the only peripheral subsystem on its PP channel.

Other equipments that can be added to the subsystem are:

- Channel Access Option
- 844 Drive Option
- Four FMD Option

These equipments and the controller are described in this manual. The disk drives are described in manuals listed in the preface.

FIXED MODULE DRIVE (FMD) CONTROLLER

The controller consists of a cabinet, power and cooling components, and a chassis containing 25 (model A) or 23 (model B) logic cards.

CHANNEL ACCESS OPTION

This option provides a data and control interface for another PP data channel. It consists of one ECL 60-pak, an interface cable assembly, and a channel access enable switch. Three channel access options can be added to a model A controller. Four channel access options can be added to a model B controller.

844 DRIVE OPTION

This option provides an interface for eight 844 disk drives. One 844 Drive Option can be added to a controller. The option consists of eight ECL 60-paks, 16 cable assemblies, power sequence hardware, and eight drive access enable switches.

FOUR FMD OPTION

This option provides an interface for four CDC CYBER Serial Fixed Module Drives (eight spindles). The option consists of four ECL 60-paks, eight cable assemblies, and eight drive (spindle) access enable switches.

NOTE

Each FMD cabinet contains two spindles.

CONFIGURATION

In a minimum configuration, the controller attaches to one PP data channel and to two FMD spindles. The controller can attach to eight spindles without the addition of any options. With the addition of the options, the subsystem can attach to up to four PP data channels, 16 FMD spindles, and eight 844 drives.

FUNCTIONAL DESCRIPTION

The controller is a programmable device that may be divided into the following sections.

PP Interface

This exchanges data and control signals with the PP I/O channel.

Processor

This controls the PP interface and the drive interfaces. The processor executes a modified CDC CYBER PP instruction repertoire. Eight large scale integration microprocessor chips constitute the central part of the processor. A 256-word, 60-bit-per-word control read-only memory (ROM) contains PP instruction microcode. The processor has a 4-K 16-bit random-access memory (RAM) that contains the MA721 controlware. The processor also includes a RAM used as a buffer. A 2-K, 16-bit RAM buffer is part of the model A controller and a 4-K 16-bit RAM buffer is part of the model B controller. A 1-K 16-bit ROM contains firmware that has some rudimentary diagnostics and controls autoloading and function execution.

Processor Channels

Seventeen 16-bit bidirectional channels are available to the processor to send and receive control and status signals to/from the other parts of the controller. One of these is dedicated to communication with the PP interface.

Error Correction

The controller contains hardware to correct most data errors. Correction is done using a 48-bit or 32-bit polynomial provided by the processor.

Drive Interface

This provides the connection with the drives in the subsystem.

Data Path Control

This controls the assembly/disassembly of data, checks for sector marks, counts data bytes, and generally controls transfers between the controller and the drives.

PHYSICAL DESCRIPTION

Figure 1-1 illustrates and identifies major controller components.

The controller uses ECL 10,000 series integrated circuits encapsulated in dual-in-line ceramic type 16-pin or 48-pin chips. These chips are mounted on printed-circuit modules. A module contains up to 60 chips. These modules are called 60-paks and plug into the logic chassis. In addition, the controller uses several microprocessor chip types that are of the large scale integration variety.

The logic chassis consists of printed-circuit boards mounted in a metal frame. Each board has several rows of pins that pass through the board and protrude from front to back. Modules are inserted by sliding them over metal guides in the frame until they plug into pins protruding from the front of the board. Backpanel pins are interconnected using the wire-wrap method.

Doors and removable panels on the cabinet provide access to site maintainable components. The controller occupies part of two 27-location rows. The model A controller consists of twenty-five 60-paks and the model B controller consists of twenty-three 60-paks. The expansion options reside in the same two rows.

Most power-related components are located at the base of the cabinet. Power supplies operate from 120/208-V, 400-Hz, 3-phase power. The blower and convenience outlet operate from 50-Hz or 60-Hz power.

NOTE

Because the convenience outlet is protected by a 7-A circuit breaker, it is suitable for use with low power equipment only.

DIMENSIONS

Height	1675 mm (66 in)
Depth	745 mm (29 in)
Width	635 mm (25 in)
Weight	175 kg (350 lb)

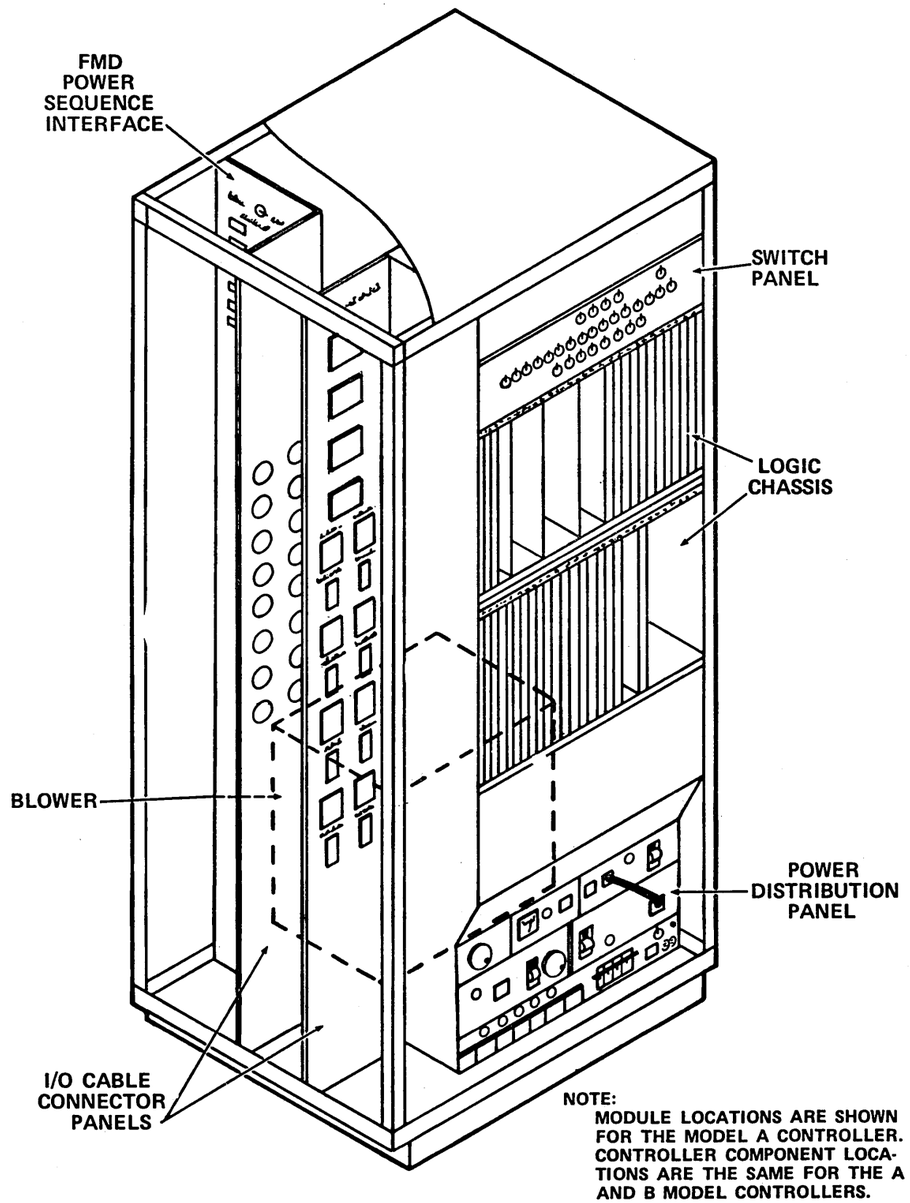

FMD POWER SEQUENCE INTERFACE
SWITCH PANEL
LOGIC CHASSIS
BLOWER
POWER DISTRIBUTION PANEL
I/O CABLE CONNECTOR PANELS
NOTE:
MODULE LOCATIONS ARE SHOWN FOR THE MODEL A CONTROLLER. CONTROLLER COMPONENT LOCATIONS ARE THE SAME FOR THE A AND B MODEL CONTROLLERS.

Figure 1-1. Controller Component Locations

ENVIRONMENTAL REQUIREMENTS

Cooling method	Forced air	
Heat dissipation	3311 Btu/h (965 W)	
Temperature		
Operating		15 °C to 32.2 °C (59 °F to 90 °F)
Nonoperating		-40 °C to +70 °C (-40 °F to +158 °F)
Recommended		24 °C (75 °F)
Maximum operating gradient		5 °C/h (9 °F/h)
Maximum nonoperating gradient		20 °C/h (36 °F/h)
Humidity		
Operating	35% to 60% relative humidity	
Nonoperating	0% to 100% relative humidity	

POWER REQUIREMENTS

•	120/208 V	400 Hz	3-phase, 3.1 A/phase
•	120 V	50/60 Hz	1-phase, 9 A
		or	
	220, 230, 240, 250 V	50/60 Hz	1-phase, 5 A

OPERATION

This section describes operator switches/indicators for each subsystem equipment and provides procedures for typical operator tasks.

SWITCHES/INDICATORS

Figure 2-1 shows the locations of controller operator switches/indicators. Table 2-1 describes switch/indicator functions.

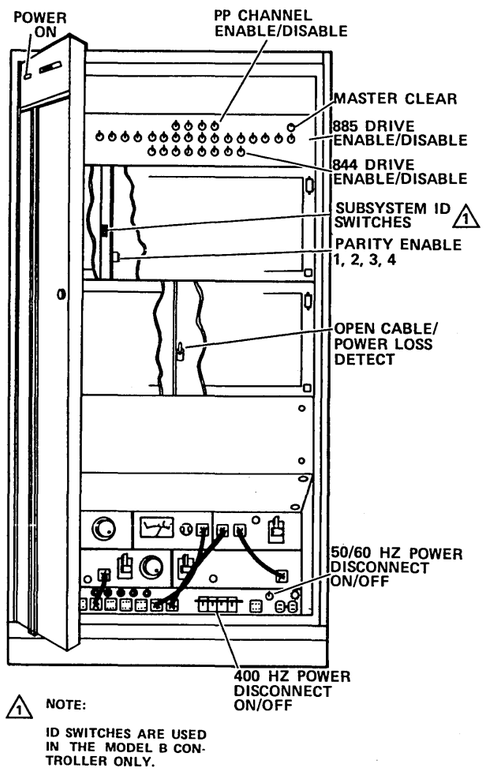


Figure 2-1. Controller Switch/Indicator Locations

Table 2-1. Controller Switches/Indicators

Name	Type	Function
POWER ON	Indicator	Lights when power is applied to controller.
PP CHANNEL ENABLE/ DISABLE	Four toggle switches	Enables/disables communication between controller and PP channel attached to access associated with switch.
MASTER CLEAR	Pushbutton switch	Clears controller logic and connected access and forces processor memory address to $20\ 000_8$.
885 DRIVE ENABLE/ DISABLE	Sixteen toggle switches	Enables/disables communication between controller and FMD attached to connector associated with switch.
844 DRIVE ENABLE/ DISABLE	Eight toggle switches	Enables/disables communication between controller and 844 drive attached to connectors associated with switch.
50/60 HZ POWER DISCONNECT ON/OFF	Toggle switch	ON: Applies power to blower. OFF: Removes power from blower.
400 HZ POWER DISCONNECT ON/OFF	Toggle switch	ON: Applies power to controller logic. OFF: Removes power from controller logic.
1, 2, 3, 4 ON/OFF	Four switches (at chassis location A08)	ON: Enables parity for the respective PP access. 1 = access A, 2 = access B, 3 = access C, 4 = access D. OFF: Disables parity.
PROTECTED/ DISABLE	Toggle switch (at chassis location B13)	Enables open cable/power loss detect circuit. Disables this circuit. NOTE: Put in disable (down) position when running voltage margins.
SUBSYSTEM IDENTIFICATION †	Eight toggle switches (at chassis location A07)	Switches should be set to a number to uniquely identify the controller within the system.

† The subsystem identification switches are used only in the model B controller.

OPERATING PROCEDURES

Subsystem Power Control

Each controller and drive contains power sequence circuitry that regulates initial subsystem electrical load. This circuitry allows power feeding the entire subsystem to be controlled from a single power control box. At installation time, a customer engineer performs the cable routing and switch setting required for power sequencing. Thereafter, the operator normally controls subsystem power from the power control box.

Once power has been applied, the subsystem is ready for operation when the READY indicator lights on the last drive to receive power. The operator can turn a single drive off or on with the drive's START switch. Removing logic power from a controller that is providing power sequencing to a group of drives also removes power from each drive having the LOCAL/REMOTE switch set to REMOTE. Section 3 further describes the power sequence circuit.

Controller Initialization

A controller must be autoloaded with controlware before the controller can execute the complete function set described in section 3 of the 7155 Disk Storage Subsystem Reference Manual listed in the preface. The following functions reside permanently in the ROM portion of processor memory to enable autoloading.

- 0012_8 - General status
- $01NN_8$ - Autoload from disk (NN = disk drive number)
- $03NN_8$ - Disk deadstart
- 0414_8 - Autoload from PP

Although all controller autoload procedures rely on one or more of these functions, the exact procedure used depends upon site operating procedures, the operating system in use, computer system configuration, and whether or not the computer system is running. Refer to the appropriate operating system installation handbook for controller autoload procedures recommended by Control Data.

PROGRAMMING

The processor in the controller executes microcode from a 256-word, 60-bit ROM to provide a modified PP instruction set for the controlware programmer.

The processor uses one's complement arithmetic and 16-bit words. The processor right-justifies and zero-fills operands that use less than all 16 bits, and uses two's complement arithmetic for address calculations.

NOTE

Memory addresses are given in octal.

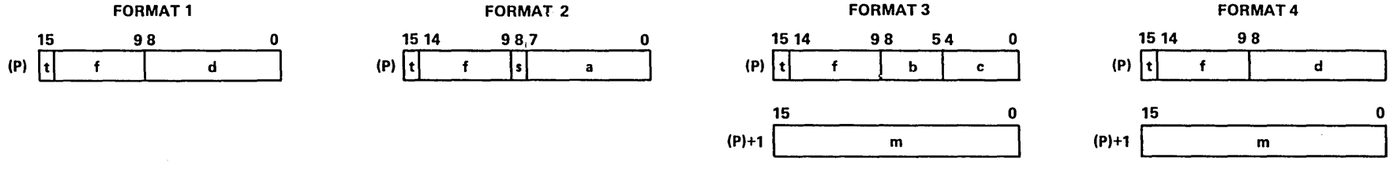
The processor memory, which consists of 16-bit words, includes the following three parts:

- A 4-K RAM (addresses 0 to 7777) contains the controlware.
- A 2-K RAM (addresses 10000 to 13777) in the model A controller or a 4-K RAM (addresses 10000 to 17777) in the model B controller acts as a data buffer.
- A 1-K ROM (addresses 20000 to 21777) contains a code for autoloading, executing functions, and performing rudimentary diagnostics.

The following processor instructions are listed according to operation code. Related instructions are grouped when a description applies to more than one instruction. Figure 2-2 lists all instructions and shows format and timing information. Table 2-2 shows how assembler mnemonics and parameters determine execution address formation.

NOTE

Parentheses ( ) are used to enclose required parameters. One set must be included in each instruction.



Symbol	( )	A	a	b	c	d	f	m	p	s	t
Bit(s)	–	–	0-7 of (P)	5-8 of (P)	0-4 of (P)	0-8 of (P)	9-14 of (P)	0-15 of (P)+1	–	8 of (P)	15 of (P)
Function	indicates contents of register or location	16-bit accumulator register	relative address magnitude, shift count (0-255)	channel bit designator	channel designator	immediate operand, address designator, channel designator	operation code	immediate operand, address designator	16-bit program address register	sign bit; 0 = +, 1 = -	program sync bit. Any mnemonic followed by S (for example LDDS) sets t.

FORMAT	MNEMONIC	OPERATION CODE	INSTRUCTION	CYCLES
1	HLT	00	Processor halt	Hang
4	LJM	01	Long jump to m + (d)	5 or 6 ①
4	RJM	02	R/W return jump to m + (d) + 1	9 or 10 ①
2	UJN	03	Unconditional jump ± a	3(+) or 4(–)
2	ZJN	04	Zero jump ± a	4 if condition satisfied, 3 if not
2	NJN	05	Nonzero jump ± a	
2	PJN	06	Plus jump ± a	
2	MJN	07	Minus jump ± a	
2	SHN	10	Shift ± a (+ is left-circular, – is right-off)	3 plus a
1	LMN	11	Logical difference d	2
1	LPN	12	Logical product d	2
1	SCN	13	Selective clear (A) with d	2
1	LDN	14	Load d	2
1	LCN	15	Load complement d	2
1	ADN	16	Add d	3
1	SBN	17	Subtract d	3
4	LDC	20	Load m	3
4	ADC	21	Add m	4
4	LPC	22	Logical product m	3
4	LMC	23	Logical difference m	3
1	PSN	24	Pass	2
4	RJR	25	ROM return jump to m + (d)	8 or 9 ①
1	POP	26	Pop stack to RJR caller	5
1	LPD	27	Logical product (d)	4
1	LDD	30	Load (d)	4
1	ADD	31	Add (d)	5
1	SBD	32	Subtract (d)	5
1	LMD	33	Logical difference (d)	4
1	STD	34	Store (d)	3
1	RAD	35	Replace add (d)	5
1	ADD	36	Replace add one (d)	5
1	SOD	37	Replace subtract one (d)	5

FORMAT	MNEMONIC	OPERATION CODE	INSTRUCTION	CYCLES
1	LDI	40	Load ((d))	5
1	ADI	41	Add ((d))	6
1	SBI	42	Subtract ((d))	6
1	LMI	43	Logical difference ((d))	5
1	STI	44	Store ((d))	5
1	RAI	45	Replace add ((d))	6
1	AOI	46	Replace add one ((d))	6
1	SOI	47	Replace subtract one ((d))	6
4	LDM	50	Load (m + (d))	5 or 6 ①
4	ADM	51	Add (m + (d))	6 or 7 ①
4	SBM	52	Subtract (m + (d))	6 or 7 ①
4	LMM	53	Logical difference (m + (d))	5 or 6 ①
4	STM	54	Store (m + (d))	5 or 6 ①
4	RAM	55	Replace add (m + (d))	6 or 7 ①
4	AOM	56	Replace add one (m + (d))	6 or 7 ①
4	SOM	57	Replace subtract one (m + (d))	6 or 7 ①
4	IFJ	60	Jump to m if input channel d full	5
4	IEJ	61	Jump to m if input channel d empty	5
4	OFJ	62	Jump to m if output channel d full	4
4	OEJ	63	Jump to m if output channel d empty	4
4	AJM	64	Jump to m if channel d active	4
4	IJM	65	Jump to m if channel d inactive	4
–	–	66	Unused	–
–	–	67	Unused	–
1	IAN	70	Input to A from channel d	4 plus full wait time ②
4	IAM	71	Input (A) words to m from channel d	7 plus 3·(A) plus full wait times
1	OAN	72	Output from A on channel d	4 plus empty wait time
4	OAM	73	Output (A) words from m on channel d	3 plus 3·(A) plus empty wait time
–	–	74	Unused	–
1	OFN	75	Output flag pulse on channel d	2
3	JSM	76	Jump to m if channel c, bit b is set	5
3	JNM	77	Jump to m if channel c, bit b is not set	5

① Test occurs during first half of first cycle

NOTES:

① When d is 8, m + (d) = m and the smaller number of cycles applies.

② When bit 0 of (P) is set, processor echoes output channel.

Figure 2-2. Microprocessor Instruction Set

Table 2-2. Address Modes

Address Mode	Assembler Mnemonic	Assembler Parameter	Execution Address
Relative	XXN	+a	(p)+a
Relative	XXN	-a	(p)-a
Direct	XXD	d	d
Direct	XXC	M	M
Direct	XXM	MO	M
Indirect	XXI	d	(d)
Indexed	XXM	M d where d ≠ 0	m+(d)

HALT

00 HLT Processor halt

Stops instruction execution. Execution resumes at address 20 000_8 when a power-on, pushbutton, or PP channel master clear occurs or when the controller decodes an autoload (0414_8 or $01NN_8$) function.

UNCONDITIONAL JUMPS

01 LJM m d Long jump to m+(d)

03 UJN (+)a Unconditional jump ± a

Transfers control to execution address.

RETURN JUMP (RAM)

02 RJM m d Return jump to m+(d)+1 of RAM

Transfers (p)+2 to execution address and transfers control to execution address plus one. Execution address minus one must contain first word of long jump instruction (x01xxx). Return occurs when program execution reaches execution address minus one. Execution address must be less than 20 000_8.

CONDITION JUMPS ON (A)

04 ZJN(±)a Zero jump ± a

05 NJN(±)a Nonzero jump ± a

06 PJN (±)a Plus jump ± a

07 MJN (±)a Minus jump ± a

Transfers control to execution address if (A) satisfies specified condition. Otherwise, resumes execution at (p)+1.

Jump	Satisfying Condition
Zero	(A) = 000000
Nonzero	(A) ≠ 000000
Plus	Bit 15 of A is 0
Minus	Bit 15 of A is 1

SHIFT

10 SHN(±)a Shift ± a

Shifts (A) left circular (+) or right end-off (-) a bit position.

LOGICAL DIFFERENCE

11 LMN d Logical difference d

23 LMC m Logical difference m

33 LMD d Logical difference (d)

43 LMI d Logical difference ((d))

53 LMM md Logical difference (m+(d))

Complements A bits that correspond to 1 bits in d, m, or operand from execution address.

LOGICAL PRODUCT

12 LPN d Logical product d

22 LPC m Logical product m

27 LPD d Logical product (d)

Replaces (A) with logical product of (A) and d, m, or operand from execution address.

SELECTIVE CLEAR

13	SCN d	Selective clear (A) with d

Forces to 0 A bits that correspond to 1 bits in d.

LOAD

14	LDN d	Load d
20	LDC m	Load m
30	LDD d	Load (d)
40	LDI d	Load ((d))
50	LDM m d	Load (m+(d))

Loads A with d, m, or operand from execution address.

LOAD COMPLEMENT

15	LCN d	Load complement d

Loads A with one's complement of d.

ADD

16	ADN d	Add d
21	ADC m	Add m
31	ADD d	Add (d)
41	ADI d	Add ((d))
51	ADM md	Add (m+(d))

Replaces (A) with (A) plus d, m, or operand from execution address.

SUBTRACT

17	SBN d	Subtract d
32	SBD d	Subtract (d)
42	SBI d	Subtract ((d))
52	SBM md	Subtract (m+(d))

Replaces (A) with (A) minus d, m, or operand from execution address.

PASS

24	PSN	Pass
66	PSN	Pass
67	PSN	Pass
74	PSN	Pass

Performs no operation.

RETURN JUMP (ROM)

25	RJR md	Return jump to m+(d), ROM

Transfers (p)+2 to push-down stack and transfers control to execution address. Return occurs when program encounters pop stack (26) instruction and return address is at top of push-down stack.

POP STACK

26	POP	Pop stack to RJR caller

Removes address at top of push-down stack and transfers control to that address.

STORE

34	STD d	Store (d)
44	STI d	Store ((d))
54	STM md	Store (m+(d))

Stores (A) at execution address. (A) remains unchanged. Execution address must be less than $20\ 000_8$.

REPLACE ADD

35	RAD d	Replace add (d)
45	RAI d	Replace add ((d))
55	RAM md	Replace add (m+(d))

Replaces (A) with (A) plus operand from execution address, then stores new (A) at execution address. Execution address must be less than $20\ 000_8$.

REPLACE ADD ONE

36	AOD d	Replace add one (d)
46	AOI d	Replace add one ((d))
56	AOM md	Replace add one (m+(d))

Replaces (A) with one plus operand from execution address, then stores (A) at execution address. Execution address must be less than $20\ 000_8$.

REPLACE SUBTRACT ONE

37	SOD d	Replace subtract one (d)
47	SOI d	Replace subtract one ((d))
57	SOM md	Replace subtract one (m+(d))

Replaces (A) with execution address operand minus one, then stores (A) at execution address. Execution address must be less than $20\ 000_8$.

CONDITIONAL JUMPS ON CHANNEL STATUS

60	IFJ md	Jump to m if input channel d full
61	IEJ md	Jump to m if input channel d empty
62	OFJ md	Jump to m if output channel d full
63	OEJ md	Jump to m if output channel d empty
64	AJM md	Jump to m if channel d active
65	IJM md	Jump to m if channel d inactive

Transfers control to m if channel d satisfies specified condition. Otherwise, resumes execution at (P)+2. For active/inactive jumps (64, 65), d must be 16.

NOTES

1. If channel full/empty status (for channels 0 through 15) does not change for 30 ms during 70, 71, 72, or 73 instruction, execution resumes at (P)+1 (70, 72) or (P)+2 (71, 73) and normal input channel 1 bit 9 (instruction deadman timeout) sets. If using channel 16 (special channel), the timeout is 4.5 s due to the channel deadman timer.

2. If d specifies channel 16 and that channel is inactive for instruction 71, 72, or 73, no operation results.

3. If channel 16 inactivates during block transfer on channel 16, program execution resumes at (P)+2 and A contains number of words not transferred.

SINGLE WORD INPUT

70	IAN d	Input to A from channel d

Transfers one word from input channel d to A. Transfer requires full channel but occurs regardless of active/inactive channel status.

NOTE

Bit 2^8 set allows echoing of NOCO through 15.

INPUT BLOCK TRANSFER

71	IAM md	Input (A) words to m from channel d

Transfers (A) words to memory from input channel d, starting at address m. The quantity m+(A) must be less than $20\ 000_8$.

SINGLE WORD OUTPUT

72	OAN d	Output from A on channel d

Transfers (A) to output channel d.

OUTPUT BLOCK TRANSFER

73 OAM md Output (A) words from m on channel d

Transfers (A) words from memory to channel d, starting at address m.

FLAG PULSE OUTPUT

75 OFN d Output flag pulse on channel d

Sends one-cycle flag pulse on channel d.

CONDITIONAL JUMPS ON CHANNEL BIT

76 JSM mcb Jump to m if channel c, bit b set

77 JNM mcb Jump to m if channel c, bit b not set

Transfers control to m if bit b of input channel c satisfies specified condition. Otherwise, resumes execution at (P)+2.

UNCRATING

Inspect the equipment and supplementary items for damage or shortage. Any damage or shortage should be reported promptly to Control Data and the carrier.

INSTALLATION PROCEDURE

The location of the controller on site must allow room for opening of front and rear doors to their maximum position (figure 3-1 gives controller dimensions).

POWER CONNECTIONS

Refer to the power distribution schematic in section 5 when connecting controller power.

1. Remove the six screws holding the metal panel section at the lower rear of the cabinet. Lift out panel.

2. Connect the 400-Hz, 3-phase power cable to A7TB5 as follows:

Power Lead	Terminal Pin
Neutral (white)	1
01 (black)	2
02 (red)	3
03 (orange)	4
Safety ground (green)	E13

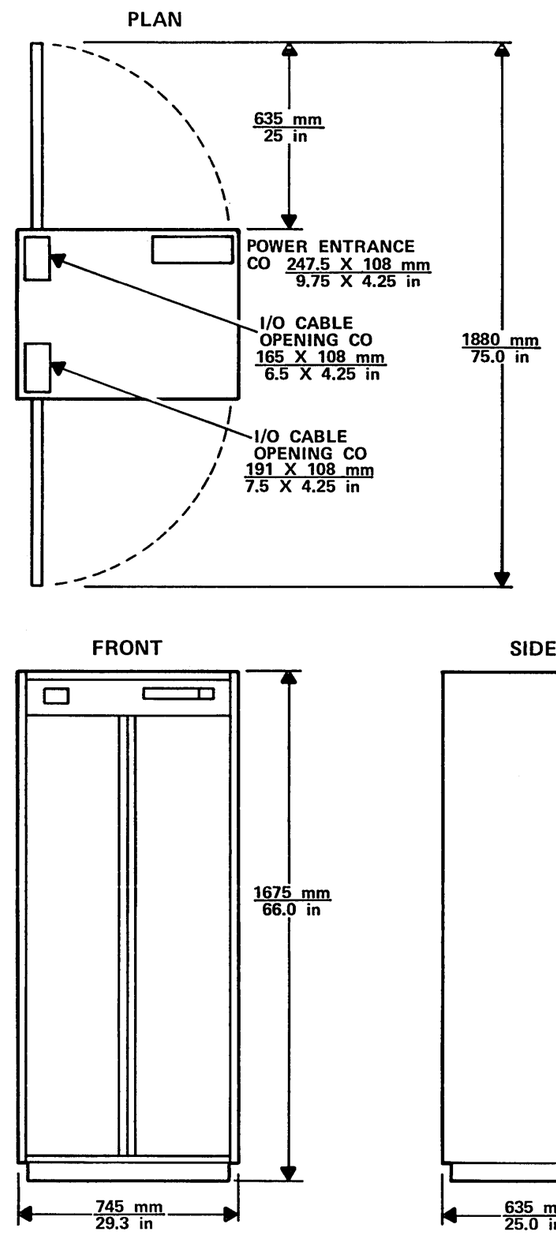


Figure 3-1. Controller Dimensions

3. Connect 50/60-Hz, single-phase power to A7TB4 as follows:

Power Lead	Terminal Pin
Neutral (white)	TB4-1
120 V (black)	TB4-2
220 V, 230 V, 240 V, or 250 V	TB4-3 and TB4-4

4. Select the appropriate tap on transformer A7T1 in the PD box using the following list as a reference.

S1 Pin	T1
9	Tap 1 (common)
7	Tap 2 (120 V)
8	Tap 3 (220 V) or tap 4 (230 V) or tap 5 (240 V) or tap 6 (250 V)
Safety ground	E12

5. Connect system ground strap to the lug on A7TB30.

FMD Power Sequence Connections

The power sequence circuit in a subsystem allows power to be applied to all units on the circuit from a single switch. To do this all units are connected serially with power sequence cables. The power sequence circuit causes all drives to power-up serially to prevent a very large demand for current caused by starting several drives simultaneously.

Each controller has a panel labeled 885 POWER SEQUENCE INTERFACE, shown in figure 3-2. This panel has a toggle switch labeled MASTER/SLAVE, and 10 receptacles to plug in power sequence cables. Each FMD has two receptacles to plug in power sequence cables from two power sequence circuits, and has a switch labeled LOCAL/REMOTE that enables the power sequence circuit at the drive if it is in the REMOTE position. A power up sequence from either circuit cycles up both spindles in a drive.

A power sequence circuit can consist of one or more controllers, each having from one to eight drives attached to it (two spindles per drive). When connecting the power sequence circuits, observe the following restrictions and characteristics.

- The first controller in the series must have its MASTER/SLAVE switch set to MASTER. All other controllers in the circuit (if any) must have this switch set to SLAVE.
- The LOCAL/REMOTE switch in the drives must be set to REMOTE to enable the power sequence circuit in the drive. The power must be applied at the drive if the switch is in the LOCAL position.
- Drive cables must be attached to the controller at the lowest numbered receptacle available; that is, unused receptacles must be the highest numbered.

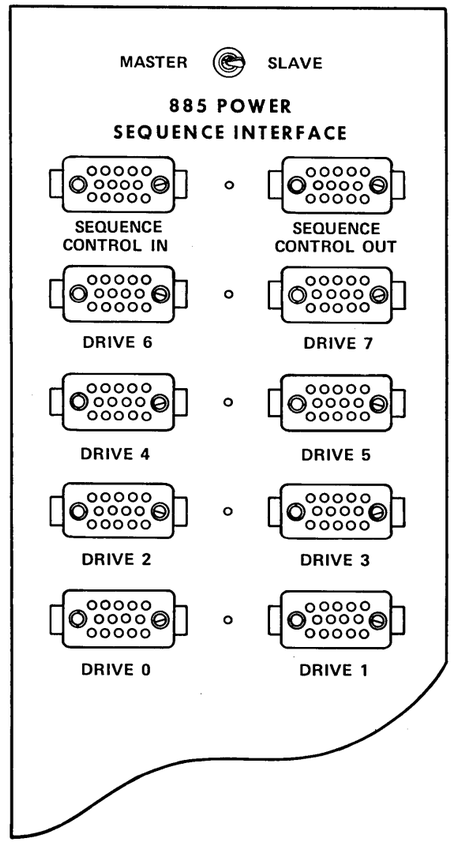


Figure 3-2. Power Sequence Interface Panel

- Attach a SLAVE controller's input cable from another controller at the receptacle labeled SEQUENCE CONTROL IN.
- Attach the output cable from one controller to another at the highest unused drive receptacle or, if all eight drive receptacles are used, at SEQUENCE CONTROL OUT. In the latter case, the cable goes from SEQUENCE CONTROL OUT to SEQUENCE CONTROL IN.
- Any drive set to LOCAL must be powered up at the drive. If the drive is cabled to the power sequence circuit, the circuit does not affect the drive and the drive does not affect the circuit.
- To remove power from a drive set to REMOTE that is cabled to two power sequence circuits, both circuits must power down. The drive continues to run if one circuit has removed power.

Figure 3-3 shows an example of a power sequence circuit.

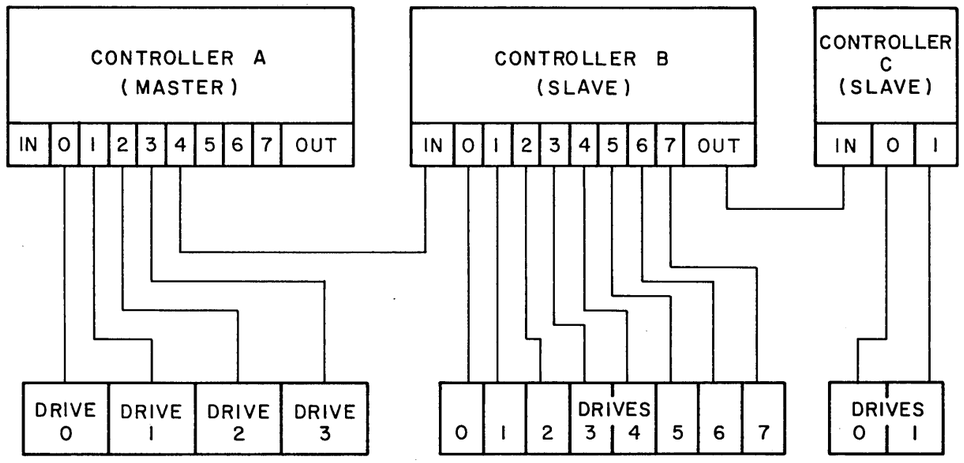

CONTROLLER A (MASTER)
IN 0 1 2 3 4 5 6 7 OUT
CONTROLLER B (SLAVE)
IN 0 1 2 3 4 5 6 7 OUT
CONTROLLER C (SLAVE)
IN 0 1
DRIVE 0
DRIVE 1
DRIVE 2
DRIVE 3
0 1 2 DRIVES 3 4 5 6 7
DRIVES 0 1

Figure 3-3. Power Sequence Cabling

Signal Cable Connections

Connect the CDC CYBER I/O cables from the PP at the top of the front connector panel. There are two cables for each PP channel connected to the controller.

Connect the I/O cable from each FMD spindle at the connector panel in the rear of the cabinet. Connect the two cables from each 844 drive at the front connector panel.

NOTE

The controller is the only peripheral unit on its PP channel. The 19.81-m (65-ft) I/O cables from the PP should be used.

Power Up

To apply power to the controller, perform the following steps.

1. Check the position of the PP CHANNEL ENABLE/DISABLE switches on the panel above the logic chassis.
2. Check the position of the 885 DRIVE ENABLE/DISABLE and 844 DRIVE ENABLE/DISABLE switches on the panel above the logic chassis.
3. Check the position of the parity enable switches on the 60-pak at chassis location A08. Set switches 1, 2, 3, and 4 to ON or OFF depending on the type of PP channel attached to the controller access. Switch 1 is access A, 2 is B, 3 is C, and 4 is D.
4. Check the position of the power loss protect switch. This switch, on the 60-pak at chassis location B13, should be in the up position to be on.
5. Put the POWER DISCONNECT switch in the ON position.
6. Put the 400-Hz circuit breaker in the ON position.
7. Using a voltmeter, measure -5.2 voltage at the power pin P1A02 or P1B02 on the backpanel at location B13. Adjust the variac if necessary.
8. Using a voltmeter, measure -2.2 voltage on the backpanel at pin P1A44 or P1B44 (any location). Adjust the variac if necessary.

The controller is now ready to run diagnostics.

CLOCK TUNING

The controller must be synchronized with the PP channel to operate properly. To do this two wires in the controller can be adjusted in length to synchronize the controller. These wires are adjusted at the factory before shipment to the customer site. If the controller clocks must be tuned at the site, use the following procedure.

NOTE

To tune clocks the CDC CYBER cables must be connected and the controller must be capable of receiving the 10-MHz Clock and Function signals from the PP.

1. Make sure scope is calibrated and probes are set.

2. All testpoint and backpanel pin references apply to the appropriate access being tuned, locations A01 through A04.

NOTE

If distance between clock pulses is not 100 ns, make sure the PPU is not running clock margins. If clock margins are normal, refer to figure 3-4.

3. Sync on and observe the 10-MHz clock, TP31. Distance between clock pulses should be 100 ns leading edge to leading edge.

NOTE

If the clock pulse is less than 29 to 30 ns, the wire will have to be cut off the coil wire on the access board. If it is longer than 30 ns, a longer coil wire will have to be added. 25.4 mm (1 in) of wire equals 0.8 ns. Refer to figure 3-4.

4. Sync on TP31 and observe channel 1 probe. Attach channel 2 probe to TP29, checking that the wide clock pulse that comes up after the 10-MHz clock is 29 to 30 ns leading edge to leading edge.

5. Send a function over the channel and sync on TP36. Attach channel 1 probe to TP36 and channel 2 probe to TP29. The leading edge of TP36 should precede TP29 by 3 to 6 ns as shown in figure 3-4. This should result in a 76- to 80-ns function pulse at TP36. The time that is critical is the relationship of TP36 to TP29 and not the length of the pulse at TP36. This relationship is controlled by a tuning wire on the backpanel P2B03 to P2A29 on the appropriate access location A01 through A04. If the relationship shown in figure 3-4 is more than 6 ns, the wire will have to be shortened. If it is less than 3 ns, a longer wire is needed. 203 mm (8 in) wire equals 1 ns.

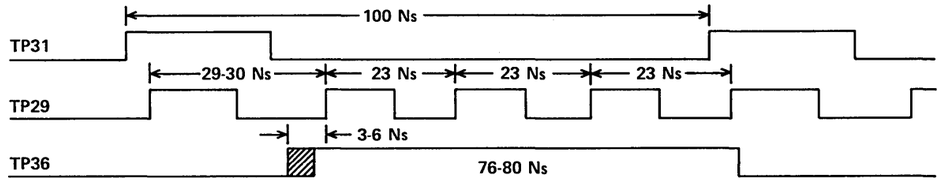


Figure 3-4. Clock Tuning Waveform

CHANNEL ACCESS OPTION INSTALLATION PROCEDURE

A maximum of three channel access options can be added to the model A controller and a maximum of four channel access options can be added to the model B controller. The following information applies to each one. Refer to section 7 for a complete breakdown of parts required to install this option.

1. Install channel R/T 60-pak in the logic chassis location that corresponds to the channel access to be added. A01, A02, A03, and A04 correspond to channel accesses A, B, C, and D respectively.

NOTE

Termination characteristics require that the model A controller have a channel R/T pak installed at location A01.

2. Install switch in switch panel. The switch panel is located at the front of the cabinet just above the logic chassis. Install switch from the rear in position labeled PP CHANNEL ENABLE, SW2 (access B), SW3 (access C), or SW4 (access D). Refer to figure 3-5.

3. Install other end of switch wires to the connector socket housing at chassis location A05 as follows:

   Access A to J1-5

   Access B to J1-6

   Access C to J1-7

   Access D to J1-8

   Refer to figure 3-5, detail C.

4. Mount cable bracket, using four bolts provided. Mount from the rear of the connector panel at appropriately labeled access position.

5. Install two connector socket housings on the 60-pak at A02, A03, or A04. Refer to figure 3-6 and to the CYBER Interface cable tabs in section 8.

6. Check the position of the parity enable switches on the 60-pak at chassis location A08. Set switches 1, 2, 3, and 4 to ON or OFF depending on the type of PP channel attached to the controller access. Switch 1 is access A, 2 is B, 3 is C, and 4 is D.

7. Run channel diagnostic tests.

844 DRIVE OPTION INSTALLATION PROCEDURE

This option adds an interface for eight CDC 844 removable-media disk storage units. Section 7 has a complete breakdown of parts required to install this option.

1. Make wire changes as indicated in section 8 FV670-A/B Modification Wire List.

2. Remove side skin from cabinet.

3. Remove RF seal that is bolted to the side of the I/O connector panel.

4. Disconnect PP I/O cables from connector panel.

NOTE

Remove pigtail connector from connector panel only. It is unnecessary to disturb the plastic block on the backpanel.

5. Remove I/O connector panel.

6. Install new connector panel (CDC part number 22939320).

7. Install PP I/O cables on new connector panel.

8. Install two power sequence wires coming from the I/O connector assembly 1P1 to the power sequence panel (figure 3-7). Install wires:

   1P1-h to TB1-5

   1P1-j to TB1-6

9. Install relay K1 on the power sequence panel. This panel label indicates position of relay.

10. Install connector socket housings on chassis row B, locations B05 through B12. Refer to Cable Placement Map, Row B, figure 3-8 and to the 844 Drive Option (model A) cable tabs in section 8.

11. Install switches in switch panel. Install in each switch from the rear in the appropriate switch position where the panel is labeled 844 ENABLE SW1 through SW8. Refer to FMD Wire Placement diagram, figure 3-5, detail A.

NOTE

If necessary for reasons of time, step 10 can be postponed until a time more convenient to the site. All accesses are enabled without the switches installed.

12. Install the two connector socket housings on the logic chassis backpanel, location B13. Refer to Cable Placement Map, Row B, figure 3-8.

13. Install the eight 60-paks in chassis locations B05 through B12.

14. Run diagnostics.

15. Check 844 power sequencing circuit.

16. Install RF panel.

17. Install side skin.

FOUR FMD OPTION INSTALLATION PROCEDURE

This option adds an interface for four FMD units (eight spindles). Section 7 has a complete breakdown of parts required to install this option.

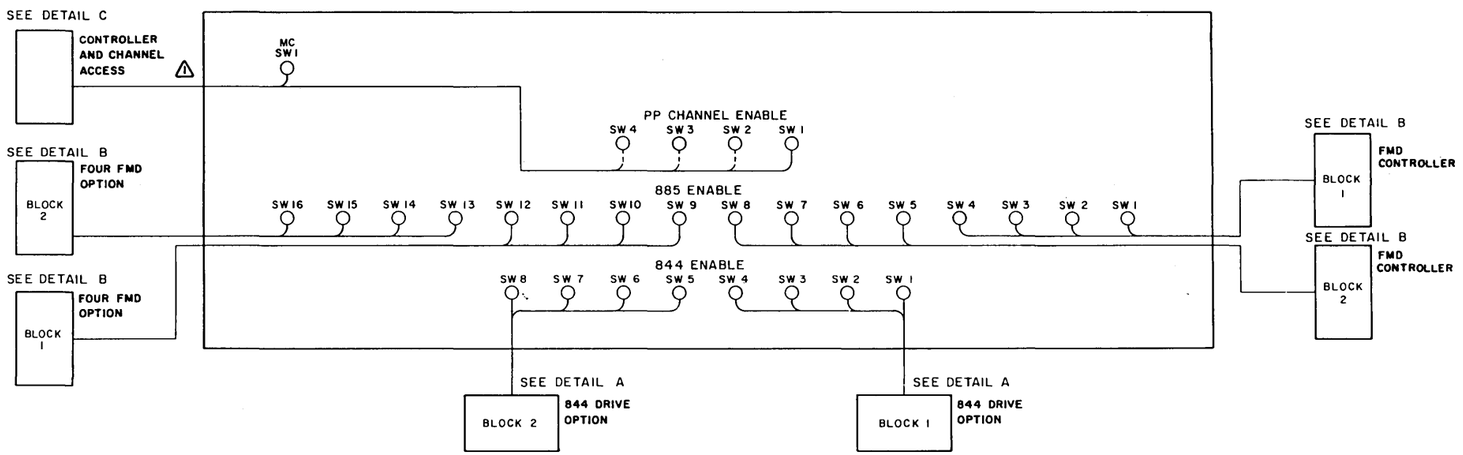
NOTE

If the 844 Drive Option and the Four FMD Option are both installed, the 844 Drive Option should be installed first, if possible.

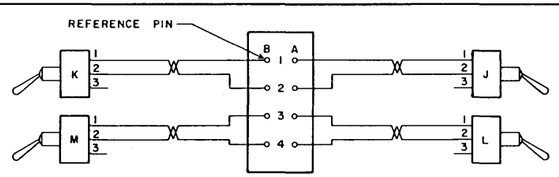
1. Install 60-paks in logic chassis at locations B14, B15, B16, and B17. Refer to chassis map in section 5 for placement.

2. Install one of the eight cable assemblies in the connector panel, bolting the connector assembly in place.

3. Install the connector socket housings in the backpanel of the logic chassis (figure 3-8). There are three for each unit. Install the three for the cable assembly (step 2) before proceeding to the next cable and its associated connector socket housing.



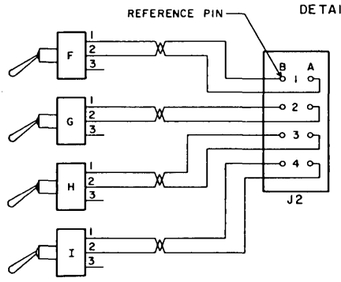
DETAIL A



844 UNIT ENABLE SWITCH PLACEMENT CHART

	SWITCH J		SWITCH K		SWITCH L		SWITCH M	
	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2
844 DRIVE OPTION 844 ENABLE	SW 4 844 UNIT 3	SW8 844 UNIT 7	SW3 844 UNIT 2	SW 7 844 UNIT 6	SW 2 844 UNIT 1	SW 6 844 UNIT 5	SW1 844 UNIT 0	SW 5 844 UNIT 4

DETAIL B



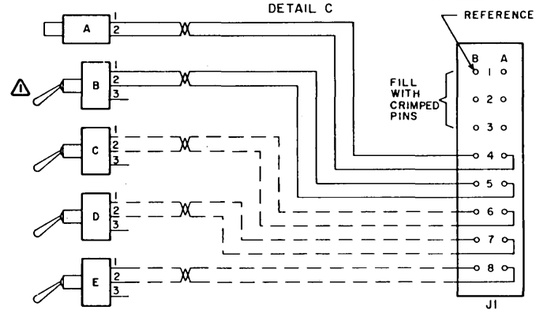
885 UNIT ENABLE SWITCH PLACEMENT CHART

	SWITCH F		SWITCH G		SWITCH H		SWITCH I	
	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2	BLOCK 1	BLOCK 2
FMD CONTROLLER 885 ENABLE	SW 4 885 UNIT 3	SW 8 885 UNIT 7	SW 3 885 UNIT 2	SW 7 885 UNIT 6	SW 2 885 UNIT 1	SW 6 885 UNIT 5	SW 1 885 UNIT 0	SW 5 885 UNIT 4
FOUR FMD OPTION 885 ENABLE	SW 12 885 UNIT 13	SW 16 885 UNIT 17	SW 11 885 UNIT 12	SW 15 885 UNIT 16	SW 10 885 UNIT 11	SW 14 885 UNIT 15	SW 9 885 UNIT 10	SW 13 885 UNIT 14

NOTE:

⚠ THE MODEL A CONTROLLER INCLUDES ONE CHANNEL ACCESS. THE MODEL B CONTROLLER DOES NOT INCLUDE A CHANNEL ACCESS.

DETAIL C



SWITCH A	SWITCH B	SWITCH C	SWITCH D	SWITCH E
SW 1 MC	SW 1 PP CHANNEL A ⚠	SW 2 PP CHANNEL B CHANNEL ACCESS OPTION	SW 3 PP CHANNEL C CHANNEL ACCESS OPTION	SW 4 PP CHANNEL D CHANNEL ACCESS OPTION

Figure 3-5. FMD Wire Placement Diagram

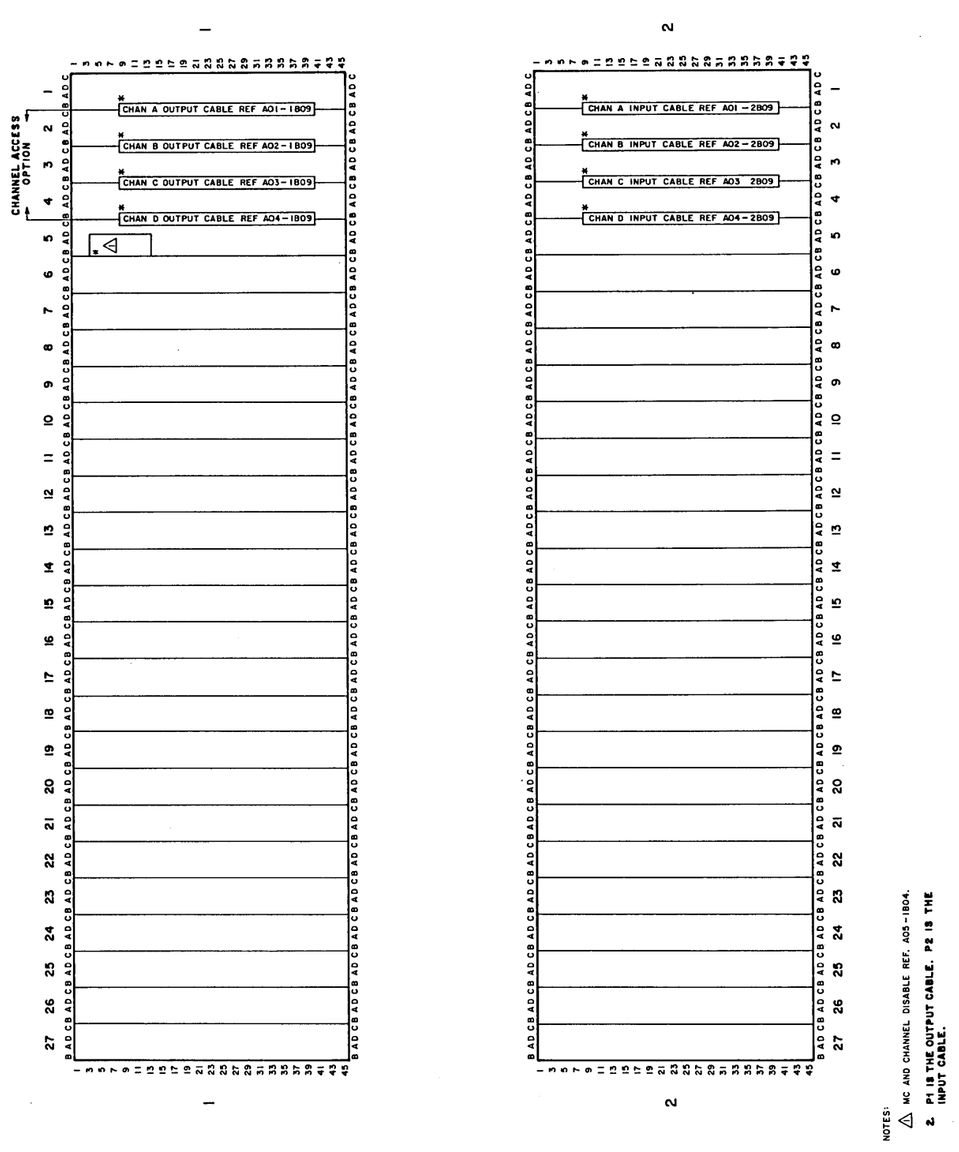

CHANNEL ACCESS OPTION
CHAN A OUTPUT CABLE REF A01-1809
CHAN B OUTPUT CABLE REF A02-1809
CHAN C OUTPUT CABLE REF A03-1809
CHAN D OUTPUT CABLE REF A04-1809
CHAN A INPUT CABLE REF A01-2809
CHAN B INPUT CABLE REF A02-2809
CHAN C INPUT CABLE REF A03 2809
CHAN D INPUT CABLE REF A04-2809
NOTES:
1. MC AND CHANNEL DISABLE REF. A03-1804.
2. P1 IS THE OUTPUT CABLE. P2 IS THE INPUT CABLE.

Figure 3-6. Cable Placement Map, Row A

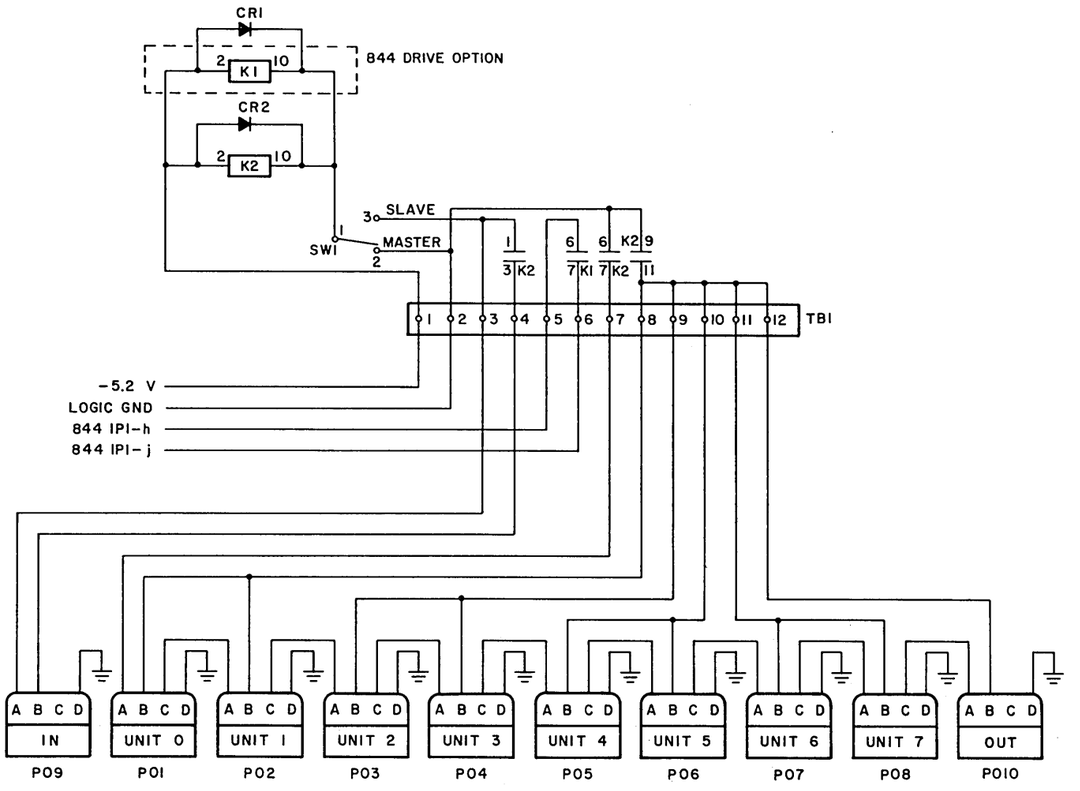


Figure 3-7. Power Sequence Wiring Diagram

4. Repeat steps 2 and 3 until all eight cables are installed.

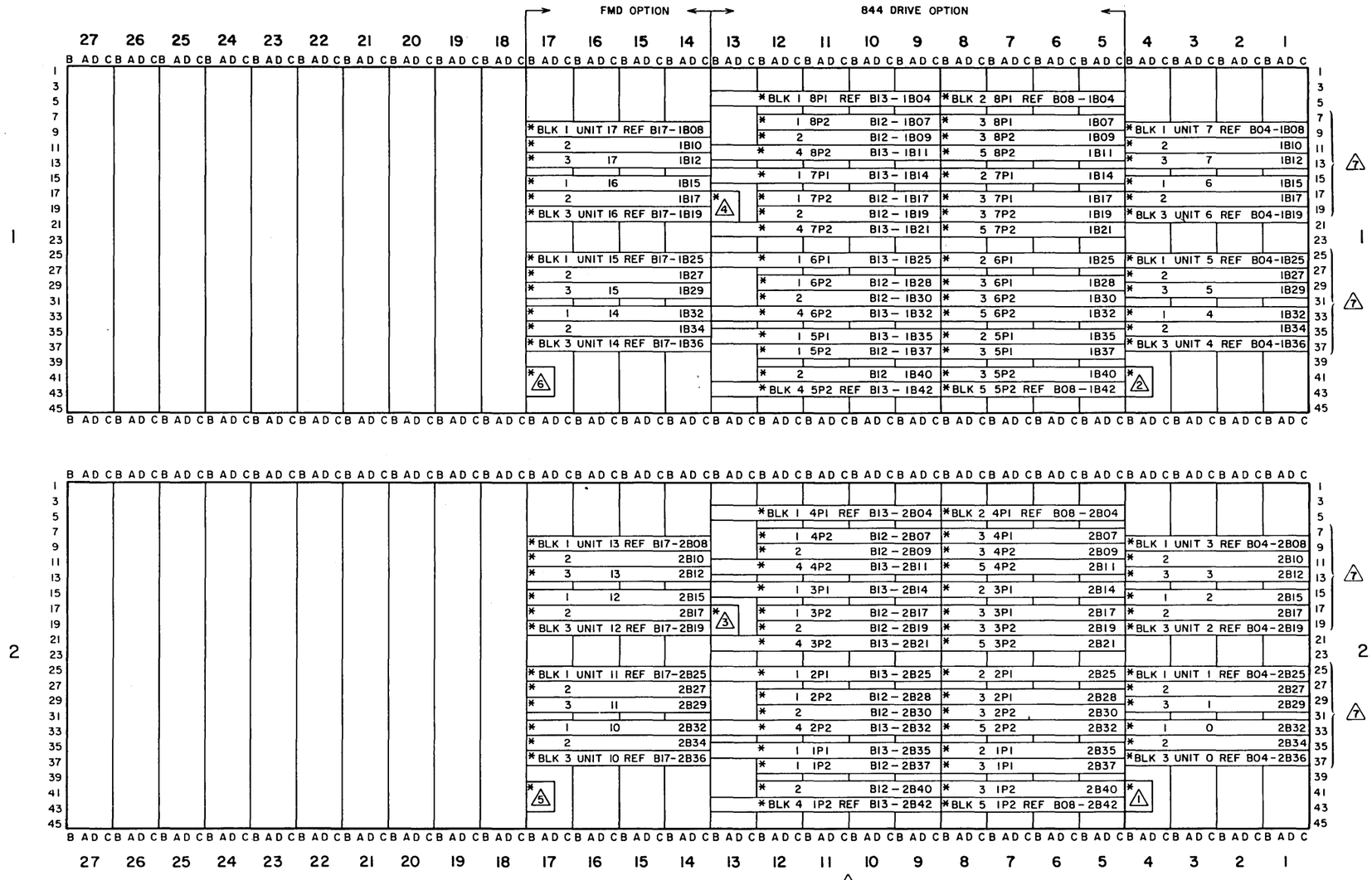
5. Install switches from the rear of the switch panel. The eight switches go in the holes labeled 885 ENABLE, SW9 through SW16. Refer to figure 3-5.

6. Install connector socket housings attached to switches. Refer to figure 3-8.

7. Route power sequence cables between the 885 POWER SEQUENCE INTERFACE panel (figure 3-2) and the FMD units.

8. Run appropriate diagnostics.

9. Check out power sequence circuit.



NOTES:

1. 885 UNIT DISABLE 0 ⟶ 3 REF. B04-2B40.
2. 885 UNIT DISABLE 4 ⟶ 7 REF. B04-1B40.
3. 844 UNIT DISABLE 0 ⟶ 3 REF. B13-2B17.
4. 844 UNIT DISABLE 4 ⟶ 7 REF B13-1B17.
5. 885 UNIT DISABLE 10 ⟶ 13 REF. B17-2B40.
6. 885 UNIT DISABLE 14 ⟶ 17 REF. B17-1B40.
7. THESE BLOCKS USED ON MODEL A CONTROLLER SERIAL 101 THROUGH 108 ONLY
8. 844 DRIVE OPTION CONNECTORS ARE LABELLED WITH STICKERS ON THE END WHERE THE REFERENCE PIN AND PIN 1 ARE LOCATED. THE LABELS INDICATE THE A SIDE, B SIDE, AND BLOCK NUMBER. THE ASTERISKS ON THE DIAGRAM ABOVE DENOTE THE END OF THE BLOCK WITH REFERENCE PIN.
9. 1P1, 1P2=UNIT 0; 2P1, 2P2=UNIT 1; 3P1, 3P2=UNIT 2; 4P1, 4P2=UNIT 3; 5P1, 5P2=UNIT 4; 6P1, 6P2=UNIT 5; 7P1, 7P2=UNIT 6; 8P1, 8P2=UNIT 7.

Figure 3-8. Cable Placement Map, Row B

INTRODUCTION

The model A controller includes one access to a PP data channel. Up to three Channel Access Options can be added to the model A controller. Up to four Channel Access Options can be added to the model B controller, which includes no access to a PP channel as standard equipment. Both the model A and model B controllers contain accesses for four FMD units (eight spindles).

The Four FMD Option adds four more FMD accesses to the controller. Each FMD has two spindles that must be addressed as separate units. The 844 Disk Option provides accesses for eight removable disk storage units.

This section describes the controller and its options.

INTERFACE DEFINITIONS

The definitions of signals on the three external interfaces in the controller follow. Figure 4-1 shows all interface signals.

PP INTERFACE

Signals From PP Only

10MHz Clock Signal

The controller uses this signal to synchronize all communication with a PP.

Active Signal

The PP sends this signal to initiate or resume communication with the controller.

Function Signal

This signal identifies the accompanying 12 data signals as a function code.

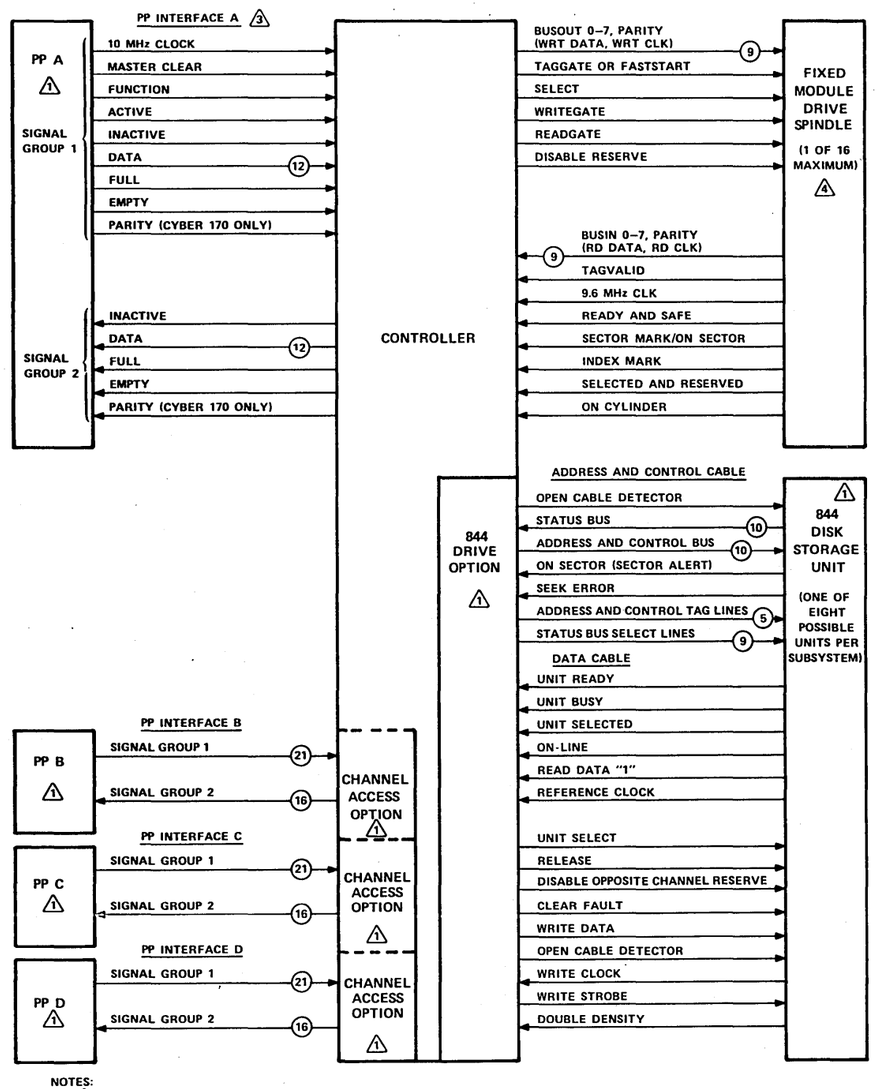
Master Clear Signal

The PP sends this signal to clear the controller as part of a computer system deadstart.

Bidirectional PP Interface Signals

Data 0-11 Signals

These 12 signals carry data, function, and status words between the PP and the controller.



NOTES:
1. NOT PART OF THE MODEL A OR MODEL B CONTROLLERS.
2. —(X)— INDICATES NUMBER OF LINES
3. THE CHANNEL A ACCESS IS PART OF THE MODEL A CONTROLLER. IT IS NOT PART OF THE MODEL B CONTROLLER.
4. ACCESSES FOR 8 FMD SPINDLES ARE INCLUDED WITH THE CONTROLLER. ACCESSES FOR THE OTHER EIGHT SPINDLES COME WITH THE FOUR FMD OPTIONS.

Figure 4-1. Interface Diagram

Parity (CDC CYBER 170 Only) Signal

This signal provides odd parity for the 12 data signals it accompanies.

Full Signal

This signal indicates to the receiver that the word formed by the 12 data signals can be accepted.

Empty Signal

This signal indicates to the transmitter that the receiver has accepted the word accompanying the last Full signal.

Inactive Signal

The controller replies to a Function signal (and its associated function code) with an Inactive signal. An Inactive signal may also be used by either the PP or the controller to terminate communication.

FMD INTERFACE

Controller to FMD Unit

Busout 0-7 (Write Data, Write Clock) Lines

These lines carry commands such as unit functions and other control information. Write data (nonreturn to zero, NRZ) is carried on busout 0. Write clock (NRZ) is carried on busout 1.

Parity Line

This line carries a parity bit with every byte sent on the busout lines. Odd parity is used.

Tag Gate Signal

This signal identifies the data on the busout lines as control or status functions. The signal gates the commands into the unit. (This signal is on the same line as Fast Start.)

Fast Start Signal

This signal is used only when reading data fields. This signal locks phase lock oscillator to data. (This signal is on the same line as Tag Gate.)

Select Signal

This signal selects the drive unit unless the unit is busy or off line. The unit responds to this signal by sending a Select and Reserved signal back to the controller.

Write Gate Signal

This signal enables the write driver in the unit. The controller must send Write Data and Write Clock to the unit before sending Write Gate.

Read Gate Signal

This signal enables read data on the read line.

Disable Opposite Channel Reserve Signal

This signal releases the reserved condition on the other controller access of the drive unit. Unit status does not affect the execution of this operation. (This operation should be used only when other channel access is known to be inoperative.)

FMD Unit To Controller

Busin 0-7 (Read Data, Read Clock) Lines

These lines carry unit status to the controller. Read data (NRZ) is carried on busout 0. Read clock (NRZ) is carried on busout 1.

Parity Line

This line carries a parity bit with every byte sent on the busin lines. Odd parity is used.

Tag Valid Signal

The drive unit sends this signal to indicate that it has completed the tag sequence and to indicate that unit status is valid.

Ready and Safe Signal

This signal remains set until one of the following error conditions occurs in the unit:

- STOP switch is on.
- Motor not up to speed.
- HDA sequence error.
- Seek time out.
- Seek overshoot.
- Servo off track.
- Read/write errors:

  Write Gate and no control select
  Head short
  Write attempted when unit is offset
  Multihead error
  Capable enable error
  Write overrun

Control error
Write transition error
Write current error

- Unit check:

  Sector compare error
  Index error
  Decode parity error
  Busout parity error
  Illegal command

Even with Ready and Safe clear, the unit executes nonmotion functions, but ignores Write Gate and Read Gate.

Sector Mark/On Sector Signal

This signal indicates detection of a sector mark (start of the data record). If the detected sector mark has been addressed (seek operation in process), the signal stays set and indicates an on sector condition.

Index Mark Signal

This 17-ms signal is a reference signal to mark the start of each disk revolution.

Select and Reserved Signal

This signal is a response to the Select signal indicating that the controller has successfully reserved the unit.

On Cylinder Signal

This signal indicates that the drive is on the addressed track.

9.6 MHz Clock Signal

This signal is used to generate the NRZ write clock sent on busout bit 1 during a disk write operation.

844 INTERFACE

Address and Control Cable

Status Bus

The status bus consists of 10 lines that carry status information from the unit to the controller. Information on the status bus is determined by Status Select signals sent from the controller to the unit. Table 4-1 shows the relationship of the status select lines to the status bus.

Address and Control Bus

The address and control bus consists of 10 lines that carry information from the controller to the unit. Information on these lines is determined by Address and Control Tag signals that are sent from the controller to the unit. Table 4-2 shows the relationship of the tag lines to the address and control bus.

Address and Control Tag Lines Received by the Unit†

Difference Select - This signal indicates that the address and control bus contains positioning information (the difference between the unit's present cylinder address and the controller's new cylinder address).

Cylinder Select - This signal indicates that the address and control bus contains the controller's new cylinder address.

Sector Select - This signal indicates that the address and control bus contains the address of the sector which generates the next On Sector signal.

Head Select - This signal indicates that the address and control bus contains the address of the head to be selected.

† Refer to table 4-2.

Table 4-1. Status Select Line Functions

Status Select Lines									
Status Bus	Read Cylinder Select	Read Differential Control	Read Head Register	Read Sector Control	Read Sector Register	Read Interlock	Read Position	Read Fault	Read Control
Bit 0	1	1	1	1	1	Pack on	Forward	(W+R) On Cyl	Sector
Bit 1	2	2	2	2	2	Sector block	Reverse	W R	Pack unsafe
Bit 2	4	4	4	4	4	Heads loaded	Cylinder pulse	Current	Seek incomplete
Bit 3	8	8	8	8	8	Brush cycle	End of travel	+ Volt	On cylinder
Bit 4	16	16	16	16	16	Start switch	Fine servo	- Volt	Index
Bit 5	32	32				Local remote	Speed	Seek	EOT seek error
Bit 6	64	64				Spindle motor on		AC write fault	End of cylinder
Bit 7	128	128				Power supply tempera-ture			
Bit 8	256	256		Control valid					
Bit 9	512	512							

Table 4-2. Tag Line Functions

Address and Control Bus	Difference Select	Cylinder Select	Tag Line		Control Select
			Sector Select	Head Select	
Bit 0	1	1	1	1	Write Gate
Bit 1	2	2	2	2	Read Gate
Bit 2	4	4	4	4	Seek Forward
Bit 3	8	8	8	8	Head Advance
Bit 4	16	16	16	16	Not used
Bit 5	32	32			Seek Reverse
Bit 6	64	64			Return to Zero (RTZ)
Bit 7	128	128			Data Strobe Early
Bit 8	256	256			Data Strobe Late
Bit 9	512	512			

Control Select - This signal indicates that the address and control bus contains control information with the following bit assigmments.

Bit	Signal	Function
0	Write Gate	Enables write driver.
1	Read Gate	Enables digital read data on the read data lines.
2	Seek Forward	Initiates the positioning sequence in the forward direction if the difference counter contains a number greater than zero. If the difference counter equals zero, a forward carriage offset results.
3	Head Advance	Increments the head counter by one.

NOTE

This signal occurring with the End of Cylinder signal clears the head counter.

4	Not Used	

Bit	Signal	Function
5	Seek Reverse	Initiates the positioning sequence in the reverse direction if the difference counter contains a number greater than zero. If the difference counter equals zero, a reverse carriage offset results.
6	Return to Zero	Initiates positioning to cylinder zero, and clears seek error condition if one exists.
7	Data Strobe Early	When this signal is true, the data strobe is moved to the early margin position.
8	Data Strobe Late	When this signal is true, the data strobe is moved to the late margin position.

On Sector (Sector Alert)

This is an unselected status line that indicates that the addressed sector is one sector away from the heads. The On Sector signal is one sector in length and occurs once per revolution until a read gate, clear, or release is received. The On Sector signal is disabled while a seek command is in process.

Seek Error

This is an unselected status line. It indicates that the unit was unable to complete a move within 625 ms or that the carriage has moved to a position outside the recording field. A return to zero seek command clears the seek error condition, returns the heads to cylinder zero, and enables an On Cylinder signal to be sent to the controller.

Status Bus Select Lines†

Read Cylinder Select (Controller to Unit) - This signal gates the contents of the unit cylinder register to the controller on the status bus.

Interlock Select (Controller to Unit) - This signal gates unit interlock status to the controller with the following bit assignments on the status bus.

Bit	Signal	Function
0	Pack On	Indicates a pack is mounted on the spindle.
1	Sector Block	Indicates the unit cover is closed and sector block is in position to sense sector disk.
	or	
	Control Interlock	Indicates the unit cover is closed, all dc circuit breakers are closed, and the start switch is on.
2	Heads Loaded	Indicates heads have been loaded on the disk pack.
3	Brush Cycle	Indicates pack brush cycle is in progress.
4	Start Switch	Indicates start switch is on.
5	Local/Remote	Indicates unit sequencing power is under control.
6	Spindle Motor	Power is applied to the spindle motor.
7	Power Supply Temperature	Indicates power supply temperature normal.
	or	
	Logic Temperature	Indicates logic chassis temperature normal.
8	Not Used	

Read Head Register Select - This signal gates the contents of the unit head register to the controller.

Read Difference Counter Select - This signal gates the one's complement of the contents of the unit difference counter to the controller on the status bus.

Read Sector Counter Select - This signal gates the contents of the unit sector counter to the controller on the status bus. Bit 8 is Sector Counter Valid signal. When this line is true, the ouput of the sector counter is not in the process of changing. The counter contents are one number ahead of the actual sector count.

Read Sector Register Select - This signal gates the contents of the unit sector register to the controller on the data bus.

Read Position Status Select - This signal gates positioner control status to the controller on he data bus with bit assignment as follows:

Bit	Signal	Function
0	Forward	Indicates the forward latch is set.
1	Reverse	Indicates the forward latch is cleared.
2	Cylinder Pulse	Transmits cylinder pulses during a positioning function.
3	End of Travel	Indicates the heads have been positioned beyond the usable recording field in either the forward or reverse direction.
4	Fine Servo	Indicates the heads are being positioned under fine servo control and are less than 1/2 track from the final destination.
5	Speed & Mtr On	Indicates the pack is rotating at a speed safe for flying the heads.

† Refer to table 4-1.

Read Fault Status Select - This signal gates the contents of the fault register to the controller on the status bus with the following bit assignments.

Bit	Signal	Function
0	$\frac{(W+E+R)\bullet}{On\ Cyl}$	Indicates a write, erase, or read gate has been received while unit was off cylinder.
	or	
	(W+R) • On Cyl	Indicates a write or read gate has been received while unit was off cylinder.
1	(W+E) • R	Indicates a write or erase gate has been received while the read gate is true.
	or	
	W • R	Indicates a write gate has been received while the read gate is true.
2	Current	Indicates one or more of the following fault conditions. • More than one head selected. • Erase and no write driver on. • Write drive on and no erase. • Both write drivers on. • Write gate without write data.
3	+Volt	Indicates abnormal positive voltage in the unit.
4	-Volt	Indicates abnormal negative voltage in the unit.
5	Seek	Indicates a seek error has occurred.
6	AC Write Fault	Indicates write gate without write data.
7	Not Used	

Read Control Status Select - This signal gates the following control functions to the controller on the status bus.

Bit	Signal	Function
0	Sector Mark	Indicates start of record.
1	Pack Unsafe	Indicates a unit fault has occurred.
2	Seek Error	Indicates unit was unable to complete a move within 625 ms or that the carriage has moved to a position outside the recording field.
	or	
	Seek Incomplete	Indicates unit was unable to complete a move within 575 + 175 ms or that the carriage has moved to a position outside the recording field. A return-to-zero seek command clears the seek error or seek incomplete condition, returns the heads to cylinder zero, and enables an On Cylinder signal to the controller.
3	On Cylinder	Indicates unit has completed a move to the addressed cylinder.
4	Index	Track reference signal. This signal occurs once per revolution. The leading edge is coincident with the leading edge of the sector zero sector mark.
5	EOT Seek Error	Indicates that the carriage has moved to a position outside the recording field. A return-to-zero seek command clears the EOT seek error condition, returns the heads to zero, and enables an On Cylinder signal to the controller.
6	End of Cylinder	This line indicates the head counter has been advanced beyond head 18.
7	Not Used	
8	Not Used	

Data Cable

Unit Ready (Unit to Controller) Signal

This signal indicates the selected unit has completed a first seek. It is cleared when the heads have unloaded with the spindle motor off. The unit does not accept seek commands until ready.

Unit Busy (Unit to Controller) Signal

This signal indicates the selected unit is reserved by another channel. It applies to multiaccess use only.

Unit Selected (Unit to Controller) Signal

This signal indicates the selected unit is available and that its unit select input is true.

On-Line (Unit to Controller) Line

This is a single-ended line operated from the on-line switch. An open condition indicates an off-line status, and the controller should disable the interface to this unit.

Read Data 1 (Unit to Controller) Line

This line transmits the recovered data in the form of pulses-on-ones information after the data has been separated from the read clock.

Reference Clock (Unit to Controller)

The reference clock defines the beginning of a data cell. It is an internally derived reference signal and is synchronous with recorded data.

Unit Select (Controller to Unit) Line

This line selects the unit for communication with the controller unless the unit is busy or off-line. The unit returns a Unit Selected signal in response to this signal.

Release (Controller to Unit) Line

This line clears the reserve in the selected unit. Unit select and release may occur at the same time.

Disable Opposite Channel Reserve (Controller to Unit) Signal

This signal releases all units reserved by the opposite channel without regard for unit status. It should be used only when it is known that the opposite channel is inoperative.

Clear Fault Line

This line clears the Fault flip-flop and the fault register in the selected unit.

Write Data Line

This line carries data to be recorded on the disk pack. Coding is nonreturn to zero (NRZ). The bit rate for the unit is 6.451 MHz.

Open Cable Detector Lines

One of these lines is in each cable; it is a signal to the unit indicating that the unit is connected to the controller. This line also gives controller power loss protection to the drive.

Write Clock (Unit to Controller) Line

This line carries a 6.451-MHz clock used to generate NRZ write data in the controller and returned to the unit as write strobe. This is a continuous frequency synchronized with unit spindle speed variations for maximum data capacity.

Write Strobe (Controller to Unit) Line

This line returns the write clock to the unit to compensate for I/O cable propagation differences by synchronizing NRZ write data with unit internal write clock.

Double Density (Unit to Controller) Line

This line indicates that a double density unit is selected. Both sides of this differential signal are connected to ground in the unit.

PROCESSOR NORMAL CHANNELS

The controller processor uses 17 bidirectional registers/channels to communicate with and control the rest of the controller. Each channel has 16 input bits, 16 output bits, an input full pulse, input empty pulse, input flag pulse, output full pulse, output empty pulse, and an output flag pulse. The normal channel signals are defined in the following pages. Table 4-3 defines all channel bits.

Output Full Pulse

A 72 (output from A) or 73 output (A) instruction strobes the output full pulse 42 ns after the processor has sent new information to the respective normal output channel register. This pulse sets the Full Status flip-flop. Output empty pulse resets Full Status flip-flop.

Output Empty Pulse

Controller hardware sends this to processor in response to output full. Output empty resets output full status.

Output Flag Pulse

A 75 (output flag) instruction generates an output flag pulse. This pulse is 85 ns long and is usually used to clear hardware or initiate action in the controller.

Input Full Pulse

The controller hardware generates an input full pulse, setting the Input Full Status flip-flop. This indicates that the selected normal input channel has information for the processor. A 70 (input to A) or 71 input (A) instruction causes the processor to read the selected channel information into the processor accumulator or memory, and to return an input empty pulse. Input empty resets input full status. Some channels have input full tied high to allow greater flexibility.

Table 4-3. Channel Bits (Sheet 1 of 2)

NIC0 – COUPLER STATUS
NOC0 – COUPLER CONTROL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Master Clear	NU	Channel Parity Enabled	Program Memory P.E.	NU	NU	NU	Correction In Progress	Output Register Full	Input Register Full	Channel Reserved	Channel Deadman Timer	Channel Active	Parity Error On Current Word	Function	Connected
NU						8	7	6	5	4	3	2	1	Coupler Access Mux 2^1	2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Clear Connect	NU	Tie High

NIC1 – CONTROLLER STATUS
NOC1 – CONTROLLER CONTROL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lost Clock	NU	NU	NU	ECC Nonzero	RAM Data Parity Error	Instruction DMT	Lost Control Word	Up/Down Count ≠ 0	Not Ready and Safe or Pack Unsafe	Buffer Memory Output Reg. P.E.	Write Verify Compare Error	Sync Byte Search	Sector Length Violation	Lost Data	Sync Byte Miscompare
Loop 885 Bus	Loop 885 Decode	Force Buffer Memory P.E.	Force Program Memory P.E.	Force FMD Bus P.E. Out	Force FMD Bus P.E. In	Disable Program Memory P.E. Stop	NU	FMD Disable Opposite Channel	FMD Select	FMD Unit	NU	Unit No. 2^3	Unit No. 2^2	Unit No. 2^1	Unit No. 2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Master Clear Control Logic	Load Unit No.	Tie High

NIC2 – ADDRESS FIELD1
NOC2 – SYNC BYTE CONTROL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}															2^0
NU								Write Verify	Skip Sector Mark			Sync Byte Pattern			

Input Flag	Full	Empty
NU	Address Reg Full	NU
Flag Pulse	**Full**	**Empty**
Start Error Correction	NU	Tie High

NIC3 – ECC REGISTER STATUS
NOC3 – HEAD AND PARCEL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}															2^0
NU														Parcel Decode 2^1	2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Clear ECC Register	NU	Tie High

NIC4 – BIT COUNT STATUS
NOC4 – BIT COUNT LOAD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}															2^0
2^{15}															2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Clear Status	Load	Resume

NIC5 – CONTROL WORD STATUS
NOC5 – CONTROL WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}															2^0
Send Inactive	Clock Selection 2^1	2^0	Enable ECC Shift Clock	Invert Data To/From ECC Reg.	Write ECC/ Read ECC	Enable ECC Feedback	Enable Data to Buffer	Mark Start Delay 2^1	2^0	Sync Byte Search	Fast Start	Write Gate	Read Gate	Select 16-Bit Mode	Write Sync Byte

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Terminate Control	Load	Resume

NIC6 – BUFFER ADDR STATUS
NOC6 – BUFFER ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	Tie High	2^{11}											2^0
Load/ Select Status	Write	Read	NU	2^{11}											2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Clear PP Interface	Load	Tie High

NIC7 – UP/DOWN COUNT
NOC7 – UP/DOWN COUNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	NU	2^{11}											2^0
Maint. Loop	Buffer Direction PP to Disk	Disable Processor To Buffer	NU	2^{11}											2^0

Input Flag	Full	Empty
NU	Tie High	NU
Flag Pulse	**Full**	**Empty**
Set Reserve	Load	Tie High

Table 4-3. Channel Bits (Sheet 2 of 2)

NIC8 – 885 STATUS / NOC8 – 885 FUNCTIONS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
Index	Sector Mark/ On Sector	On-Cyl	Sel & Reserved	Ready & Safe	On Sector	Status Valid	Status Parity Error	Selected/Echo Status								NU	Tie High	NU
Bus Data								Decode								Flag Pulse	Full	Empty
																NU	Initiate FMD Function	Tie High

NIC9 – CONTROLLER / NOC9 – 844 TAG LINES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
2^7			CONTROLLER NUMBER				2^0		NU		4K Buffer	NU	Write Gate Xmtr.	Read Gate Xmtr.	Tag Xmtr.	NU	Tie High	NU
NU								Select	Clear Fault	Release	Clear Opposite Channel	Status Select				Flag Pulse	Full	Empty
												2^3	2^2	2^1	2^0	Clear MC Status	NU	Tie High

NIC10 – 844 BUS DATA/STATUS / NOC10 – 844 BUS DATA/CONTROL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
Sector Alert	Seek Error	Unit Busy	Selected	Ready	On-Line	2^9									2^0	NU	Tie High	NU
Difference	Cylinder	Head	Sector	Control	Equip Sel	2^9									2^0	Flag Pulse	Full	Empty
																NU	NU	Tie High

NIC11 – CORRECTION LENGTH / NOC11 – CORRECTION LENGTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
2^{15}															2^0	NU	Tie High	NU
844								885								Flag Pulse	Full	Empty
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Load ECC Reg.	NU	Tie High

NIC12 – POLYNOMIAL PARCEL I / NOC12 – POLYNOMIAL PARCEL I

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
2^{15}															2^0	NU	Tie High	NU
2^{15}															2^0	Flag Pulse	Full	Empty
																NU	NU	Tie High

NIC13 – POLYNOMIAL PARCEL II / NOC 13 – POLYNOMIAL PARCEL II

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
2^{15}															2^0	NU	Tie High	NU
2^{15}															2^0	Flag Pulse	Full	Empty
																NU	NU	Tie High

NIC14 – POLYNOMIAL PARCEL III / NOC14 – POLYNOMIAL PARCEL III

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
2^{15}															2^0	NU	Tie High	NU
2^{15}															2^0	Flag Pulse	Full	Empty
																NU	NU	Tie High

***SPECIAL CYBER INPUT CHANNEL / *SPECIAL CYBER OUTPUT CHANNEL**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Input Flag	Full	Empty
NU	NU	NU	NU	2^{11}											2^0	Channel Inactive	Full From PP	Empty to PP
NU	NU	NU	NU	2^{11}											2^0	Flag Pulse	Full	Full
																Inactive	Full to PP	Empty From PP

*SPECIAL CYBER INPUT CHANNEL GOES FROM PP OUTPUT CHANNEL TO PROCESSOR.
SPECIAL CYBER OUTPUT CHANNEL GOES FROM PROCESSOR TO PP INPUT CHANNEL.

Input Empty Pulse

Processor generates this pulse after reading an input channel. This clears input full status. Input empty is not transmitted during an echo instruction.

Input Flag Pulse

This pulse sets the Input Flag Status flip-flop. It terminates any input block transfer after the first word is read. Input empty pulse resets input flag status.

INPUT 0 - COUPLER STATUS

Input 0/Empty

Not used.

Input 0/Full

Constant 1.

Input 0/Flag

Not used.

Input 0/0

Connect. PP channel is connected to the controller.

Input 0/1

Function. Controller has received function from connected PP channel. Cleared by output 6/flagpulse, output 16/flagpulse, or PP-generated inactive pulse.

Input 0/2

Current word parity error. Data in channel register for connected PP channel has even parity.

Input 0/3

Channel inactive. Connected PP channel not in block transfer mode.

Input 0/4

Channel deadman timeout. Connected, active PP channel has not transferred a word for 4.5 ± 1.5 s. Controller has sent inactive pulse to PP channel and released connect.

Input 0/5

Channel reserved. Connected channel access can read from or write into buffer memory. Set by output 7/flag. Cleared by PP inactive or output 16/flag.

Input 0/6

Input register full. Register feeding buffer memory contains data.

Input 0/7

Output register full. Register receiving data from buffer memory contains data.

Input 0/8

Correction in progress. Checkword hardware is cycling to determine whether checkword error is correctable. Output 2/flag initiates correction cycling. Correction expires when the operation finds a correctable checkword vector or when the bit count which was loaded on output 4/0 to 15 equals zero.

Input 0/9 to 11

Not used.

Input 0/12

Program memory parity error. Processor detected parity error while accessing the 4-K read/write program memory, the 2-K buffer memory (model A controller) or 4-K buffer memory (model B controller), or the 1-K program ROM. Processor halts on an error unless output 1/9 is set (instruction deadman timeout). Processor halts unconditionally on an error while accessing the ROM.

Input 0/13

Channel parity enabled. Indicates that the channel access selected by NOCO, bits 0, 1 has parity check enabled.

Input 0/14

Not used.

Input 0/15

Channel master clear. Indicates that a master clear pulse has been received by the channel selected by Output 0/0 and 1.

OUTPUT 0 - COUPLER CONTROL

Output 0/Empty

Constant 1.

Output 0/Full

Not used.

Output 0/Flag Pulse

Unconditionally releases a connected PP access.

Output 0/0 and 1

PP access multiplex code. Contains a code that selects one of four PP accesses. Codes and accesses are as follows:

Code		
Bit 1	Bit 0	Access
0	0	A
0	1	B
1	0	C
1	1	D

Output 0/2 to 9

Indicator lights. Light eight light-emitting diodes located on the 60-pak at location A16.

Output 0/10 to 15

Not used.

INPUT 1 - CONTROLLER STATUS

Input 1/Empty

Not used.

Input 1/Full

Constant 1.

Input 1/Flag Pulse

Not used.

Input 1/0

Sync byte miscompare. Drive sync byte (110011 for 844 or 11001 for 885) did not match the pattern in output 2/0 to 5.

Input 1/1

Lost data. When writing on the disk, the buffer did not provide data to the shift register fast enough to match the disk transfer rate. When reading from the disk, the buffer did not remove data from the shift register fast enough to match the disk transfer rate. Lost data halts a read or write.

Input 1/2

Sector length violation. Read gate or write gate was present when the controller detected the sector mark. Error halts the operation in progress.

Input 1/3

Sync byte search. Sync byte search operation is in progress.

Input 1/4

Write verify compare error. Controller detected a difference between data in the buffer and data sent by the disk during a write verify operation. Error does not halt the operation.

Input 1/5

Buffer memory output register parity error. Controller detected a parity error in a word in the output register during a buffer read. Error does not halt operation.

Input 1/6

885 drive not ready and not safe, or 844-4x pack unsafe. Selected drive is unsafe because of a failure.

Input 1/7

Up/down count not zero. Number of buffer words read was less than the number of buffer words written if the counter was preset to zero prior to a normal read or normal write.

Input 1/8

Lost control word. During a control word sequence, bit counter went to zero with no new control word available on normal output channel 5.

Input 1/9

Instruction deadman timeout. During 70, 71, 72, or 73 processor instruction, 30 $\pm$ 3 ms elapsed without selected channels full/empty status changing (i.e., no word transferred for 30 $\pm$ 3 ms). All 71, 72, or 73 instructions for any normal or special channel fall through until a master clear clears input 1/9.

Input 1/10

Data parity error. Controller detected a parity error on a 12-bit byte sent to the buffer during a block transfer. Input 1/10 does not halt the operation.

Input 1/11

ECC residue nonzero. One (or more) bit in the EDAC register is nonzero. If tested at the completion of a read, it indicates a checkword error. If set after completion of correction in progress (input 0/8), it indicates uncorrectable checkword error.

Input 1/12 to 14

Not used.

Input 1/15

Lost clock. Controller did not receive a clock transition for 340 ns on the read or write clock lines from the drive.

OUTPUT 1 - CONTROLLER CONTROL

Output 1/Empty

Constant 1.

Output 1/Full

Loads disk drive unit number (in output 1/0 to 3) into controller.

Output 1/Flag

Unconditionally master clears controller logic, including normal channel bits. Does not clear CYBER channel connect logic or processor.

Output 1/0 to 3

885 or 844 unit number.

Output 1/4

Not used.

Output 1/5

FMD unit. Logical one enables the 885 drive data path for reading and writing. Logical zero enables 844 drive data path for reading and writing.

Output 1/6

FMD select. Sends select line to 885 drive selected by output 1/0 to 3. FMD select must be issued after and dropped before output 1/0 to 3. Select in the drive follows leading edge of FMD select within 500 ns.

Output 1/7

FMD clear other channel. When accompanied by FMD select, releases the reserve on the other access in the selected drive. Release is done without regard to unit status, and should be used only when other access is inoperative. Issuing output 1/6 and output 1/7 simultaneously assures selection of the drive. Drive disregards output 1/7 when output 1/6 is not present.

Output 1/8

Not used.

Output 1/9

Disable read/write memory parity error stop. Allows the processor to continue execution despite a read/write memory parity error. Normally, processor halts on program parity error. Intended as a diagnostic aid only and can be used in conjunction with output 1/12 and 13.

Output 1/10

Force FMD bus parity error. Forces parity error on status data from the drive. Should set input 8/8. Intended as a diagnostic aid only.

Output 1/11

Force FMD bus parity error out. Forces parity error on tag and bus information going to the drive. Intended as a diagnostic aid only.

Output 1/12

Force program memory parity error. Forces parity error on words written in the read/write memory. Input 0/12 should set. Operation halts unless output 1/9 is set. Intended as a diagnostic aid only.

Output 1/13

Force buffer memory parity error. Forces parity error on words written into the buffer memory from either buffer control or the processor. When processor reads these words, input 0/12 sets, and the operation halts unless output 1/9 is set. When buffer control reads these words, input 1/5 sets. Intended as a diagnostic aid only.

Output 1/14

Loop 885 decode. Allows 885 drive decode information, output 8/0 to 7, to be sent back into input 8/0 to 7. Byte goes to transmitters selected by output 1/0 to 3 and loops back through matching receivers. Drives need not be cabled to access, but if a drive is cabled, drive must not be selected.

Output 1/15

Loop 885 bus. Allows 885 drive bus information, output 8/8 to 15, to be sent back into input 8/0 to 7. Same as output 1/14.

INPUT 2 - ADDRESS FIELD

Input 2/Empty

Not used.

Input 2/Full

Indicates the controller has gated data from disk into address register.

Input 2/Flag

Not used.

Input 2/0 to 15

Address field. Provide direct path to the processor for data from the disk. Processor inputs either 12- or 16-bit bytes from the shift register. Dynamic full/empty transfer control allows a block transfer of address or data field to the processor independent of buffer memory path. Intended for address field verification. Information sent to input channel 2 is not buffered. Hardware errors will not occur when processor reads data via this channel.

OUTPUT 2 - SYNC BYTE COMPARE

Output 2/Empty

Constant one.

Output 2/Full

Not used.

Output 2/Flag

Initiates error correction cycle to determine if checkword error is correctable. Before issuing this pulse, the appropriate data field length bit count must be loaded in output 4/0 to 15. Error correction cycle completes when input 0/8 clears. If input 1/11 clears, checkword is correctable.

Output 2/0 to 5

Sync byte pattern. Provides the compare byte for the sync byte search operation when reading disk. If sync byte pattern and sync byte do not compare, input 1/0 sets. Also provides 6-bit sync byte pattern during a disk write.

Output 2/6

Skip sector mark. Disables sector length violation detection, input 1/2.

Output 2/7

Write verify enable. Enables data paths during a write verify operation. Controller compares data from the buffer memory with data read from disk. A miscompare sets input 1/4. Miscompare does not terminate verify operation.

Output 2/8 to 15

Not used.

INPUT 3- ECC REGISTER STATUS

Input 3/Empty

Not used.

Input 3/Full

Constant one.

Input 3/Flag

Not used.

Input 3/0 to 15

Error correction character. Contains a parcel of the 48-bit ECC register as determined by output 3/0 and 1.

OUTPUT 3 - PARCEL DECODE

Output 3/Empty

Constant one.

Output 3/Full

Not used.

Output 3/Flag

Clears ECC register.

Output 3/0 and 1

Parcel decode. Contains a code that designates one of three 16-bit bytes from 48-bit ECC register to be read as status on input 3/0 to 15. Code definitions are as follows:

00	Lower ECC byte
01	Middle ECC byte
10	Upper ECC byte
11	Not Applicable

Output 3/2 to 15

Not used.

INPUT 4 - BIT COUNTER STATUS

Input 4/Empty

Not used.

Input 4/Full

Constant one.

Input 4/Flag

Not used.

Input 4/0 to 15

Bit counter status. Contains the contents of bit counter.

OUTPUT 4 - DISK FORMAT BIT COUNT

Output 4/Empty

Response to full. Clears the channel.

Output 4/Full

Loads bit count into channel register.

Output 4/Flag

Clears input 1/10, data parity error.

Output 4/0 to 15

Disk format bit count. Bit count and control word (output 5/0 to 15) provide the sequence control for the drives. A sequence step consists of issuing a bit count and then issuing a matching control word. Sequence stops when the bit count goes to zero. If bit count goes to zero, output 4 and output 5 are loaded if full is set. If full is not set at that time, input 1/8 sets (lost control word).

INPUT 5 - CONTROL WORD STATUS

Input 5/Empty

Not used.

Input 5/Full

Constant 1.

Input 5/Flag

Not used.

Input 5/0 to 15

Control word. Reflects state of the control word register set by output 5/0 to 15.

OUTPUT 5 - CONTROL WORD

Output 5/Empty

Response to full.

Output 5/Full

Loads control word into channel.

Output 5/Flag

Stops the control sequence after loading next control word into control word register. Flag must be present three selected clock cycles before loading a control word. Second control register load after terminate initiates new control sequence.

Output 5/0

Write sync byte. Allows 12- or 16-bit sync field to be written on disk. Lower 6 bits of sync byte are taken from NOC2/0-5. Upper bits are zero.

Output 5/1

Select 16-bit mode. When set, enables assembly/disassembly of 16-bit bytes in the shift register; when clear, enables assembly/disassembly of 12-bit bytes. 12-bit bytes are loaded/stored in bits 0 through 11 of buffer memory words.

Output 5/2

Read gate. Causes Read Gate signal to be sent to the selected drive.

Output 5/3

Write gate. Causes Write Gate signal to be sent to the selected drive.

Output 5/4

Fast start. Causes Fast Start signal to be sent to the selected 885 drive. 885 recognizes fast start only if read gate is set.

Output 5/5

Sync byte search. Enables sync byte search operation during disk read. Operation searches for the first 1 bit, then reads next 5 (885) or 6 (844-4x) bits, and finally compares last 6 bits with output 2/0 to 5. Comparison must complete before bit counter decrements to zero, or input 1/0 sets.

Output 5/6 and 7

Mark start delay decode. Causes a delay before starting bit count associated with sequence step. Bit count will not start until mark start condition is satisfied. Code definitions are as follows:

7	6	
0	0	No delay
0	1	Sector mark start
1	0	On sector mark start
1	1	Index mark start

Mark start delay can be used only to start control word sequence. Terminate or master clear must be issued between mark start delays.

Output 5/8

Enable data to buffer. Allows read data to pass through deskew registers into buffer memory on read sequence step. During write verify, bit allows read data to pass through deskew registers to be compared with buffer data. Output 5/2 (read gate) must be set to use this bit.

Output 5/9

Enable ECC feedback. Enables error correction code register feedback paths used for generation and checking of disk data field checkwords. When generating ECC, feedback paths should be enabled after writing sync byte and should be disabled before writing ECC in ECC register. When reading, feedback should be enabled after sync byte search and disabled after reading checkword.

Output 5/10

Write/read ECC. Controls data path steering when writing and reading ECC. During write, selects serial write data from ECC shift register. Prevents data from going through deskew register during reads.

Output 5/11

Invert data to/from ECC. Inverts serial data entering or leaving ECC register. Ensures a nonzero checkword for all zeros data field in 885 drives.

Output 5/12

Enable ECC shift register clock. Enables selected clock to drive ECC register.

Output 5/13 and 14

Clock selection decode. Enables one of three clocks to drive the sequence control and ECC registers. Code definitions are as follows:

14	13	
0	0	Drive write clock
0	1	Drive read clock
1	0	Processor clock
1	1	Processor clock

Output 5/15

Send inactive. Allows buffer control to send inactive to PP channel when buffer is empty.

INPUT 6 - BUFFER ADDRESS STATUS

Input 6/Empty

Not used.

Input 6/Full

Constant one.

Input 6/Flag

Not used.

Input 6/0 to 11

Buffer address. Contains address pointer selected by output 6/13 and 14. If output 6/13 and 14 are both clear, default status is read; if both are set, default status is write.

Input 6/12

Constant one. Reflects address of the buffer memory in the processor.

Input 6/13 to 15

Not used.

OUTPUT 6 - BUFFER ADDRESS LOAD

Output 6/Empty

Constant one.

Output 6/Full

Loads buffer address pointers into registers.

Output 6/Flag

Clears function, full, and active status registers in PP access selected by output 0/0 and 1.

Output 6/0 to 11

Buffer address. Contains buffer address pointers. Loaded by full if output 6/15 is set. Maximum buffer address locations is 2048 in the model A controller and 4096 in the model B controller.

Output 6/12

Not used.

Output 6/13

Read address pointer. Enables loading read address pointer into output 6/0 to 11 if output 6/15 is set. Enables reading read address pointer on input 6 when output 6/15 is clear.

Output 6/14

Write address pointer. Enables loading write address pointer into output 6/0 to 10 if output 6/15 is set. Enables reading write address pointer on input 6 when output 6/15 is clear.

Output 6/15

Load/read status. When set, enables loading address pointers into output 6, and enables up/down count into output 7. When clear, enables reading address pointer from input 6.

INPUT 7 - UP/DOWN COUNT STATUS

Input 7/Empty

Not used.

Input 7/Full

Constant one.

Input 7/Flag

Not used.

Input 7/0 to 11

Up/down count. Contains the contents of the up/down counter.

Input 7/12 to 15

Not used.

OUTPUT 7 - UP/DOWN COUNT LOAD

Output 7/Empty

Constant one.

Output 7/Full

Enables loading up/down count into register.

Output 7/Flag

Reserve. Enables connected PP access to communicate with buffer. Reserve is disabled by channel inactive, or master clear from PP or processor. Autoload also disables reserve. Processor instructions 70 through 74 do not need reserve.

Output 7/0 to 11

Up/down count. Contains quantity loaded into up/down counter. When up/down counter goes to zero, read cycles stop. Counter increments by one at end of each write cycle, and decrements by one at end of each read cycle.

Output 7/12

Not used.

Output 7/13

Disable processor to buffer. When set, prevents processor from accessing buffer memory. When clear, disables buffer memory control.

Output 7/14

PP to/from disk. When set, enables data path from connected CYBER channel to buffer and from buffer to shift register. When clear, enables data path from deskew register to buffer and from buffer to connected PP access.

Output 7/15

Maintenance loop. Enables data path from the buffer memory through the shift register and deskew register and back to the buffer memory for verification. Output 4 and output 5 control the operation. Output 7/13 enables the path only and is used only for maintenance purposes.

INPUT 8 - 885 DRIVE STATUS

Input 8/Empty

Not used.

Input 8/Full

Constant one.

Input 8/Flag

Not used.

Input 8/0 to 7

Selected echo status. Reflect the drive bus status word selected by output 8/0 to 7. If output 1/14 or 15 is set, input 8/0 to 7 reflects output 8/0 to 7 or output 8/8 to 15 (loopback).

Input 8/8

Status parity error. Indicates that the controller detected a parity error on the last status word (input 8/0 to 7) sent to the status register. Bit clears when the register contains a word with correct parity.

Input 8/9

Status valid. Indicates that contents of status register can be checked. Status parity error will not affect status valid. Remains set until next drive function sequence is initiated.

Input 8/10

On sector. Indicates that the addressed sector is under drive read/write heads. Input 8/14 sets this bit.

Input 8/11

Ready and safe. Indicates that 885 drive is safe and ready. Clear indicates that one of the following conditions has been detected.

- START switch off.
- Motor not up to speed.
- HDA sequence not complete.
- Seek time out error.
- Seek error.
- Servo off track.
- Sequence error.
- Read/write error:

  Write gate and no control select
  Head short
  Write command while in off-set
  Multihead error
  Capable enable error
  Write overrun
  Control error
  Bad write transition
  Bad write current

- Sector compare error.
- Index error.
- Decode parity error.
- Busout parity error.
- Interlock error.
- Illegal command.

When drive has cleared ready and safe, it will respond to nonmotion functions if selected, but will ignore read and write gate.

Input 8/12

Selected and reserved. Indicates drive is available and selected. Status is valid 850 ns after this bit sets.

Input 8/13

On cylinder. Indicates drive is on track. Status is valid immediately.

Input 8/14

Sector mark/on sector. Indicates start of record. Also indicates on sector condition if pulse length exceeds 300 + 100 ns. On sector sets when addressed sector is detected. Signal is gated with input 8/12.

Input 8/15

Index. A 17-ms pulse. Occurs once per revolution. Used as reference point. Gated with input 8/12.

OUTPUT 8 - 885 DRIVE FUNCTIONS

Output 8/Empty

Constant one.

Output 8/Full

Initiates function sequence in drive.

Output 8/Flag

Not used.

Output 8/0 to 7

Tag decode information.

Output 8/8 to 15

Bus information.

INPUT 9 - TRANSMITTER TESTING

Input 9/Empty

Not used.

Input 9/Full

Constant one.

Input 9/Flag

Not used.

Input 9/0 to 2

Transmitter testing. These bits are for use by diagnostics. They are used to test the write gate, read gate, and tag transmitters on the 885 interface.

Input 9/3

Not used.

Input 9/4

4-K buffer. This bit indicates the 4-K buffer memory in model B controller. This bit is not used in the model A controller.

Input 9/5 to 7

Not used.

Input 9/8 to 15

Controller number. These eight bits provide a switch selectable code for identification of the controller for maintenance purposes. Only the model B controller offers this identification code.

OUTPUT 9 - 844 DRIVE TAG LINES

Output 9/Empty

Constant 1.

Output 9/Full

Not used.

Output 9/Flag

Clear master clear status. This pulse clears the master clear status bit for the channel selected by output 0/0 and 1.

Output 9/0 to 3

Status select. Codes listed below select the appropriate status word in drive.

Code Bit 3210	Status Word
0000	Not used
0001	Read cylinder select
0010	Read difference counter
0011	Read head register
0100	Read sector counter
0101	Read sector register
0110	Read position status
0111	Read interlock status
1000	Read fault status
1001	Read control status

Output 9/4

Clear opposite channel reserve. Release reserve on drives' other access without regard for unit status. Should be used only if other channel is inoperative. When used with unit select, access to drive can be obtained if other channel has selected drive.

Output 9/5

Release. Clears reserve in selected drive. Select and Release signals may be used simultaneously.

Output 9/6

Clear fault. Clears fault flip-flop and fault register in selected drive. Clear Fault and Unit Select signals may be set simultaneously.

Output 9/7

Unit select. Selects drive determined by output 1/0 to 3, allowing communication between controller and drive. Drive has two controller accesses and can be selected by one at a time. Unit select cannot be completed if drive is busy (selected by other access) or is off-line. Drive sets input 10/12 (unit selected) following successful select. Output 1/0 to 3 (unit number) must be set before and cleared after unit select.

Output 9/8 to 15

Not used.

INPUT 10 - 844 BUS DATA AND UNSELECTED STATUS

Input 10/Empty

Not used.

Input 10/Full

Constant one.

Input 10/Flag

Not used.

Input 10/0 to 9

844 bus data. Contain drive status word selected by output 9/0 to 3.

Input 10/10

On-line. Drive ON LINE switch is ON. When bit is clear, controller should disable drive interface.

Input 10/11

Unit ready. Selected drive has completed first seek. When drive heads have unloaded and spindle motor stops, bit clears and drive will not respond to seek commands.

Input 10/12

Unit selected. Selected drive is available and its unit select bit set.

Input 10/13

Unit busy. Selected drive reserved by other channel.

Input 10/14

Seek error. Drive was unable to complete a seek within 500 ms, or drive carriage moved to a position outside the recording field. Return to zero seek command clears this bit, returns heads to cylinder zero, and enables On Cylinder signal.

Input 10/15

On sector. Sets when addressed sector is one sector from read/write heads. Stays set for one sector length, and resets each revolution until drive receives a read gate, clear, or release. Drive disables on sector while a seek command is being done.

OUTPUT 10 - 844 BUS DATA

Output 10/Empty

Constant one.

Output 10/Full

Not used.

Output 10/Flag

Not used.

Output 10/0 to 9

Address and control bus. Carry information to selected drive as determined by output 10/10 to 15.

Output 10/10

Equipment select.

Output 10/11

Control select. Designates output 10/0 to 9 as control information. Output 10/0 to 9 must be stable before and after setting this bit.

Output 10/12

Sector register load. Designates output 10/0 to 9 as sector address information.

Output 10/13

Head select. Designates output 10/0 to 9 as head address information.

Output 10/14

Cylinder select. Designates output 10/0 to 9 as cylinder address information.

Output 10/15

Difference select. Designates output 10/0 to 9 as the difference between drives' present cylinder address and new cylinder address.

INPUT 11 - CORRECTION LENGTH STATUS

Input 11/Empty

Not used.

Input 11/Full

Constant one.

Input 11/Flag

Not used.

Input 11/0 to 15

Reflect status of output 11/0 to 15.

OUTPUT 11 - CORRECTION LENGTH VECTOR

Output 11/Empty

Constant one.

Output 11/Full

Not used.

Output 11/Flag

Loads contents of output 12, 13, and 14 into 48-bit ECC register.

Output 11/0 to 15

Correction length vector. Select the burst correction length capability of the ECC logic. Output 11/0 to 7 select 885 drive correction length field. Output 11/8 to 15 select 844 drive correction length field. Correctable burst error lengths of 1 to 8 bits can be selected by loading consecutive zero bits (right-justified) to match appropriate drive field correction length.

INPUT 12, 13, AND 14 - POLYNOMIAL STATUS

Input 12, 13, 14/Empty

Not used.

Input 12, 13, 14/Full

Constant one.

Input 12, 13, 14/Flag

Not used.

Input 12/0 to 15

Polynomial status, parcel 1. Reflect status of output 12/0 to 15.

Input 13/0 to 15

Polynomial status, parcel 2. Reflect status of output 13/0 to 15.

Input 14/0 to 15

Polynomial status, parcel 3. Reflect status of output 14/0 to 15.

OUTPUT 12, 13, AND 14 - ECC POLYNOMIAL

Output 12, 13, 14/Empty

Constant one.

Output 12, 13, 14/Full

Not used.

Output 12, 13, 14/Flag

Not used.

Output 12/0 to 15

ECC polynomial, parcel 1. Lower 16 bits of the 48-bit ECC polynomial loaded into ECC register by output 11/flag during error correction. Output 12/0 goes to bit 0 of ECC register. Output 12 also serves as lower portion of 48-bit polynomial register for ECC generator/checker.

Output 13/0 to 15

ECC polynomial, parcel 2. Middle 16 bits of the 48-bit ECC polynomial loaded into ECC register by output 11/flag during error correction. Output 13/0 goes to bit 16 of ECC register. Output 13 also serves as middle portion of 48-bit polynomial register for ECC generator/checker.

Output 14/0 to 15

ECC polynomial, parcel 3. Upper 16 bits of the 48-bit ECC polynomial loaded into ECC register by output 11/flag during error correction. Output 14/0 goes to bit 32 of ECC register. Output 14 also serves as upper portion of 48-bit polynomial register for ECC generator/checker.

INPUT 15 - NOT USED

OUTPUT 15 - NOT USED

INPUT 16 - SPECIAL CHANNEL (PP INPUT)

Input 16/Empty

Response to full.

Input 16/Full

Identifies data on channel.

Input 16/Flag

Set by inactive or output 16/flag; cleared by active. 64 and 65 jump instructions monitor this flag status.

Input 16/0 to 11

PP data. Carries 12-bit words from peripheral processor.

Input 16/12 to 15

Not used.

OUTPUT 16 - SPECIAL CHANNEL (PP OUTPUT)

Output 16/Empty

Response to full.

Output 16/Full

Identifies data on channel.

Output 16/Flag

Acts as Inactive signal sent to PP. Controller resynchronizes pulse with channel clock. If issued when a function is present, it clears function status (input 0/1) and causes empty to be sent to PP in response to function. If issued after 72 or 73 instruction, results in setting input 16/flag, disconnecting PP channel.

Output 16/0 to 11

PP data. Carries 12-bit words to peripheral processor.

Output 16/12 to 15

Not used.

NOTE

Output 16/12 to 15 bits do enter into parity generation and should be set to zero if correct parity is to be transmitted with the 12-bit PP data word.

FUNCTIONAL DESCRIPTION

PP INTERFACE

This section of the controller consists of the paks at A01, A02, A03, A04, and A08 in the model A controller and paks A01, A02, A03, A04, A07 and A08 in the model B controller. It does the following:

- Receives and transmits all information passing between the controller and PP.
- Synchronizes the controller with the PP.
- Connects and reserves the controller to a PP.
- Checks/generates PP channel parity.
- Checks for an autoload function.
- Performs channel deadman timeout.

PROCESSOR

This section of the controller consists of paks at A16 through A27. The central part of the processor is located at A23, A24, A25, and A26 in the model A controller and at A24 and A26 in the model B controller. These paks contain the 10800 and 10803 microprocessor chips, the buffer memory, and the program RAM. Other parts of the processor are the control memory at A22, the program ROM at A27, and the processor I/O channels at A16 through A20.

Figure 4-2 illustrates the processor organization. The processor registers and buses are explained below.

Register Definitions

A (Accumulator) Register

A 16-bit register on the 10800, clocked every 85 ns at t00. Receives data from the shift register or the I bus. Sends data to ALU (10803), I bus, O bus, and shift register.

PC (Program Counter) Register

A 16-bit register on the 10803, stores the next program address. Clocked by t00 and enabled by t42. Addressed during some 10803 register file operations.

R1 (Scratch) Register

A 16-bit register on the 10803 is used as a scratch or backup register. When addressed, is clocked by t00 and enabled by t42.

DR (Data) Register

A 16-bit register on the 10803 used for data transfer and address calculations. Clocked by t00 and enabled by t42.

AR (Address) Register

A 16-bit register on the 10803 used to process memory addresses. When selected, is clocked by t00 and enabled by t42.

R2, R3 Registers

A 16-bit register on the 10803 used to form a pushdown stack to implement the return jump to ROM instruction. R2 is the top of the stack. When addressed, t00 clocks R2 and R3.

CMA (Control Memory Address) Register

An 8-bit register at chassis location A22 holds the next control memory address. Clocked at t42.

CMR (Control Memory) Register

A 47-bit register at chassis location A22 that holds the control bits read from control memory. Clocked by t00.

r (Resync) Register

A 3-bit register at chassis location A22 that holds processor channel status - output full, input full, and inactive. Clocked by t42.

b Register

A 4-bit register at chassis location A27 that holds the b field of a 76 or 77 instruction. b field holds the decode of a bit location on an input channel for a 76 or 77 instruction. Clocking occurs during each RNI cycle.

c Register

A 5-bit register at chassis location A21 holds the number of the selected processor channel. Clocking occurs during an RNI cycle when a 6x or 7x instruction has been decoded.

ZD Register

A 1-bit register on the 10803 holds the ALU zero detect status for the preceding cycle. t00 clocks register.

Processor Buses

I Bus

A 16-bit bidirectional bus connects the 10800, 10803, buffer memory write path, A bus, and program RAM.

O Bus

A 16-bit bidirectional bus connects the 10800, 10803, and memory.

A Bus

A 16-bit bus carrying data from the I bus into the 10800 only. Provides a second operand input.

D Bus

A 16-bit bidirectional bus connecting the 10803 with the processor channels.

Processor Sync Bit

Bit 15 of the 16-bit instruction word is used only to provide an oscilloscope sync point for maintenance purposes. The bit can be set from the console and monitored at the pak at A27, testpoint 50.

Instruction Deadman Timeout

Execution of a 70, 71, 72, or 73 instruction enables the instruction deadman timer at location A22. If a full or empty is not generated on processor channels 0 through 14 for 30 ms (+10%), the timer expires. Timeout limits the processor channels to one word inputs and sets NIC1/9. Master clear clears this condition.

Instruction Sequence

Figure 4-2 illustrates the processor and the various fields of the 60-bit control memory word. The following sequence gives some indication of how the elements of the processor relate during execution of an instruction.

Instruction 16d (Add d):

1. f (operation code) part of instruction (RAM data 9-14) is sent from the RAM to the control memory address multiplexer. This code contains the quantity 16_8, and selects control memory address 16_8.

2. Control memory sets appropriate bits in the 10803 control field. (Other bits are not significant in this cycle.) DR (data) register in 10803 puts its contents on the I bus.

3. Next address is 125_8; control memory sets bits in 10800 and 10803 control field. The data put on the I bus from the 10803 DR register is added to the contents of the A (accumulator) register in the 10800.

4. Next address is 377_8. 10803 control bits, pointer control, and several miscellaneous control bits are all set by control memory. Program counter is incremented by one. Instruction sequence complete. RAM does an RNI.

DATA PATH CONTROL

This section of the controller consists of the paks at locations A15, B19, B20, B21, and B22. This hardware controls data transfers between the buffer memory and the disk interface. It does the following:

- Executes control word operations. The control word is sent by the processor on normal output channel 5.
- Assembles 12- or 16-bit bytes from serial disk data during a disk read.
- Disassembles 12- or 16-bit byte into serial disk data during a disk write.
- Controls data transfers into and out of the buffer.
- Generates controller clock pulses. The control word selects one of three clock signals - processor clock, drive read clock, or drive write clock - for use by sequence control and the error correction circuitry.
- Checks parity on data read from the buffer.
- Checks for the sync byte during disk read operations.

DISK INTERFACE

The FMD interface consists of paks at locations B01 through B04. These paks communicate with FMD spindles 0 through 7. The Four FMD Option, located at paks B14 through B17, adds the interface for FMD 8 through 15.

The 844 Drive Option, located at B05 through B12, provides the interface for eight 844 disk storage units. The pak at location B13 provides for control of the 844 drive interface.

CONTROLLER CLOCKS

The controller uses the following clock signals to synchronize and control its operations.

10MHz PP Clock

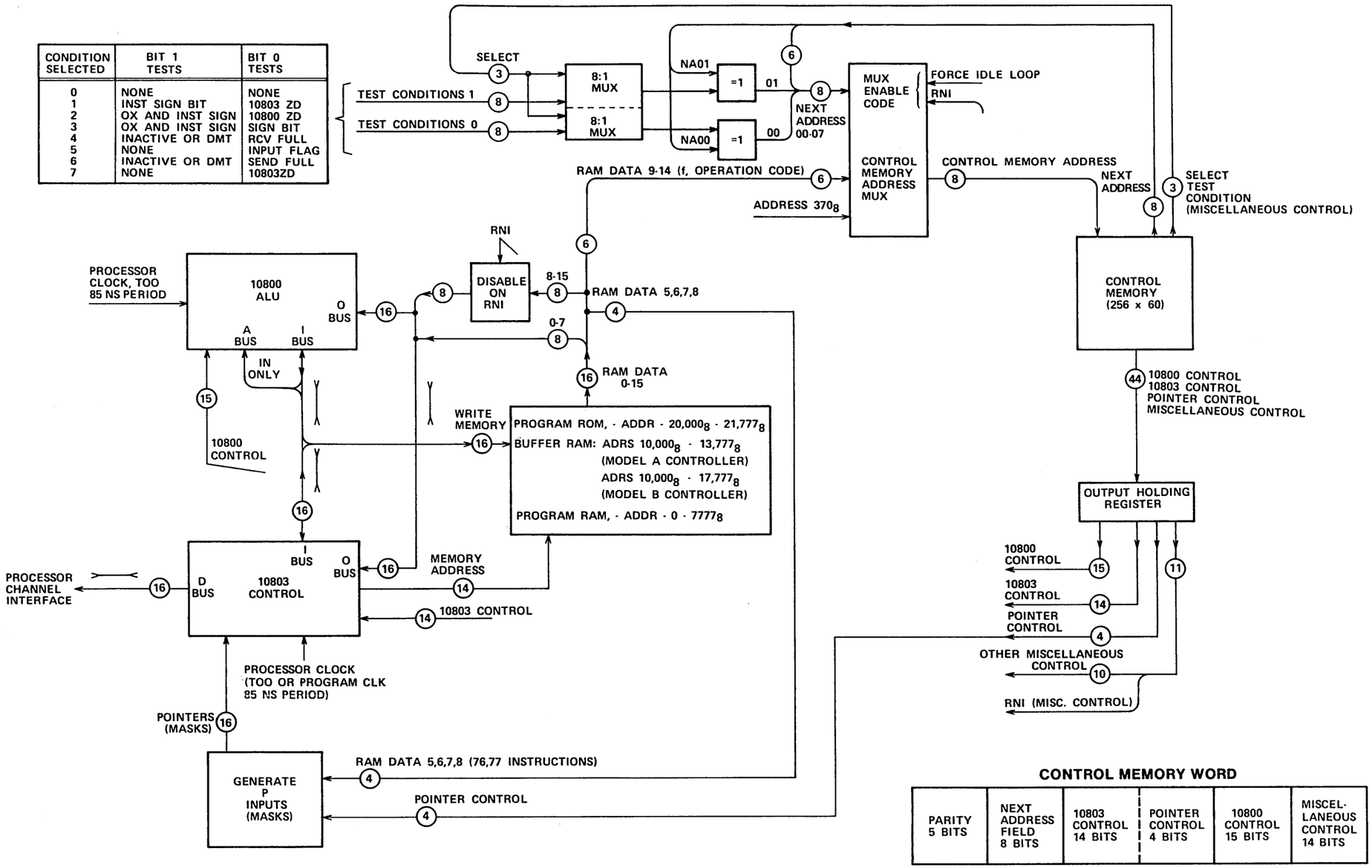
This signal from the PP is used to synchronize the controller and PP during function operations and data transfer operations. Several internal clock pulses derived from 10-MHz clock are used in the controller PP interface. Section 3 of this manual has a procedure to tune this clock signal in the controller.

Program Clock

This bit in the control memory word is used in the 10803 chip.

The following clocks provide timing pulses throughout data path control and error correction circuitry. One of the three is selected by a code in the control word (N0C5/13, 14).

CONDITION SELECTED	BIT 1 TESTS	BIT 0 TESTS
0	NONE	NONE
1	INST SIGN BIT	10803 ZD
2	OX AND INST SIGN	10800 ZD
3	OX AND INST SIGN	SIGN BIT
4	INACTIVE OR DMT	RCV FULL
5	NONE	INPUT FLAG
6	INACTIVE OR DMT	SEND FULL
7	NONE	10803ZD



CONTROL MEMORY WORD

PARITY 5 BITS	NEXT ADDRESS FIELD 8 BITS	10803 CONTROL 14 BITS	POINTER CONTROL 4 BITS	10800 CONTROL 15 BITS	MISCEL-LANEOUS CONTROL 14 BITS

Figure 4-2. Processor Organization

Processor Clock

This consists of 21-ns pulses occurring at t00 and t42 and having an 85-ns clock period. These pulses are generated by a circuit at location A22.

885 Read or Write Clock

The write clock is derived from the 9.6-MHz clock signal that the drive sends to the controller. Read clock is sent to the controller by the drive during a disk read operation. Both have a 104-ns period.

844 Read or Write Clock

These clock pulses are sent to the controller by the drive unit. Both read and write clocks have a 144-ns clock period.

CONTROLLER PARITY

The controller generates and checks parity in several places. Odd parity is correct parity in every case.

ROM Parity

A parity bit accompanies each byte read from the program ROM. An error sets NIC0/12, lights the ROM P.E. LED at A27, and stops the processor.

RAM Parity

A parity bit accompanies each byte read from the program RAM and buffer RAM. An error sets NIC0/12, lights the RAM P.E. LED at A27, and stops the processor if NOC1/9 (disable stop) is not set.

Buffer Memory Output Register Parity

A parity bit accompanies each byte from the buffer as it goes through the output register at B19 and B20. Parity is checked on all bytes sent out of the output register. An error sets NIC1/5.

Channel Parity

All data bytes transferred between the controller and a CDC CYBER 170 PP have a parity bit accompanying them. 6000 and CDC CYBER 70 PP do not use parity. The 60-pak at location A08 has four switches, one for each channel access, that enable or disable the parity circuits in the controller. Each switch must be set to the position appropriate to the type of PP connected to the access.

Bytes sent to the controller from the PP can be checked for parity in either of two places depending upon the situation. Data passing through the data multiplexer at A08 comes from a connected PP. Data coming out of the data multiplexer is checked for parity errors. An error lights the parity error LED on A08 and sets NIC1/10, channel parity error bit.

Data passing through the NIC select multiplexer on A08 comes from the PP access selected by NOC0/0, 1. This is usually special channel information and the PP may not be connected. Data coming out of this multiplexer is checked for parity errors. An error sets NIC0/2.

Status Parity Error

Bus in data from the 885 drives is checked for parity errors at location B04. An error sets NIC8/8.

BUFFER MEMORY

The buffer RAM is the center of all block transfers between the PP and the disks. Figure 4-3 shows the relationship of the buffer to its controlling hardware elements. The six data paths that use the buffer are explained below.

- PP to Buffer

  12-bit bytes are sent by the connected PP. These bytes go through a 4:1 multiplexer and two 2:1 multiplexers and are sent to the buffer on the path labeled external write data on figure 4-3. The upper 4 bits are zero filled.

- Disk to Buffer

  Serial data from a disk is assembled in the shift register into 12-bit bytes. The upper 4 bits are zero filled. These bytes are sent through the deskew register and two 2:1 multiplexers into the buffer.

- Processor to Buffer

  The I bus from the 10800 and 10803 chips in the processor can send 16-bit bytes to the buffer. This allows the processor to use the buffer as an extension of program RAM.

- Buffer to PP

  The buffer sends 16-bit bytes to the output register. The upper 4 bits are zero filled. Data from the output register is sent to the PP interface in the controller.

- Buffer to Disk

  The buffer sends 16-bit bytes through the output register to the shift register. The shift register sends serial data to the disk interface in the controller.

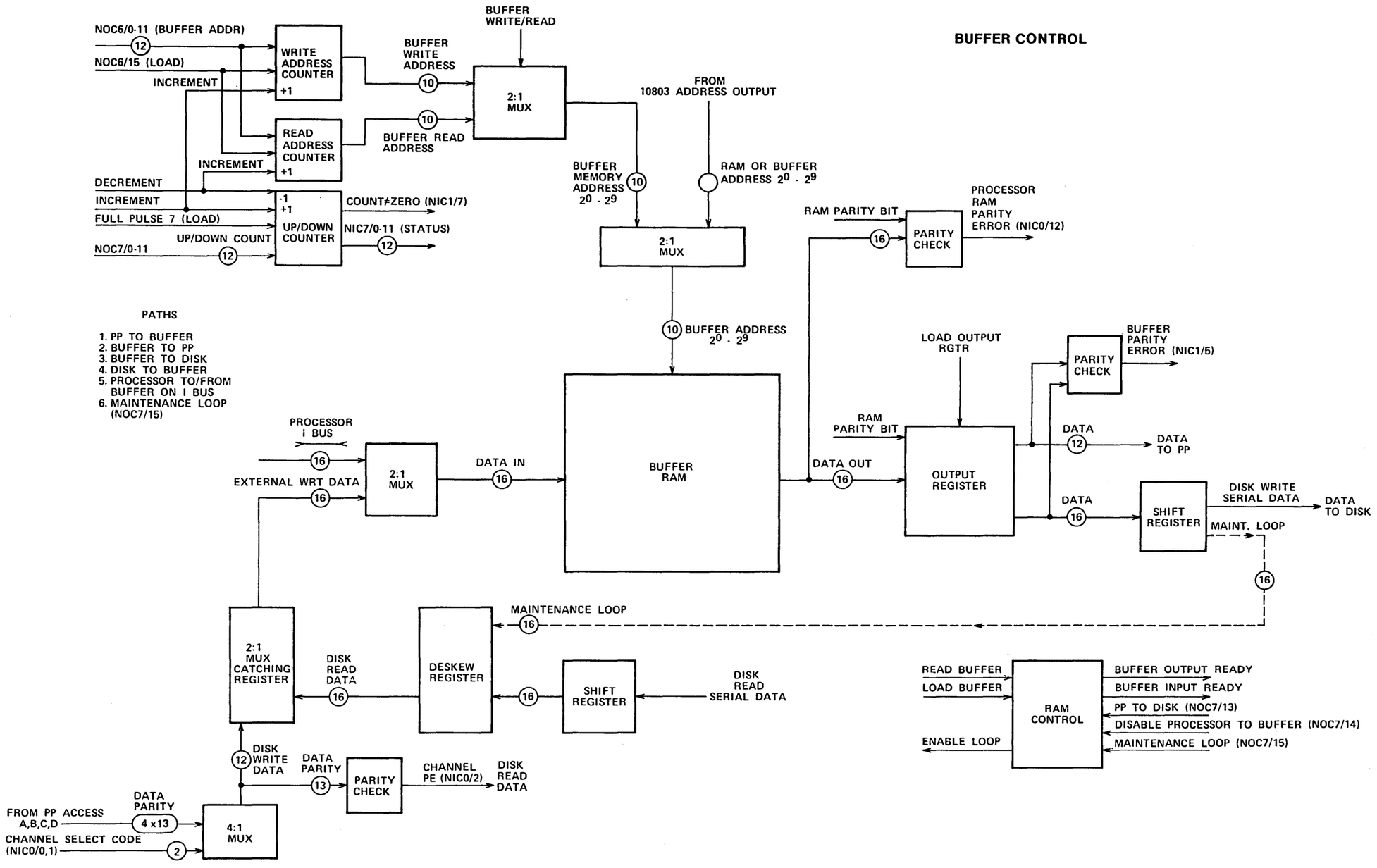


Figure 4-3. Buffer Control

- Maintenance Loop

  The processor can use this maintenance feature to check the accuracy of the data path hardware. Setting NOC7/15 enables the data path from the buffer to the output register, shift register, deskew register, catching register, and buffer input multiplexer. The processor, using the control word to control the transfer, sends 16-bit bytes from the buffer through the maintenance loop data path back into the buffer. The buffer output data is then compared with the input data.

Buffer Addressing

The processor loads the write address counter and read address counter from NOC6/0-10. NOC6/15 gates the quantity into the counters. Every time a byte is written into the buffer, the write address counter increments by one. Every time a byte is read from the buffer, the read address counter increments by one. Read and write addresses from the counters are alternately gated through a multiplexer to address buffer memory.

The up/down counter is loaded from NOC7/0-11 before the start of a buffer operation. This counter increments by one when a byte is written into the buffer and decrements by one when a byte is read from the buffer. The processor can determine the amount of data in the buffer by reading the up/down count status (NIC7/0-11). If the counter decrements to zero, the buffer read terminates.

The buffer address can also be sent by the 10803 when the buffer is being used as an extension of the program RAM.

RAM Control Signals

To use the buffer, the processor must establish a few conditions before starting an operation. First, in a PP/buffer operation the PP to Disk signal (NOC7/13) must be set or cleared to enable a transfer either to or from a disk. Second, during a buffered block transfer between a PP and disk, NOC7/13 should be set to disable processor access to the buffer.

The input and output to the buffer is done with ready/resume type of control. When the buffer can output a word, the Buffer Output Ready signal indicates this. When the word has been sent to the output register, the Read Buffer signal indicates this.

When the buffer can accept a byte, the Buffer Input Ready signal indicates this. When a byte is ready for input the Load Buffer signal indicates this.

OPERATIONAL DESCRIPTION

CONNECT/RESERVE

A PP access can connect and reserve the controller if the controller is not connected. A PP connects the controller by sending any function. The scanner, running off the microprocessor clock, enables the connect and prevents ties if the controller receives PP functions simultaneously from different PP accesses. NOC0 flag pulse or an autoload from the connected channel clears the connect condition.

Connect lights the appropriate LED on the pak at A08, and sets bit 0 of processor input channel 0.

CHANNEL DEADMAN TIMEOUT

The controller has a timer at location A08 to deactivate the PP channel if the channel is idle for 4.5 $\pm$1.5 s. The timer is enabled when the PP activates the channel. Any Full, Empty, or Inactive signal on the channel resets the timer.

Deadman timeout causes the controller to send an inactive signal to the PP channel, sets NIC0/4, and lights an LED at location A08.

AUTOLOAD

Initial start up conditions can be established in the controller by sending a 0414_8 (autoload from PP) function or a $01xx_8$ (autoload from disk) function. The controller decodes these functions at location A08, master clears the hardware, and executes the autoload routine that starts at location $20\ 000_8$ of processor memory (program ROM).

MASTER CLEAR

The controller can be cleared in several ways. Table 4-4 shows the effect of each method. In addition to the methods shown on the table, processor flag pulses 0, 1, 4, and 6 clear connect, controller hardware, controller hardware (excluding processor output channels), and selected CDC CYBER interface respectively.

Table 4-4. Effects of Master Clear

Master Clear \ Method	Clear Controller Hardware Logic	Force Processor to Memory Location $20\ 000_8$	Clear Connect	Clear Selected CDC CYBER Interface	Send PP Inactive
Button Power On MC	Yes	Yes	Yes	Yes	No
Deadstart MC (Accepted only from connected access)	Yes	Yes	Yes	Yes	No
Deadstart MC (No access connected)	Yes	Yes	N/A	Yes	No
Deadstart MC (Another access connected)	No	No	No	Yes	No
Autoload (From connected access)	Yes	Yes	No	No	No
Channel Deadman Timeout	No	No	No	No	Yes

CONTROL WORD EXECUTION

The control word sent by the processor from NOC5, and its associated bit count sent from NOC4, control hardware sequences in the controller and drives. A sequence has the following steps.

1. Processor sends a bit count to the bit counter (at B19 and B20).
2. Processor sends the control word to the control word register (at B19 and B20).
3. Processor clock decrements bit counter to zero. This completes the sequence and enables another sequence to begin. The bit count and control word are loaded without any interruption if the NOC4 full and NOC5 full are set, and output flag 5 is not set. If all of these signals are not set, NIC1/8, lost control word, sets.

To terminate the control word sequence, the processor sets output flag 5. The sequence does not terminate until the bit counter decrements to zero. To terminate the sequence properly output flag 5 should be set after the bit count has been loaded. This prevents termination before the final sequence has begun. Figure 4-4 illustrates the relationship of control word elements.

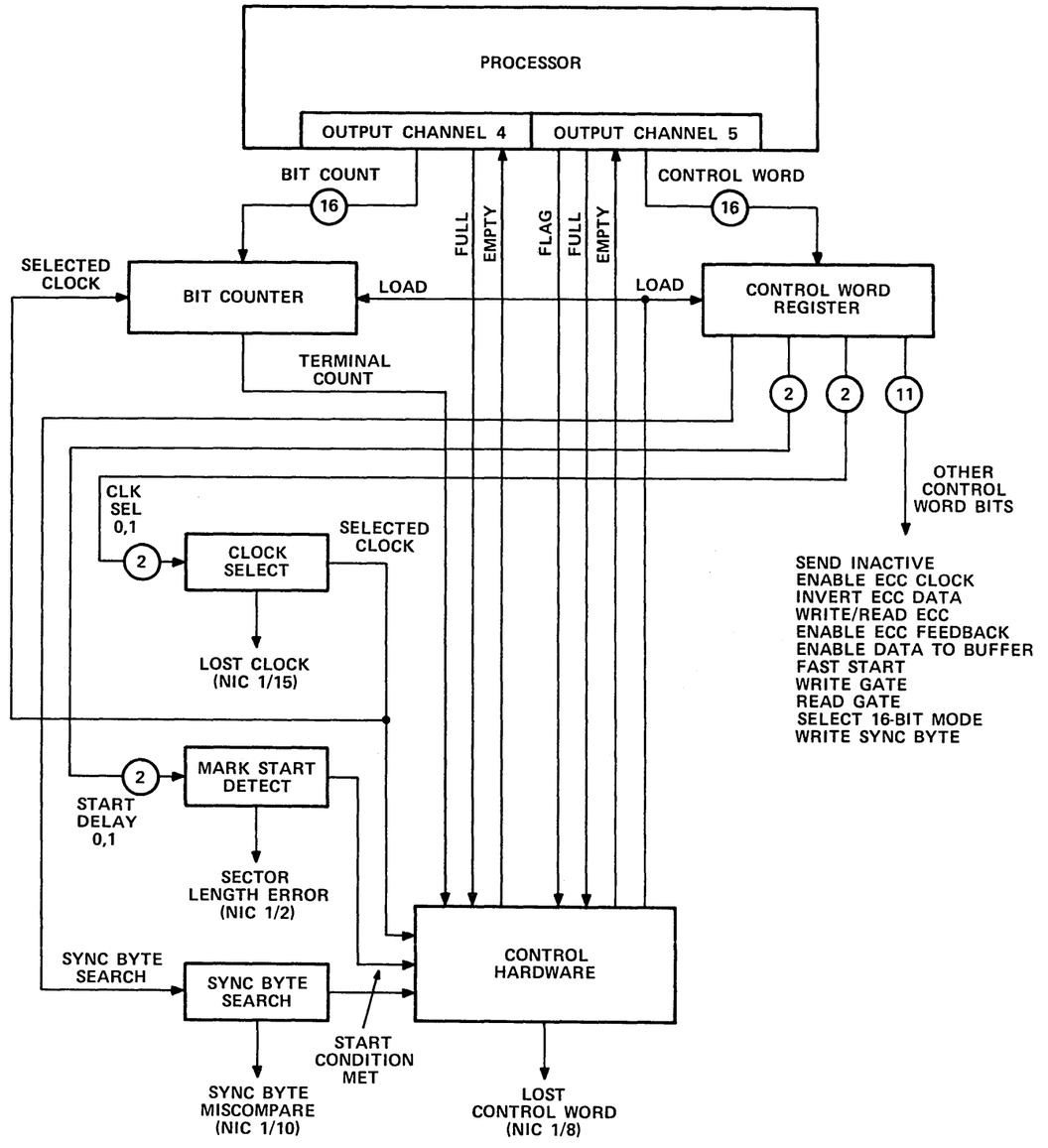


Figure 4-4. Controlword Elements

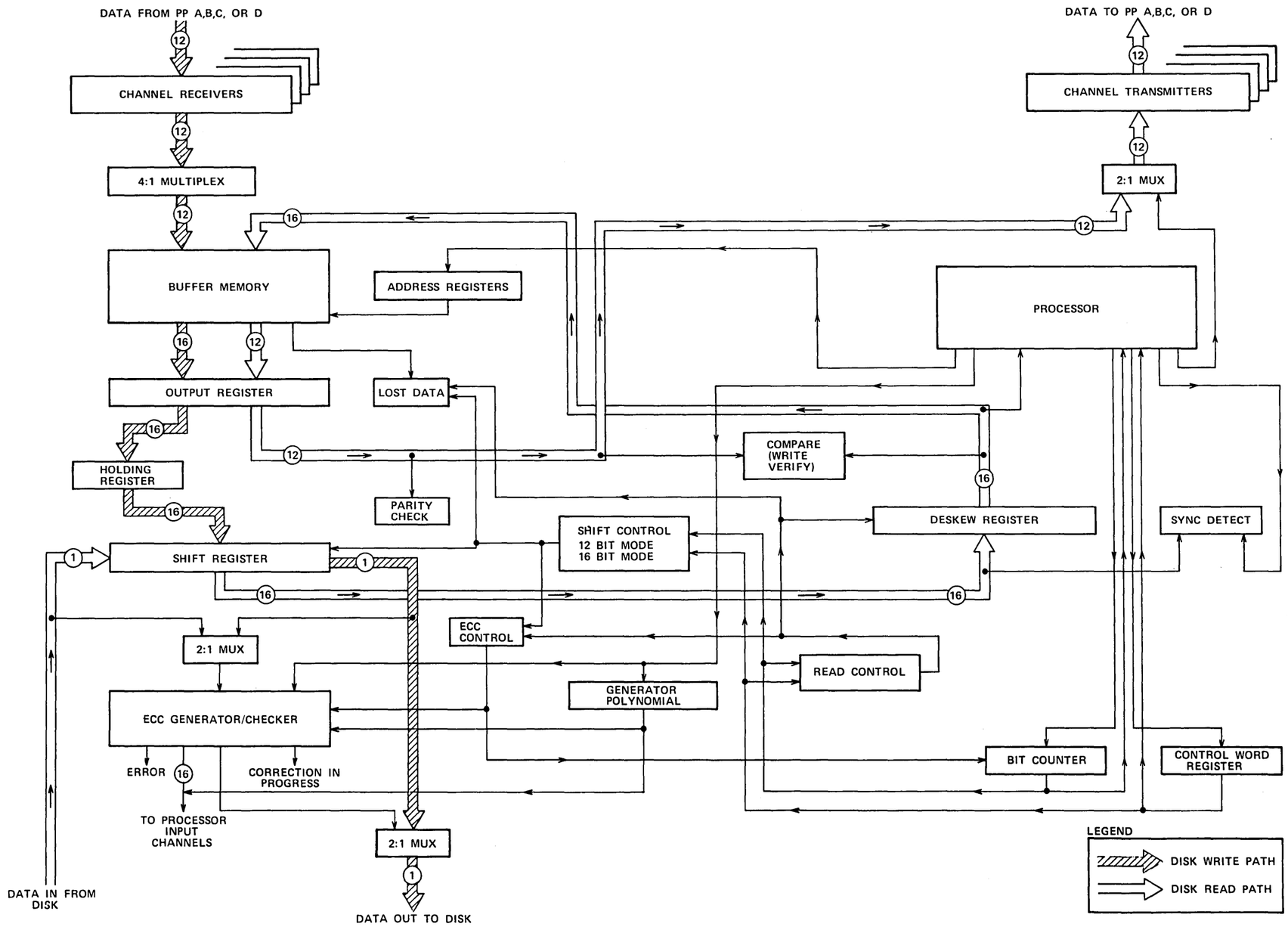


Figure 4-5. Controller Data Paths

READ/WRITE

A write operation transfers a block of data from a PP I/O channel to a disk. A read operation transfers a block of data from a disk to a PP.

The processor, using the control word, starts read and write operations in the controller. After a control word sequence has begun the processor does not intervene. Hardware controls the sequence. Figure 4-5 shows the read and write data paths and related hardware elements in the controller.

A block read and a block write transfer data through the buffer memory in exactly the same way. The buffer read and write cycles alternate every 85 ns.

The shift register assembles 12 or 16-bit bytes from serial data during a read, and disassembles 12 or 16-bit bytes into serial data during a write. Setting NOC5/1 selects 16-bit mode; clearing it selects 12-bit mode.

The read data paths shown on the figure are 16 bits wide from the shift register through the deskew register to the buffer memory. However, in 12-bit mode, the controller fills the upper four bits of these bytes with zeros.

Lost data occurs if the buffer does not send data to the shift register fast enough during a write or does not accept data fast enough from the deskew register during a read. Lost data sets NIC1/1.

The processor initiates a write verify operation by setting NOC2/7. During a write verify operation, data sent from the PP is compared with data read from a disk.

CHECKWORD GENERATION/ERROR CORRECTION

The controller can detect and correct most data errors with the checkword generator at A12. The generator provides an error correction character (ECC) that is written on the disk at the end of the data field. The 844 ECC is 32 bits long and the 885 ECC is 48 bits long.

To generate the ECC, all serial write data bits are sent into the shift register at A12. As the data field is shifted through the register, an exclusive OR is performed with the input to each stage of the register and bits of the error correction polynomial. The processor sends a 32-bit polynomial from NOC13 and 14 during an 844 write operation and a 48-bit polynomial from NOC12, 13, and 14 during an 885 write operation. At the end of the write data field, the ECC character is written on the disk.

During the read, the operation is repeated. Read data, including the ECC, is sent through the shift register and an exclusive OR is performed with the polynomial. If the content of the register equals zero at the end of the read, then the circuit did not detect an error.

If the register does not equal zero at the end of the operation, then the controller must determine whether the error is correctable. One error burst of 8 bits or less is correctable.

To determine whether the error is correctable, the processor reads the contents of the shift register from NIC3, reverses the order of the bytes, and sends the 48- or 32-bit word back to the shift register on NOC12, 13, and 14. Then the processor puts the decode polynomial on NOC12, 13, and 14 which is used to perform an exclusive OR with the shift register bits as the bits shift. The register shifts the number times equal to the number of bits in the data field plus the number of bits in the ECC. If, during the shift, the contents of the shift register becomes zero, then the error is correctable. If the error is not correctable, then NIC1/11 sets, and the operation terminates.

To correct an error, the processor must determine the buffer address of the error by checking bit count status (NIC4). Bit count indicates the number of times the register shifted to get a zero quantity. The processor then sets the correction vector (NOC11) and performs an exclusive OR with the correction vector and buffer data beginning at the address indicated by NIC4.

MAINTENANCE AIDS

The controller contains several features to help isolate problems in the hardware. These features are explained below.

Processor Instruction Sync Point

The upper order bit (bit 15) of all instruction words is unused. This bit can be set from the system console and monitored from TP50 at chassis location A27.

Maintenance Loop

The buffer memory data paths can be checked by sending data from the buffer on the write path and reading back in on the read path (figure 4-3). This is done by setting the maintenance loop bit NOC7/15.

Echo Check

The data from the processor output channels can be looped back and read on the processor input channels. This occurs during a 76 or 77 instruction when the control memory word sets the -JSM bit.

Force Parity Errors

Four parity conditions can be forced to incorrect parity by setting the appropriate processor channel bit. The bit and error are listed below.

NOC1/10 - 885 status word

NOC1/11 - 885 busout word

NOC1/12 - Program RAM word

NOC1/13 - Buffer RAM word

885 Interface Loop

NOC1/14 gates 885 drive decode information from NOC8/0-7 back into NIC8/0-7. NOC0/15 gates 885 busout information from NOC8/8-15 back into NIC8/8-15.

LIGHT EMITTING DIODES (LEDS)

Figures 4-6 and 4-7 identify the LEDs in row A of the model A and model B logic chassis, respectively. LED descriptions are as follows.

CONNECTED PP CHANNEL A, B, C, D

Indicate which PP channel is connected in the controller hardware.

AUTOLOAD

Indicates that the connected PP has sent an autoload function. A master clear or another function clears the LED.

DEADMAN TIMER

Indicates that a CDC CYBER channel timeout occurred.

PP CHANNEL DATA PARITY ERROR

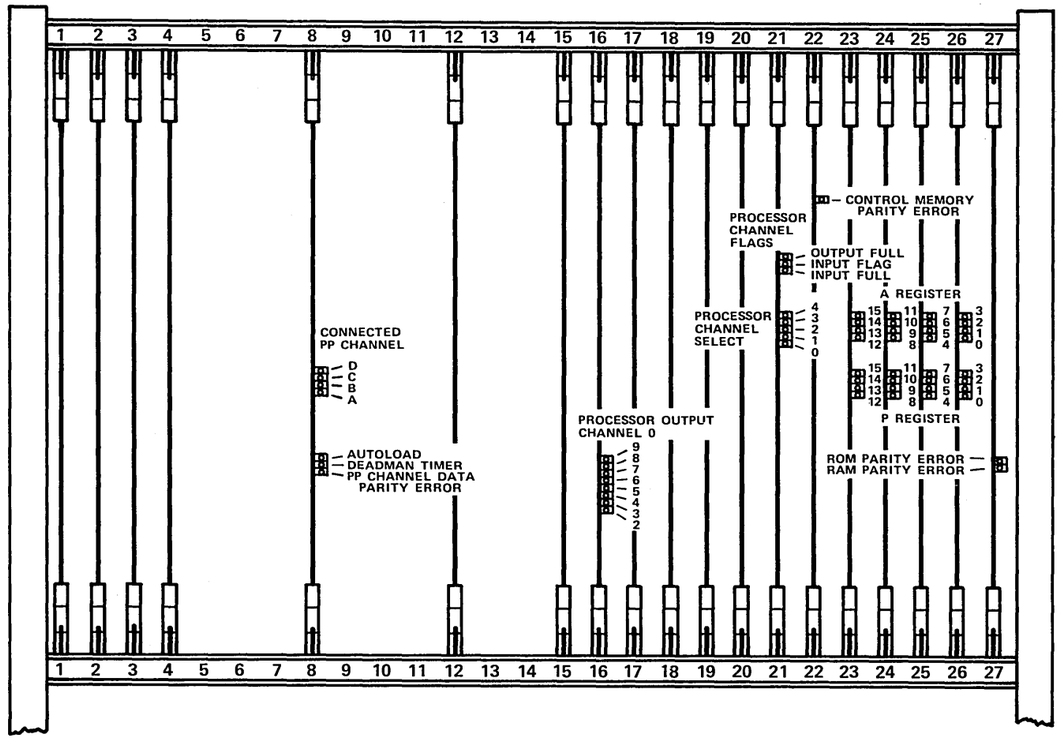
Indicates that the controller detected a parity error (even parity) on a word sent by the connected PP. Parity must be enabled to light this indicator.

PROCESSOR OUTPUT CHANNEL 0, 2 THROUGH 9

Reflect the contents of NOC0/2-9. When lit, they indicate that the controller is in the idle loop and is probably operating properly. If all are not lit, the processor has probably halted and may have a failure.

OUTPUT FULL, INPUT FLAG, INPUT FULL

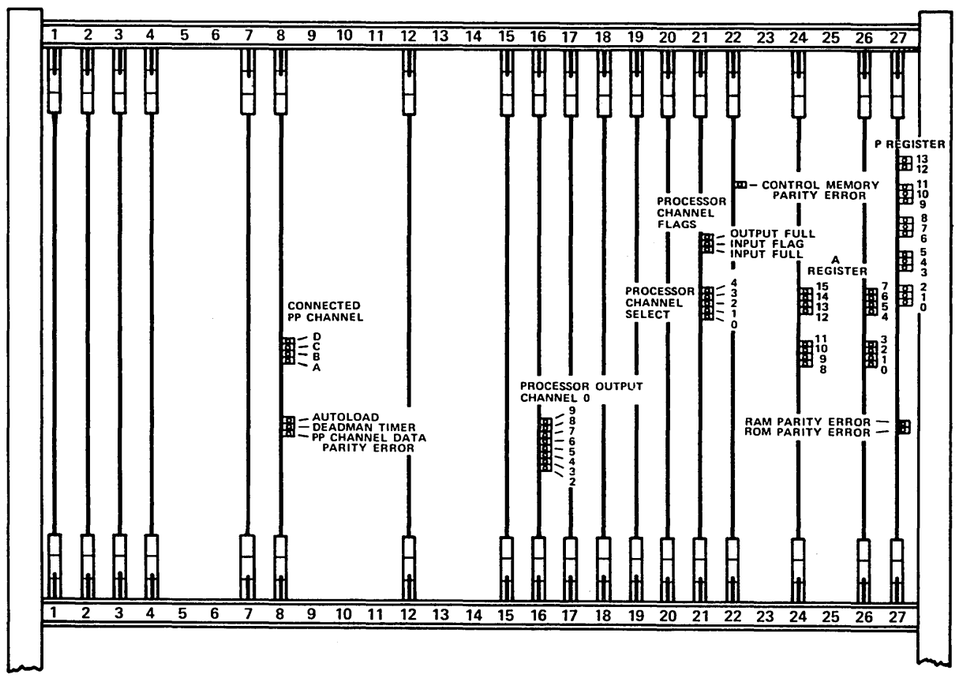
Indicate that the Output Full, Input Flag, or Input Full signal is present on the selected processor channel.


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
CONNECTED PP CHANNEL
D
C
B
A
AUTOLOAD
DEADMAN TIMER
PP CHANNEL DATA PARITY ERROR
PROCESSOR OUTPUT CHANNEL 0
9 8 7 6 5 4 3 2
PROCESSOR CHANNEL SELECT
4 3 2 1 0
PROCESSOR CHANNEL FLAGS
OUTPUT FULL
INPUT FLAG
INPUT FULL
CONTROL MEMORY PARITY ERROR
A REGISTER
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
P REGISTER
ROM PARITY ERROR
RAM PARITY ERROR

NOTES:

1. LED ON INDICATES 1, LED OFF INDICATES 0.
2. A NUMBER NEXT TO A LED INDICATES THE POWER OF 2 REPRESENTED BY THE LED.

Figure 4-6. LED Locations, Model A Controller


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
P REGISTER
CONTROL MEMORY PARITY ERROR
PROCESSOR CHANNEL FLAGS
OUTPUT FULL
INPUT FLAG
INPUT FULL
A REGISTER
PROCESSOR CHANNEL SELECT
CONNECTED PP CHANNEL
D C B A
PROCESSOR OUTPUT CHANNEL 0
AUTOLOAD
DEADMAN TIMER
PP CHANNEL DATA PARITY ERROR
RAM PARITY ERROR
ROM PARITY ERROR

NOTES:

1. LED ON INDICATES 1, LED OFF INDICATES 0.
2. A NUMBER NEXT TO A LED INDICATES THE POWER OF 2 REPRESENTED BY THE LED.

Figure 4-7. LED Locations, Model B Controller

PROCESSOR CHANNEL SELECT 0, 1, 2, 3, 4

Indicate which channel has been selected by the processor. The number of the selected channel, 0 through 16, corresponds to the octal code shown by the indicators.

CONTROL MEMORY PARITY ERROR

Indicates a parity error (even parity) was detected in one or more of the 12-bit bytes of the 60-bit word. Master clear clears this condition.

A REGISTER

Indicates the contents of the accumulator register during a halt instruction.

P REGISTER

Indicates the current program address in the processor.

ROM PARITY ERROR, RAM PARITY ERROR

Indicate that the processor has halted because of a parity error (even parity) in a word read from the program ROM, program RAM, or buffer RAM.

INTRODUCTION

This section contains the following information.

- Primary block diagram (PBD), 1.0
- Secondary block diagrams (SBD), 2.0, 2.1
- Interconnection block diagrams (IBD), 3.0, 3.1, 3.2, 3.3
- Consolidated logic diagrams (CLD)
- Chassis map
- Logic diagrams
- Power distribution diagrams

The PBD shows the relationship between major functional components. The SBD shows data paths and some control signals. The IBD shows all 60-paks and all signal lines between paks. CLDs show the logic on a single pak type using ANSI conventions. CLDs show all signals going into and out of a pak.

Where possible, one logic diagram set and one CLD are included for each 60-pak type, regardless of the number used in the controller. If necessary, more logic diagram sets and CLDs have been added to make the diagrams more easily understood.

A two-letter pak identifier has been assigned to each 60-pak type. This pak identifier appears on the logic diagram, CLD, and wherever the pak appears on the block diagrams. Block diagrams also contain the title of the pak, chassis location, and a page reference to the next lower level block diagram where the pak can be found. Figure 5-1 shows block diagram conventions.

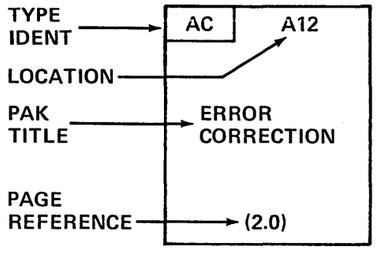
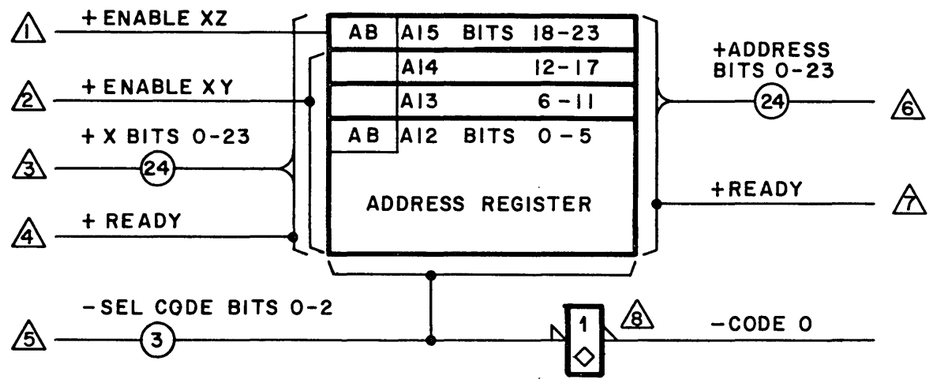


Figure 5-1. Block Diagram Conventions

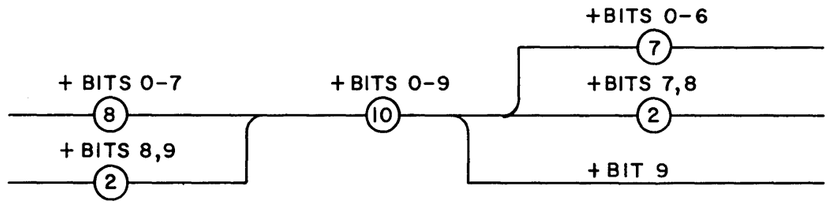
BLOCK DIAGRAM I/O CONVENTIONS

Figure 5-2 illustrates identical paks performing the same functions that are stacked on block diagrams. Figures 5-2 and 5-3 show how signals are distributed on a block diagram.

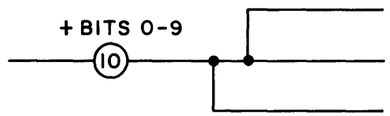


1. Input to pak at A15
2. Input to paks at A12, A13, A14
3. Input distributed to paks as shown in pak enclosures
4. Input fanned out to all paks
5. Input fanned out to all paks (same three bits go to each pak)
6. Output merged from paks as shown in pak enclosures
7. Output is same unique signal from each pak (logical rather than electrical)
8. Indicates a backpanel wired function

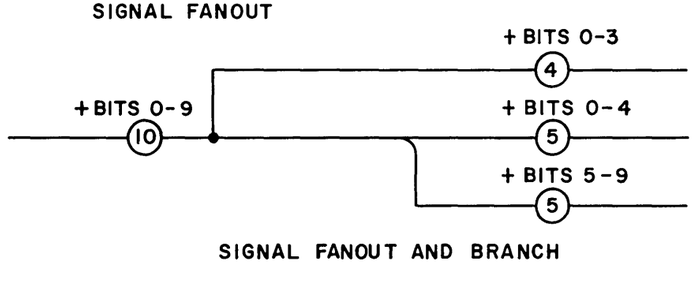
Figure 5-2. Stacking Conventions



SIGNAL MERGE AND BRANCH



SIGNAL FANOUT



SIGNAL FANOUT AND BRANCH

Figure 5-3. Branch, Merge, Fanout Conventions

CLD AND LOGIC DIAGRAMS

These diagrams use ANSI symbology. The ECL 10,000 Series Microcircuits manual and CDC Microcircuits Handbook (preface) explain the symbols used in CLDs and logic diagrams.

CLDs show all signals going into and out of a 60-pak. The circuits shown on a CLD are summarized and, if possible, chip type is shown. This is not possible where several chips are combined. The symbols contain a page number in parentheses that indicates the page of the logic diagram on which the circuit appears.

All CLDs and logic diagrams are organized in alphabetical order according to the pak identifier.

MODEL A

BLOCK DIAGRAMS

PRIMARY BLOCK DIAGRAM 1.0

This diagram shows all 60-paks in the controller including the options.

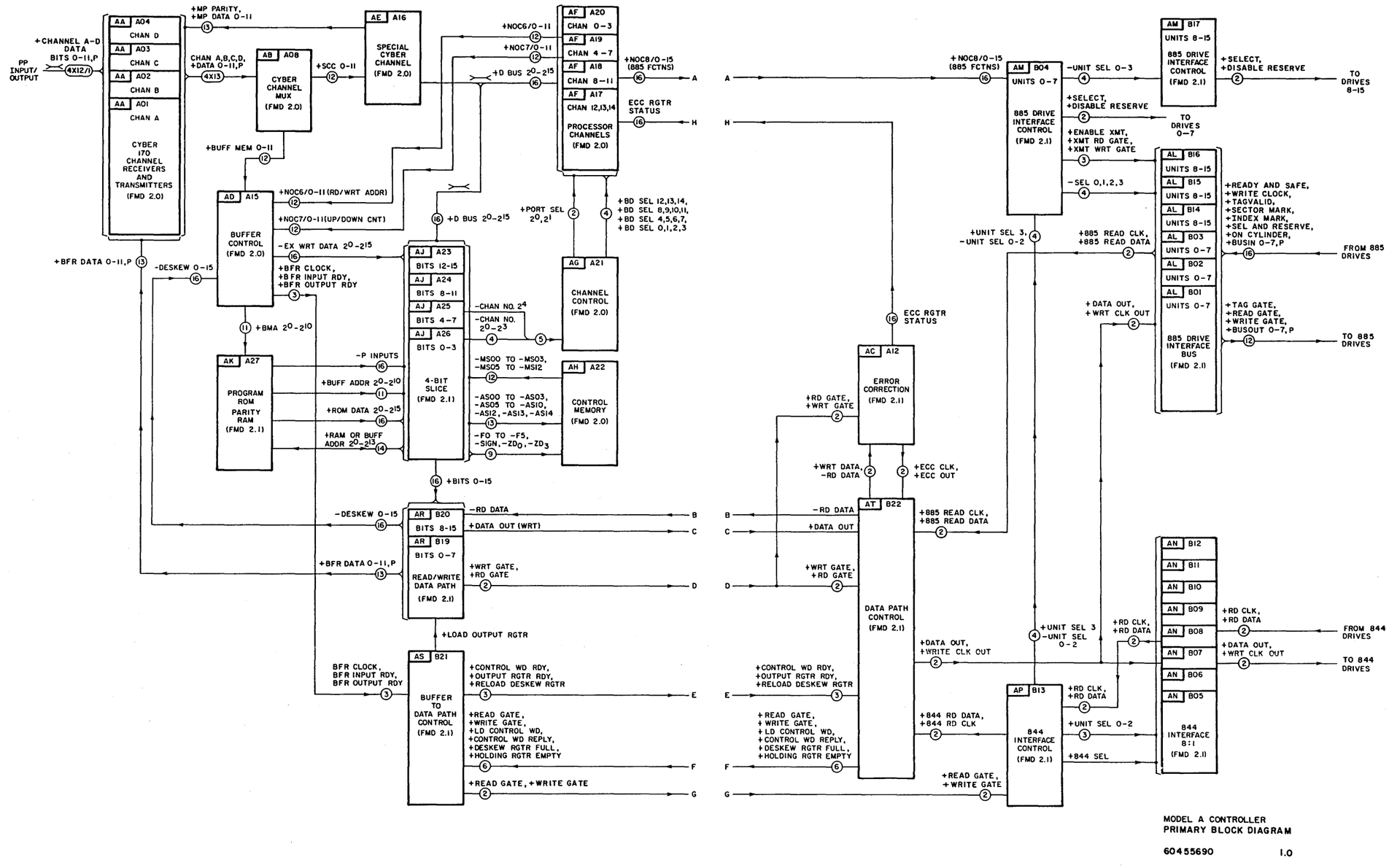
The processor section, which controls the controller hardware, contains the following memory.

- 4-K, 16-bit-per-word RAM called the program RAM. This contains the controlware.
- 2-K or 4-K, 16-bit-per-word buffer RAM.
- 1-K, 16-bit-per-word program ROM at A27. This contains some rudimentary diagnostics and an autoload procedure.
- Control memory ROM at A22 which has 256 60-bit words. This contains the PP instruction microcode.

The model A controller processor is located at A22 through A27. The model B controller processor is located at A22, A24, A26, and A27.

The buffer RAM in the model A controller is 2-K in locations A23 through A26. The buffer RAM in the model B controller is 4-K in locations A24 and A26.

The processor uses processor channels A17 through A20 to communicate with the rest of the controller hardware. The special CDC CYBER channel at A16 is used for communication between the processor and the PP. The D Bus provides a bidirectional path between the processor and the channels.



MODEL A CONTROLLER
PRIMARY BLOCK DIAGRAM

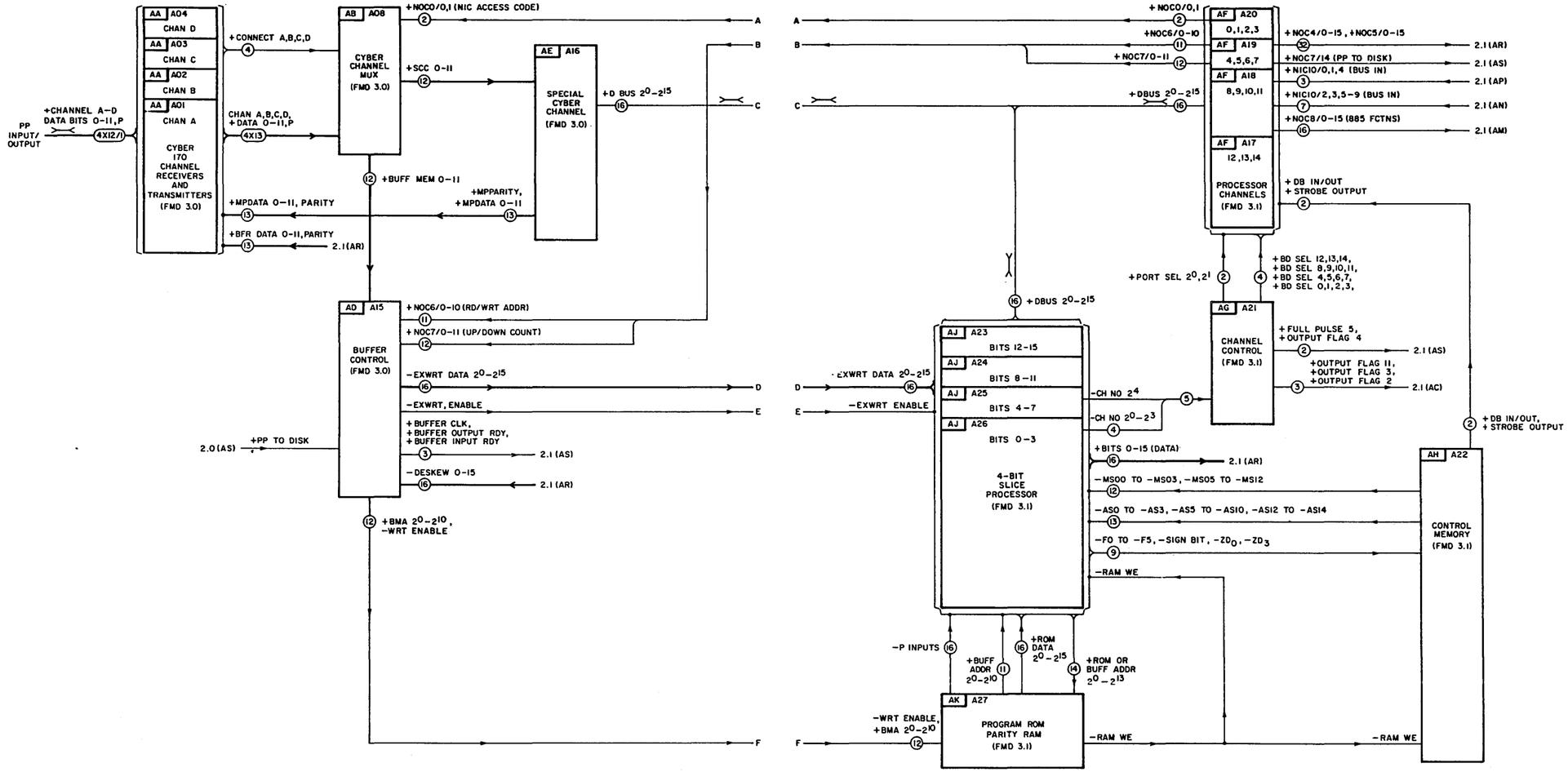
60455690 1.0

SECONDARY BLOCK DIAGRAM 2.0

This diagram shows the data path and some control signals for the PP interface and the processor sections of the controller.

Data paths:

PP to buffer	+Data Bits 0-11 from PP to A01 (or A02, A03, or A04) +Data 0-11 from A01 to A08 +Buff Mem 0-11 from A08 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 in model B controller
Buffer to PP	+Bits 0-15 from A23 through A26 to B19 and B20 in model A controller +Bits 0-15 from A24 and A26 to B19 and B20 in model B controller +Bfr Data 0-11 B19 and B20 to A01 (or A02, A03, or A04) +Data 0-11 from A01 to PP



MODEL A CONTROLLER
SECONDARY BLOCK DIAGRAM

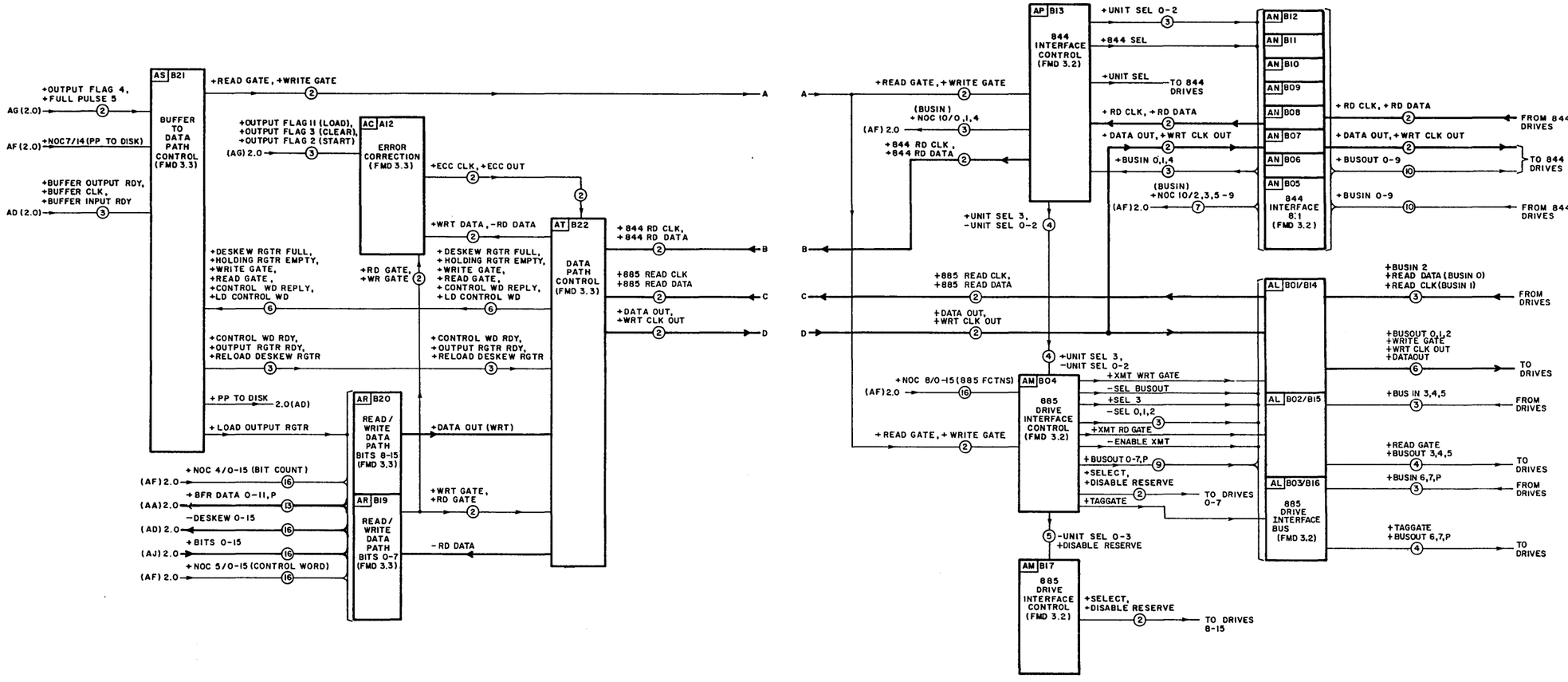
60455690 2.0

SECONDARY BLOCK DIAGRAM 2.1

This diagram shows the data paths and some control signals for the disk drive interface and data path control signals for the disk drive interface and data path control sections of the controller.

Data paths:

Buffer to disk	+Bits 0-15 from A23 through A26 (AJ) to B19 and B20 in model A controller +Bits 0-15 from A24 and A26 (BJ) to B19 and B20 in model B controller +Dataout from B20 to B22 +Dataout from B22 to B01 or B14, and B07 +Dataout to disk drive
885 to buffer	+Read Data from disk drive to B01 or B14 +885 Read Data from B01 or B14 to B22 -Rd Data from B22 to B19 -Deskew 0-15 from B19 and B20 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 (SBD 2.0) in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 (SBD 2.0) in model B controller
844 to buffer	+Rd Data from disk to B08 +Rd Data from B08 to B13 +Rd Data from B13 to B22 -Rd Data from B22 to B19 -Deskew 0-15 from B19 and B20 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 (SBD 2.0) in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 (SBD 2.0) in model B controller
Buffer to PP	+Bits 0-15 from A23 through A26 to B19 and B20 +Bfr Data 0-11 from B19 and B20 to A01 +Databits 0-11 from A01 to PP



MODEL A CONTROLLER
SECONDARY BLOCK DIAGRAM

60455690 2.1

INTERCONNECTION BLOCK DIAGRAM 3.0

This diagram shows all signals used on the PP interface, the special CDC CYBER channel, and the buffer control paks.

The PP interface consists of the channel receivers and transmitters and the CDC CYBER channel multiplexer. The model A controller comes with one channel access at location A01. The Channel Access Option can add three PP channel accesses. The model B controller does not include a channel access as standard equipment. Up to four Channel Access Options can be added to a model B controller.

The model A controller has a channel multiplexer at chassis location A08. The model B controller has channel multiplexers at chassis locations A07 and A08.

NOTE

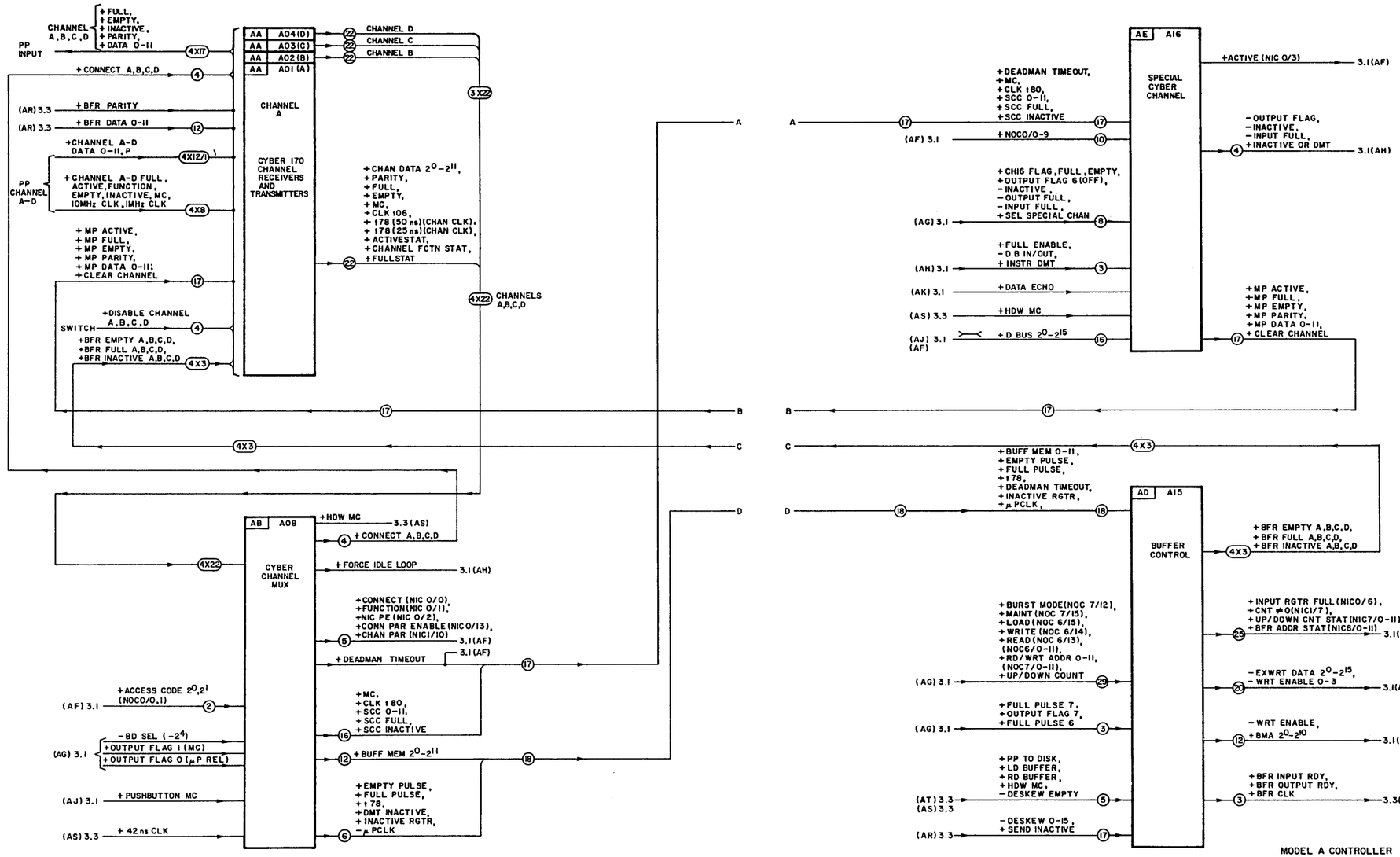
For termination reasons, location A01 must contain a 60-pak in the model A controller. The model B controller is terminated at location A07 and does not require a 60-pak at A01.

The pak at A16 contains the special CDC CYBER channel (channel 16). This is used for communication between the processor and the PP.

The buffer control controls the buffer memory read and write operations. This pak contains the up/down counter which indicates whether the buffer contains data or whether an overflow condition exists. It also has the read address counter and write address counter that determine the buffer read and write address.

Data paths:

PP to buffer	+Data 0-11 from PP to A01 (or A02, A03, or A04) +Chan Data 0-11 from A01 to A08 +Buff Mem 0-11 from A08 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 in the model A controller -Exwrt Data 0-15 from A15 to A24 and A26 in the model B controller
PP to special channel	+Data 0-11 from PP to A01 +Chan Data 0-11 from A01 to A08 +SCC 0-11 from A08 to A16 +D Bus 0-15 from A16 to A23 through A26 (AJ) in the model A controller +D Bus 0-15 from A16 to A24 and A26 (BJ) in the model B controller
Special channel to PP	+D Bus 0-15 from A23 through A26 to A16 in the model A controller +D Bus 0-15 from A24 and A26 to A16 in the model B controller +MP Data 0-11 from A16 to A01 +Data 0-11 from A01 to PP


CHANNEL A,B,C,D
+FULL, +EMPTY, +INACTIVE, +PARITY, +DATA 0-11
PP INPUT
4X17
+CONNECT A,B,C,D
(AR) 3.3
+BFR PARITY
+BFR DATA 0-11
+CHANNEL A-D DATA 0-11,P
4X12/1
PP CHANNEL A-D
+CHANNEL A-D FULL, ACTIVE, FUNCTION, EMPTY, INACTIVE, MC, 10MHz CLK, 1MHz CLK
4X8
+MP ACTIVE, +MP FULL, +MP EMPTY, +MP PARITY, +MP DATA 0-11, +CLEAR CHANNEL
+DISABLE CHANNEL A,B,C,D
SWITCH
+BFR EMPTY A,B,C,D, +BFR FULL A,B,C,D, +BFR INACTIVE A,B,C,D
4X3
AA A04(D)
AA A03(C)
AA A02(B)
AA A01(A)
CHANNEL A
CYBER 170 CHANNEL RECEIVERS AND TRANSMITTERS
CHANNEL D
CHANNEL C
CHANNEL B
3X22
+CHAN DATA 2^0-2^11, +PARITY, +FULL, +EMPTY, +MC, +CLK 106, +178(50 ns)(CHAN CLK), +178(25 ns)(CHAN CLK), +ACTIVESTAT, +CHANNEL FCTN STAT, +FULLSTAT
4X22
CHANNELS A,B,C,D
A
B
C
D
AB A08
CYBER CHANNEL MUX
+HDW MC
3.3(AS)
+CONNECT A,B,C,D
+FORCE IDLE LOOP
3.1(AH)
+CONNECT (NIC 0/0), +FUNCTION(NIC 0/1), +NIC PE (NIC 0/2), +CONN PAR ENABLE(NIC0/13), +CHAN PAR (NIC1/10)
3.1(AF)
+DEADMAN TIMEOUT
+ACCESS CODE 2^0,2^1 (NOCO/0,1)
(AF) 3.1
-BD SEL (-2^4)
+OUTPUT FLAG 1 (MC)
+OUTPUT FLAG 0 (μP REL)
(AG) 3.1
+MC, +CLK 180, +SCC 0-11, +SCC FULL, +SCC INACTIVE
+BUFF MEM 2^0-2^11
+PUSHBUTTON MC
(AJ) 3.1
+42 ns CLK
(AS) 3.3
+EMPTY PULSE, +FULL PULSE, +178, +DMT INACTIVE, +INACTIVE RGTR, -μPCLK
AE A16
SPECIAL CYBER CHANNEL
+DEADMAN TIMEOUT, +MC, +CLK 180, +SCC 0-11, +SCC FULL, +SCC INACTIVE
+NOCO/0-9
+ACTIVE (NIC 0/3)
3.1(AF)
-OUTPUT FLAG, -INACTIVE, -INPUT FULL, +INACTIVE OR DMT
3.1(AH)
+CH16 FLAG, FULL, EMPTY, +OUTPUT FLAG 6(OFF), -INACTIVE, -OUTPUT FULL, -INPUT FULL, +SEL SPECIAL CHAN
+FULL ENABLE, -D B IN/OUT, +INSTR DMT
+DATA ECHO
+HDW MC
+D BUS 2^0-2^15
+MP ACTIVE, +MP FULL, +MP EMPTY, +MP PARITY, +MP DATA 0-11, +CLEAR CHANNEL
AD A15
BUFFER CONTROL
+BUFF MEM 0-11, +EMPTY PULSE, +FULL PULSE, +178, +DEADMAN TIMEOUT, +INACTIVE RGTR, +μPCLK,
+BFR EMPTY A,B,C,D, +BFR FULL A,B,C,D, +BFR INACTIVE A,B,C,D
+BURST MODE(NOC 7/12), +MAINT(NOC 7/15), +LOAD(NOC 6/15), +WRITE(NOC 6/14), +READ(NOC 6/13), (NOC6/0-11), +RD/WRT ADDR 0-11, (NOC7/0-11), +UP/DOWN COUNT
+INPUT RGTR FULL(NICO/6), +CNT ≠0(NIC1/7), +UP/DOWN CNT STAT(NIC7/0-11), +BFR ADDR STAT(NIC6/0-11)
3.1(AF)
-EXWRT DATA 2^0-2^15, -WRT ENABLE 0-3
3.1(AJ)
+FULL PULSE 7, +OUTPUT FLAG 7, +FULL PULSE 6
-WRT ENABLE, +BMA 2^0-2^10
3.1(AK)
+PP TO DISK, +LD BUFFER, +RD BUFFER, +HDW MC, -DESKEW EMPTY
(AT) 3.3 (AS) 3.3
+BFR INPUT RDY, +BFR OUTPUT RDY, +BFR CLK
3.3(AS)
-DESKEW 0-15, +SEND INACTIVE
(AR) 3.3

MODEL A CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

60455690 3.0

INTERCONNECTION BLOCK DIAGRAM 3.1

This diagram shows all signals used in the processor section of the controller including the processor channels.

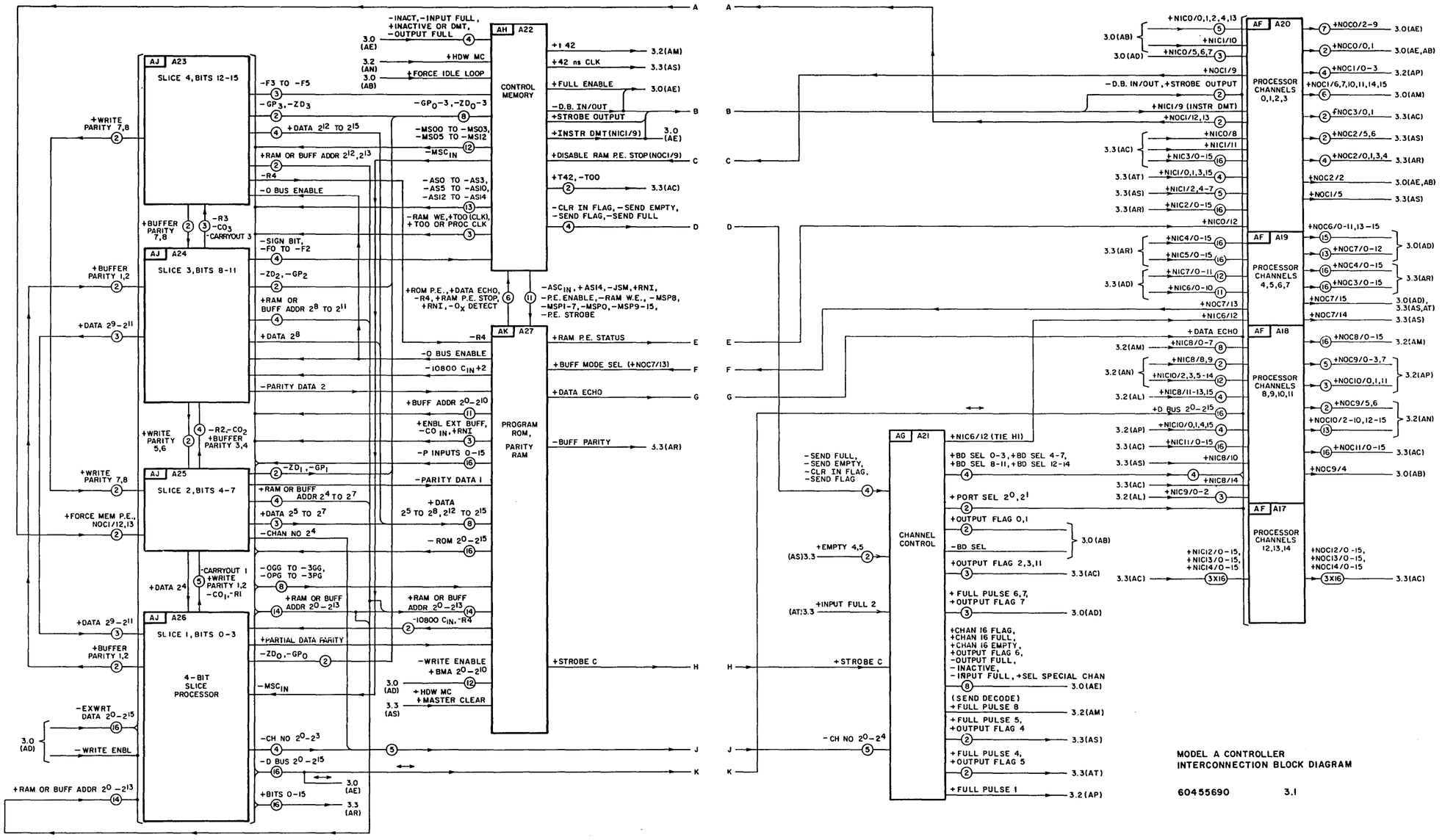
Each of the four 4-bit slice processor paks in the model A controller handles four bits of the 16-bit processor word. The four paks contain the 4-K program RAM, the 2-K buffer memory, and the 10800 and 10803 microprocessor chips.

Each of the 8-bit slice processor paks in the model B controller handles eight bits of the 16-bit processor word. The two paks contain the 4-K program RAM, the 4-K buffer memory, and the 10800 and 10803 microprocessor chips.

The pak at location A27 contains the parity RAM that holds the parity bits for words stored in the program RAM and the buffer memory. It also contains the program ROM which has a capacity of 1024 16-bit words. Program ROM contains an autoload program and some rudimentary diagnostics.

Control memory, at A22, is a ROM with a capacity of 256 60-bit words. Control memory is used primarily for processor channel control and 10800/10803 control.

The processor uses the 15 bidirectional channels at A17, A18, A19, and A20 to control and receive status from the rest of the controller hardware. Output channels are labeled NOCx/xx. For example, NOC1/15 indicates normal output channel 1, bit 15. Input channels are labeled NICx/xx. Channels 0 through 14 are used; channel 15 is not used.



MODEL A CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

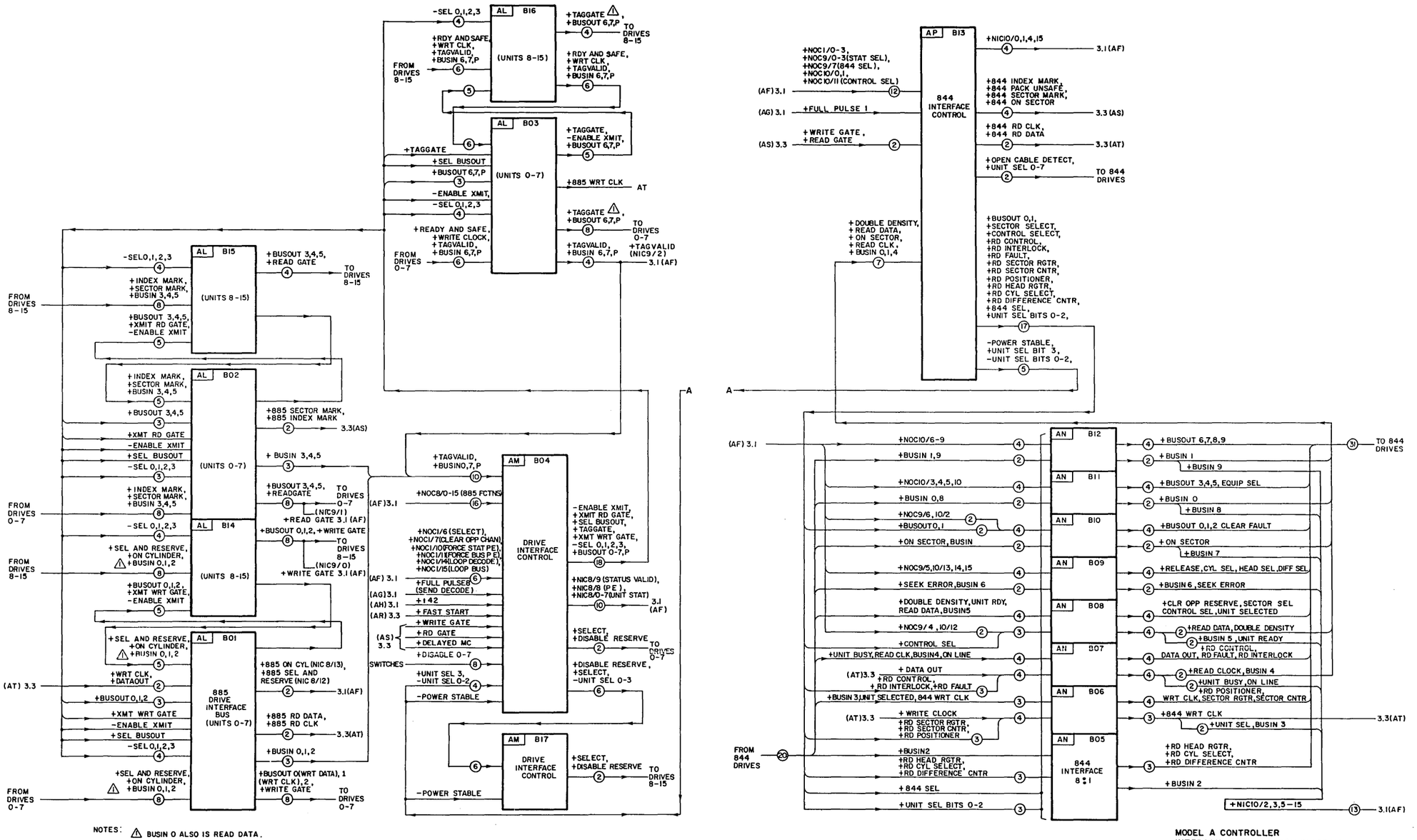
60455690 3.1

INTERCONNECTION BLOCK DIAGRAM 3.2

This diagram shows all signals used in the disk interface section of the controller. 60-paks at chassis locations B01, B02, B03, and B04 provide the interface for 885 drive units 0 through 7. 60-paks at B14, B15, B16, and B17 are part of the Four FMD Option that provides the interface for 885 drive units 8 through 15.

The paks at B05 through B12 are part of the 844 Drive Option that provides the interface for eight 844 disk storage units. The pak at B13 controls this interface.

The paks at B14, B15, B16, and B17 have a parallel function to those at B01, B02, B03, and B04. B14 receives signals from and sends signals to B01. B15/B02, B16/B03 and B17/B04 have the same relationship.



MODEL A CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

60455690 3.2

INTERCONNECTION BLOCK DIAGRAM 3.3

This diagram shows all the signals in the data path control section of the controller and the error correction pak. This logic does the following:

Control Word Executing

The control word, sent by the processor from normal output channel 5, controls or initiates some operations in the controller and disk. The control word resides in the control word register at B19 and B20.

The bit count, sent by the processor from normal output channel 4, determines the duration of the control word sequence. The bit count resides in the bit counter at B19 and B20. When the bit counter decrements to zero the control word sequence is completed.

Mark start delay code, formed by NOC5/6 and NOC5/7, delays the start of bit counter decrementing. The delay depends upon the code which may be a sector mark delay, on sector delay, or index mark delay.

Sync Byte Generation/Detection

During a disk write, the controller generates a sync byte at B19 and B20 and NOC5/0 initiates writing sync byte. During a disk read, the controller detects the sync byte at B22 and checks it for correctness at B19 and B20.

Read/Write Control

This section of the controller provides the following part of the write data path.

+Bits 0-15 from processor to B19 and B20
+Data Out from B20 to B22
+Data Out from B22 to B01, B02, or B03 (AL, 3.2)

This section of the controller provides the following part of the read data path.

+Rd Data from B01, B02, or B03 (AL) to B22
-Read Data from B22 to B19
-Deskew 0-15 from B19 to A15 (AD or BD, 3.0)

This section of the controller provides the following part of the buffer memory to PP data path.

-Bits 0-11 from A23 through A26 (AJ, 3.1) to B19 and B20 in the model A controller
-Bits 0-11 from A24 and A26 (BJ, 3.1) to B19 and B20 in the model B controller
+Bfr Data 0-11 to A01, A02, A03, or A04 (AA, 3.0)

The byte counter and compare circuit at B22 work together to gate data into the deskew register at B19 and B20 during a disk read or to gate data into the shift register at B19 and B20 during a disk write. During a read, 12- or 16-bit bytes are assembled in the shift register from serial data. During a write, 12- or 16-bit bytes must be disassembled into serial data. A 12- or 16-bit byte is sent from the holding register at B19 and B20 into the shift register.

Clock Control

Bits 13 and 14 of the control word (selected by NOC5/13, 14) contain a code that selects one of three clocks used to drive sequence control and to provide clock pulses for the bit counter and shift register at AR, and the ECC register at AC. +Clk Select 0 (bit 13) and +Clk Select 1 (bit 14) provide the code on this pak as follows:

Clk Select 1	0	
L	L	Wrt Clk from drive
L	H	Rd Clk from drive
H	L	Processor Clk
H	H	Processor Clk

The clock period for these clocks is as follows:

Processor Clk - 85 ns

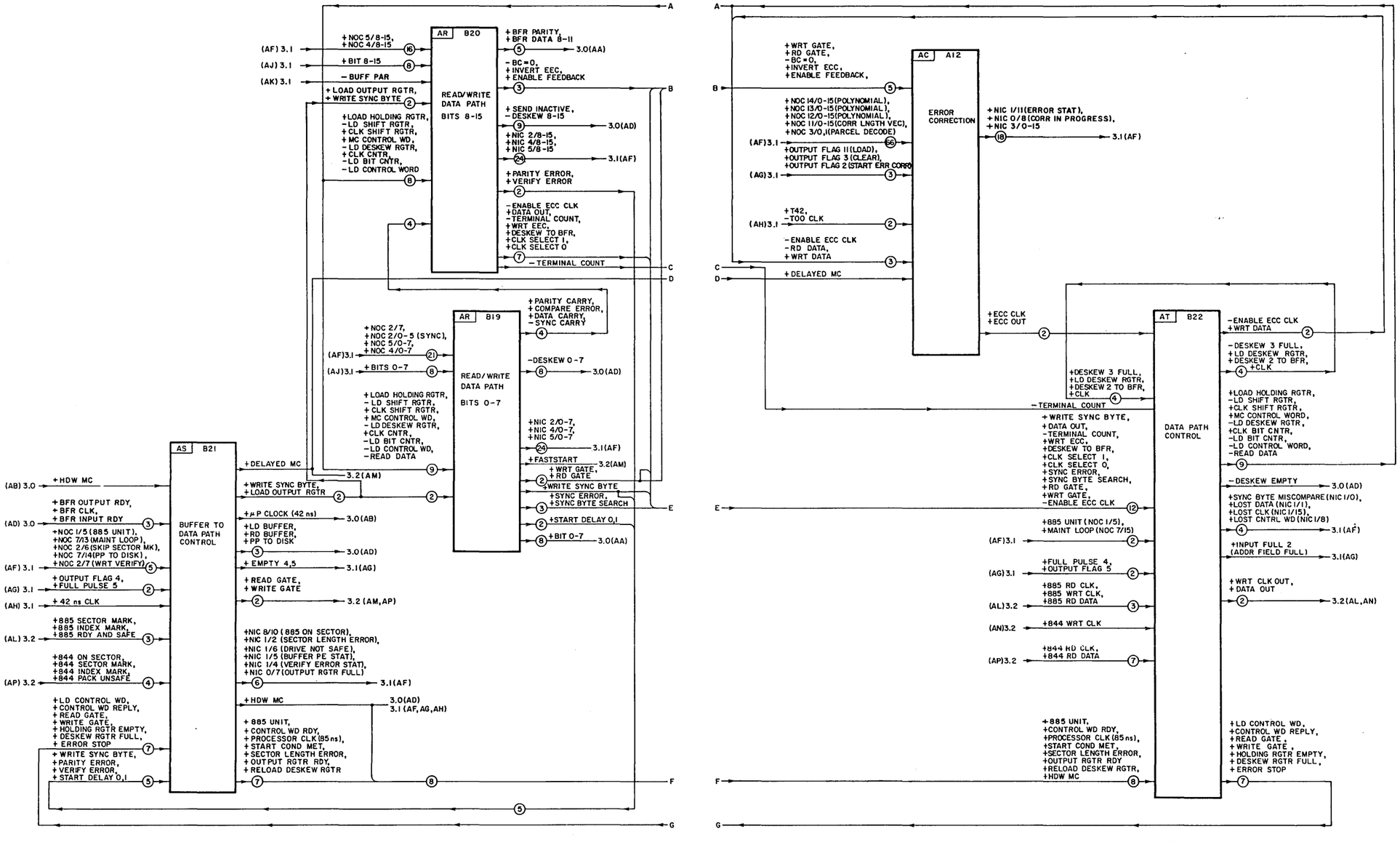
885 Rd or Wrt Clk - 104 ns

844 Rd or Wrt Clk - 144 ns

When the clock selection changes, the clock pulses for the shift register and bit counter are blocked for the next two or three full clock periods.

Error Correction

All read and write data is sent to the error correction pak. A checkword is generated and written at the end of the data record during a write. During a read, the checkword is regenerated and used to determine if there was a data error. If an error is detected, the controller attempts to correct it.


AR B20
READ/WRITE DATA PATH BITS 8-15
AR B19
READ/WRITE DATA PATH BITS 0-7
AS B21
BUFFER TO DATA PATH CONTROL
AC A12
ERROR CORRECTION
AT B22
DATA PATH CONTROL
+NOC 5/8-15, +NOC 4/8-15
+BIT 8-15
-BUFF PAR
+LOAD OUTPUT RGTR, +WRITE SYNC BYTE
+LOAD HOLDING RGTR, -LD SHIFT RGTR, +CLK SHIFT RGTR, +MC CONTROL WD, -LD DESKEW RGTR, +CLK CNTR, -LD BIT CNTR, -LD CONTROL WORD
+BFR PARITY, +BFR DATA 8-11
-BC=0, +INVERT EEC, +ENABLE FEEDBACK
+SEND INACTIVE, -DESKEW 8-15
+NIC 2/8-15, +NIC 4/8-15, +NIC 5/8-15
+PARITY ERROR, +VERIFY ERROR
-ENABLE ECC CLK, +DATA OUT, -TERMINAL COUNT, +WRT EEC, +DESKEW TO BFR, +CLK SELECT 1, +CLK SELECT 0
-TERMINAL COUNT
+PARITY CARRY, +COMPARE ERROR, +DATA CARRY, -SYNC CARRY
+NOC 2/7, +NOC 2/0-5 (SYNC), +NOC 5/0-7, +NOC 4/0-7
+BITS 0-7
-DESKEW 0-7
+NIC 2/0-7, +NIC 4/0-7, +NIC 5/0-7
+FASTSTART
+WRT GATE, +RD GATE
+WRITE SYNC BYTE
+SYNC ERROR, +SYNC BYTE SEARCH
+START DELAY 0,1
+BIT 0-7
+HDW MC
+DELAYED MC
+WRITE SYNC BYTE, +LOAD OUTPUT RGTR
+μP CLOCK (42 ns)
+LD BUFFER, +RD BUFFER, +PP TO DISK
+EMPTY 4,5
+READ GATE, +WRITE GATE
+NIC 8/10 (885 ON SECTOR), +NIC 1/2 (SECTOR LENGTH ERROR), +NIC 1/6 (DRIVE NOT SAFE), +NIC 1/5 (BUFFER PE STAT), +NIC 1/4 (VERIFY ERROR STAT), +NIC 0/7 (OUTPUT RGTR FULL)
+885 UNIT, +CONTROL WD RDY, +PROCESSOR CLK (85 ns), +START COND MET, +SECTOR LENGTH ERROR, +OUTPUT RGTR RDY, +RELOAD DESKEW RGTR
+HDW MC, +BFR OUTPUT RDY, +BFR CLK, +BFR INPUT RDY, +NOC 1/5 (885 UNIT), +NOC 7/13 (MAINT LOOP), +NOC 2/6 (SKIP SECTOR MK), +NOC 7/14 (PP TO DISK), +NOC 2/7 (WRT VERIFY), +OUTPUT FLAG 4, +FULL PULSE 5, +42 ns CLK, +885 SECTOR MARK, +885 INDEX MARK, +885 RDY AND SAFE, +844 ON SECTOR, +844 SECTOR MARK, +844 INDEX MARK, +844 PACK UNSAFE, +LD CONTROL WD, +CONTROL WD REPLY, +READ GATE, +WRITE GATE, +HOLDING RGTR EMPTY, +DESKEW RGTR FULL, +ERROR STOP, +WRITE SYNC BYTE, +PARITY ERROR, +VERIFY ERROR, +START DELAY 0,1
+WRT GATE, +RD GATE, -BC=0, +INVERT ECC, +ENABLE FEEDBACK
+NOC 14/0-15 (POLYNOMIAL), +NOC 13/0-15 (POLYNOMIAL), +NOC 12/0-15 (POLYNOMIAL), +NOC 11/0-15 (CORR LNGTH VEC), +NOC 3/0, I (PARCEL DECODE)
+OUTPUT FLAG 11 (LOAD), +OUTPUT FLAG 3 (CLEAR), +OUTPUT FLAG 2 (START ERR CORR)
+T42, -TOO CLK
-ENABLE ECC CLK, -RD DATA, +WRT DATA
+DELAYED MC
+NIC 1/11 (ERROR STAT), +NIC 0/8 (CORR IN PROGRESS), +NIC 3/0-15
+ECC CLK, +ECC OUT
+DESKEW 3 FULL, +LD DESKEW RGTR, +DESKEW 2 TO BFR, +CLK
-TERMINAL COUNT
+WRITE SYNC BYTE, +DATA OUT, -TERMINAL COUNT, +WRT ECC, +DESKEW TO BFR, +CLK SELECT 1, +CLK SELECT 0, +SYNC ERROR, +SYNC BYTE SEARCH, +RD GATE, +WRT GATE, -ENABLE ECC CLK
+885 UNIT (NOC 1/5), +MAINT LOOP (NOC 7/15)
+FULL PULSE 4, +OUTPUT FLAG 5
+885 RD CLK, +885 WRT CLK, +885 RD DATA
+844 WRT CLK
+844 RD CLK, +844 RD DATA
+885 UNIT, +CONTROL WD RDY, +PROCESSOR CLK (85 ns), +START COND MET, +SECTOR LENGTH ERROR, +OUTPUT RGTR RDY, +RELOAD DESKEW RGTR, +HDW MC
-ENABLE ECC CLK, +WRT DATA
-DESKEW 3 FULL, +LD DESKEW RGTR, +DESKEW 2 TO BFR, +CLK
+LOAD HOLDING RGTR, -LD SHIFT RGTR, +CLK SHIFT RGTR, +MC CONTROL WORD, -LD DESKEW RGTR, +CLK BIT CNTR, -LD BIT CNTR, -LD CONTROL WORD, -READ DATA
-DESKEW EMPTY
+SYNC BYTE MISCOMPARE (NIC 1/0), +LOST DATA (NIC 1/1), +LOST CLK (NIC 1/15), +LOST CNTRL WD (NIC 1/8)
+INPUT FULL 2 (ADDR FIELD FULL)
+WRT CLK OUT, +DATA OUT
+LD CONTROL WD, +CONTROL WD REPLY, +READ GATE, +WRITE GATE, +HOLDING RGTR EMPTY, +DESKEW RGTR FULL, +ERROR STOP
(AB) 3.0
(AD) 3.0
(AF) 3.1
(AG) 3.1
(AH) 3.1
(AJ) 3.1
(AK) 3.1
(AL) 3.2
(AM) 3.2
(AP) 3.2
3.0(AA)
3.0(AB)
3.0(AD)
3.1(AF)
3.1(AG)
3.2(AM,AP)
3.2(AL,AN)
3.0(AD) 3.1(AF,AG,AH)
A
B
C
D
E
F
G

MODEL A CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

60455690 3.3

PRIMARY BLOCK DIAGRAM 1.0

This diagram shows all 60-paks in the controller including the options.

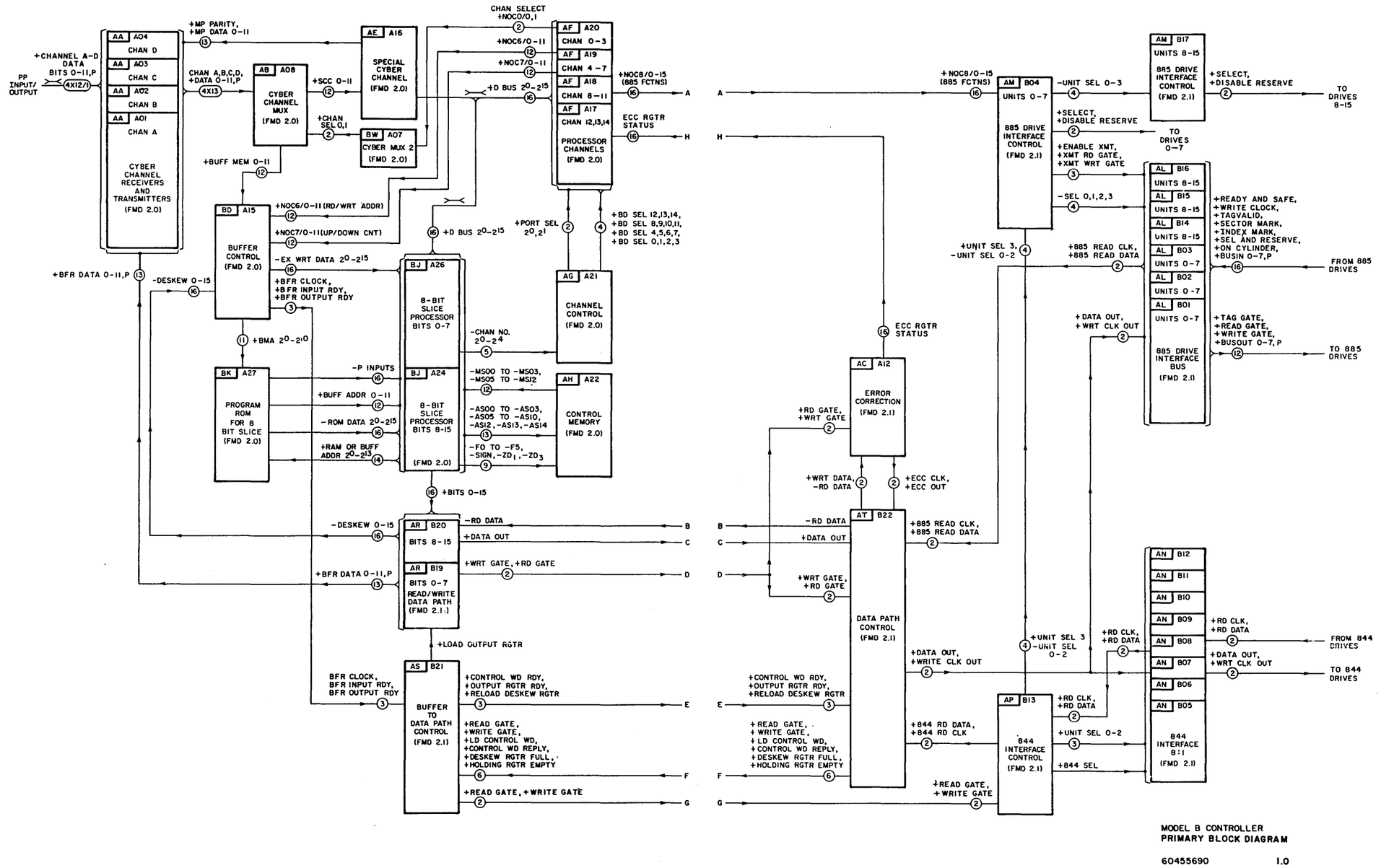
The processor section, which controls the controller hardware, contains the following memory.

- 4-K, 16-bit-per-word RAM called the program RAM. This contains the controlware.
- 2-K or 4-K, 16-bit-per-word buffer RAM.
- 1-K, 16-bit-per-word program ROM at A27. This contains some rudimentary diagnostics and an autoload procedure.
- Control memory ROM at A22 which has 256 60-bit words. This contains the PP instruction microcode.

The model A controller processor is located at A22 through A27. The model B controller processor is located at A22, A24, A26, and A27.

The buffer RAM in the model A controller is 2-K in locations A23 through A26. The buffer RAM in the model B controller is 4-K in locations A24 and A26.

The processor uses processor channels A17 through A20 to communicate with the rest of the controller hardware. The special CDC CYBER channel at A16 is used for communication between the processor and the PP. The D Bus provides a bidirectional path between the processor and the channels.


PP INPUT/ OUTPUT
4X12/1
+CHANNEL A-D DATA BITS 0-11,P
AA A04 CHAN D
AA A03 CHAN C
AA A02 CHAN B
AA A01 CHAN A
CYBER CHANNEL RECEIVERS AND TRANSMITTERS (FMD 2.0)
+MP PARITY, +MP DATA 0-11
CHAN A,B,C,D, +DATA 0-11,P
4X13
AB A08 CYBER CHANNEL MUX (FMD 2.0)
+SCC 0-11
+CHAN SEL 0,1
AE A16 SPECIAL CYBER CHANNEL (FMD 2.0)
BW A07 CYBER MUX 2 (FMD 2.0)
CHAN SELECT +NOC0/0,1
+NOC6/0-11
+NOC7/0-11
+D BUS 20-215
AF A20 CHAN 0-3
AF A19 CHAN 4-7
AF A18 CHAN 8-11
AF A17 CHAN 12,13,14
PROCESSOR CHANNELS (FMD 2.0)
+NOC8/0-15 (885 FCTNS)
ECC RGTR STATUS
A
H
+BUFF MEM 0-11
BD A15 BUFFER CONTROL (FMD 2.0)
+NOC6/0-11 (RD/WRT ADDR)
+NOC7/0-11 (UP/DOWN CNT)
-EX WRT DATA 20-215
+BFR CLOCK, +BFR INPUT RDY, +BFR OUTPUT RDY
+BFR DATA 0-11,P
-DESKEW 0-15
+PORT SEL 20,21
+BD SEL 12,13,14, +BD SEL 8,9,10,11, +BD SEL 4,5,6,7, +BD SEL 0,1,2,3
AG A21 CHANNEL CONTROL (FMD 2.0)
BJ A26 8-BIT SLICE PROCESSOR BITS 0-7
-CHAN NO. 20-24
+BMA 20-210
BK A27 PROGRAM ROM FOR 8 BIT SLICE (FMD 2.0)
-P INPUTS
+BUFF ADDR 0-11
-ROM DATA 20-215
+RAM OR BUFF ADDR 20-213
BJ A24 8-BIT SLICE PROCESSOR BITS 8-15 (FMD 2.0)
-MS00 TO -MS03, -MS05 TO -MS12
-AS00 TO -AS03, -AS05 TO -AS10, -AS12, -AS13, -AS14
-FO TO -F5, -SIGN, -ZD1, -ZD3
AH A22 CONTROL MEMORY (FMD 2.0)
+BITS 0-15
AR B20 BITS 8-15
AR B19 BITS 0-7 READ/WRITE DATA PATH (FMD 2.1)
-RD DATA
+DATA OUT
+WRT GATE, +RD GATE
B
C
D
+LOAD OUTPUT RGTR
AS B21 BUFFER TO DATA PATH CONTROL (FMD 2.1)
BFR CLOCK, BFR INPUT RDY, BFR OUTPUT RDY
+CONTROL WD RDY, +OUTPUT RGTR RDY, +RELOAD DESKEW RGTR
+READ GATE, +WRITE GATE, +LD CONTROL WD, +CONTROL WD REPLY, +DESKEW RGTR FULL, +HOLDING RGTR EMPTY
+READ GATE, +WRITE GATE
E
F
G
AM B04 UNITS 0-7
885 DRIVE INTERFACE CONTROL (FMD 2.1)
-UNIT SEL 0-3
+SELECT, +DISABLE RESERVE
+ENABLE XMT, +XMT RD GATE, +XMT WRT GATE
-SEL 0,1,2,3
+UNIT SEL 3, -UNIT SEL 0-2
AM B17 UNITS 8-15
885 DRIVE INTERFACE CONTROL (FMD 2.1)
TO DRIVES 8-15
TO DRIVES 0-7
AL B16 UNITS 8-15
AL B15 UNITS 8-15
AL B14 UNITS 8-15
AL B03 UNITS 0-7
AL B02 UNITS 0-7
AL B01 UNITS 0-7
+885 READ CLK, +885 READ DATA
+READY AND SAFE, +WRITE CLOCK, +TAGVALID, +SECTOR MARK, +INDEX MARK, +SEL AND RESERVE, +ON CYLINDER, +BUSIN 0-7,P
FROM 885 DRIVES
+DATA OUT, +WRT CLK OUT
+TAG GATE, +READ GATE, +WRITE GATE, +BUSOUT 0-7,P
TO 885 DRIVES
885 DRIVE INTERFACE BUS (FMD 2.1)
AC A12 ERROR CORRECTION (FMD 2.1)
+RD GATE, +WRT GATE
+WRT DATA, -RD DATA
+ECC CLK, +ECC OUT
AT B22 DATA PATH CONTROL (FMD 2.1)
+885 READ CLK, +885 READ DATA
+DATA OUT, +WRITE CLK OUT
+UNIT SEL 3, -UNIT SEL 0-2
+RD CLK, +RD DATA
AP B13 844 INTERFACE CONTROL (FMD 2.1)
+844 RD DATA, +844 RD CLK
+844 SEL
AN B12
AN B11
AN B10
AN B09
AN B08
AN B07
AN B06
AN B05
844 INTERFACE 8:1 (FMD 2.1)
+RD CLK, +RD DATA
FROM 844 DRIVES
+DATA OUT, +WRT CLK OUT
TO 844 DRIVES

MODEL B CONTROLLER
PRIMARY BLOCK DIAGRAM

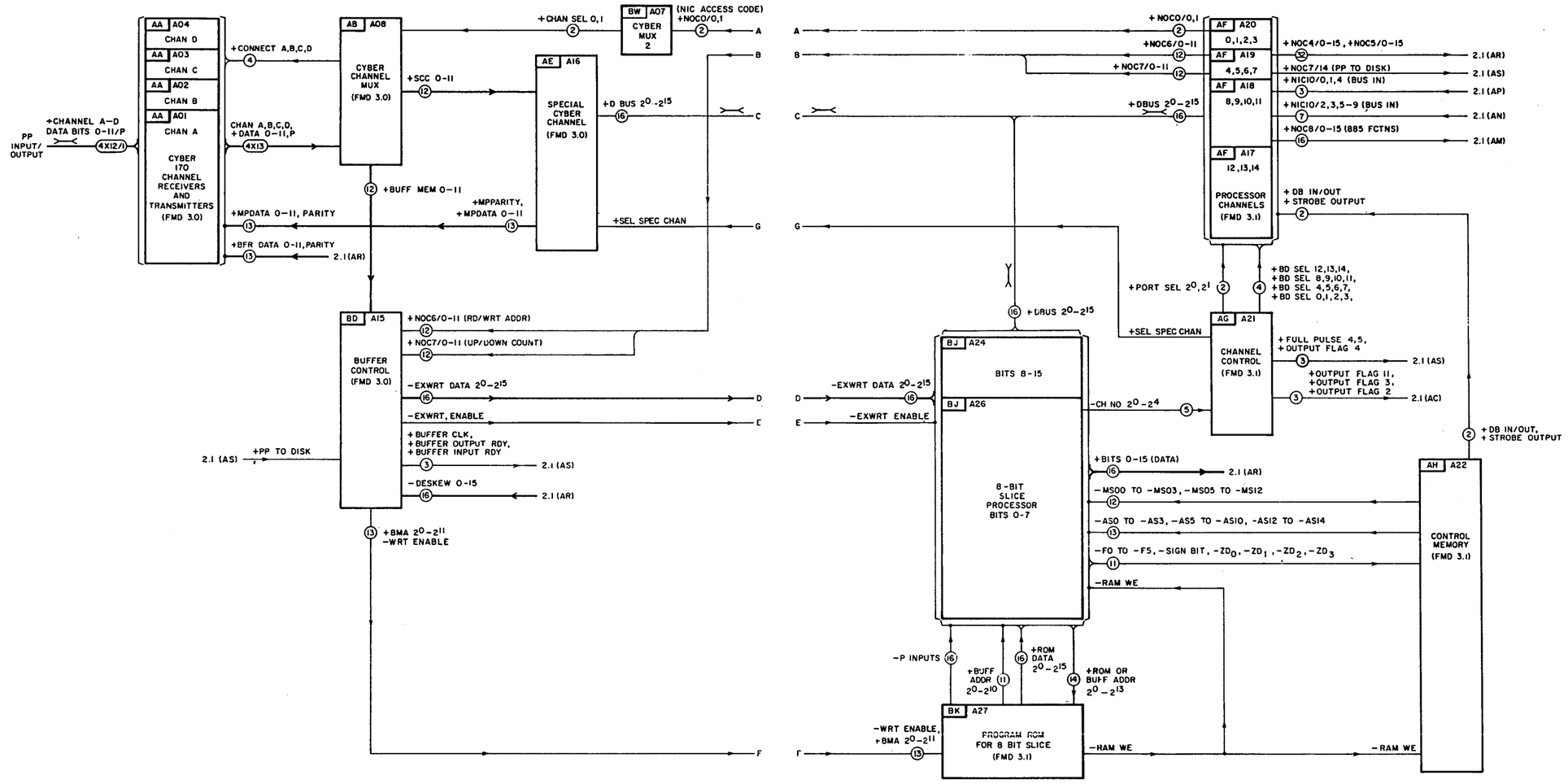
60455690 1.0

SECONDARY BLOCK DIAGRAM 2.0

This diagram shows the data path and some control signals for the PP interface and the processor sections of the controller.

Data paths:

PP to buffer	+Data Bits 0-11 from PP to A01 (or A02, A03, or A04) +Data 0-11 from A01 to A08 +Buff Mem 0-11 from A08 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 in model B controller
Buffer to PP	+Bits 0-15 from A23 through A26 to B19 and B20 in model A controller +Bits 0-15 from A24 and A26 to B19 and B20 in model B controller +Bfr Data 0-11 B19 and B20 to A01 (or A02, A03, or A04) +Data 0-11 from A01 to PP



MODEL B CONTROLLER
SECONDARY BLOCK DIAGRAM

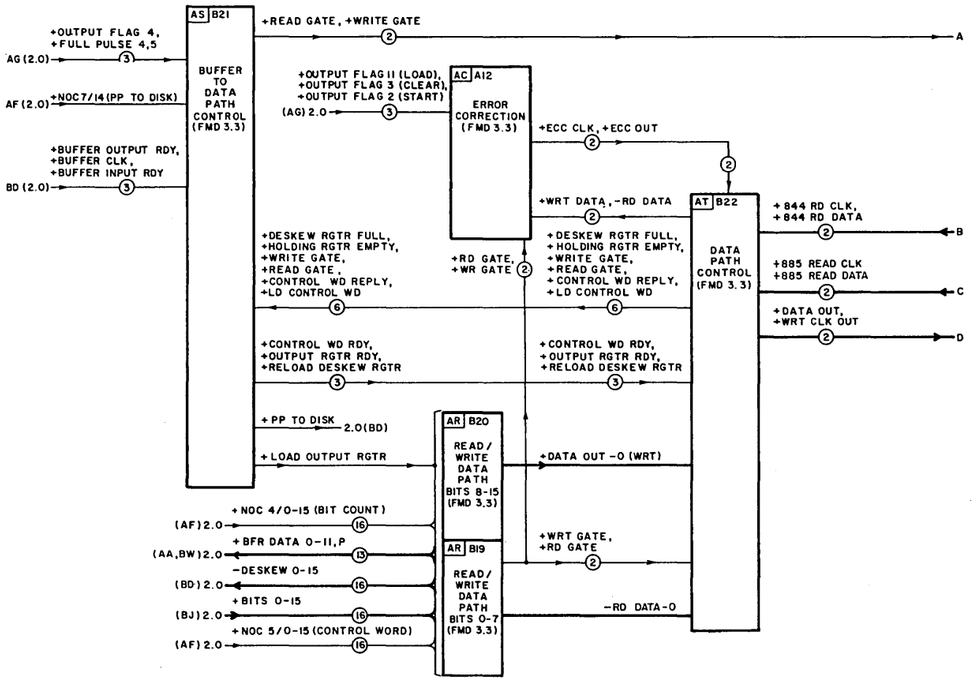
60455690 2.0

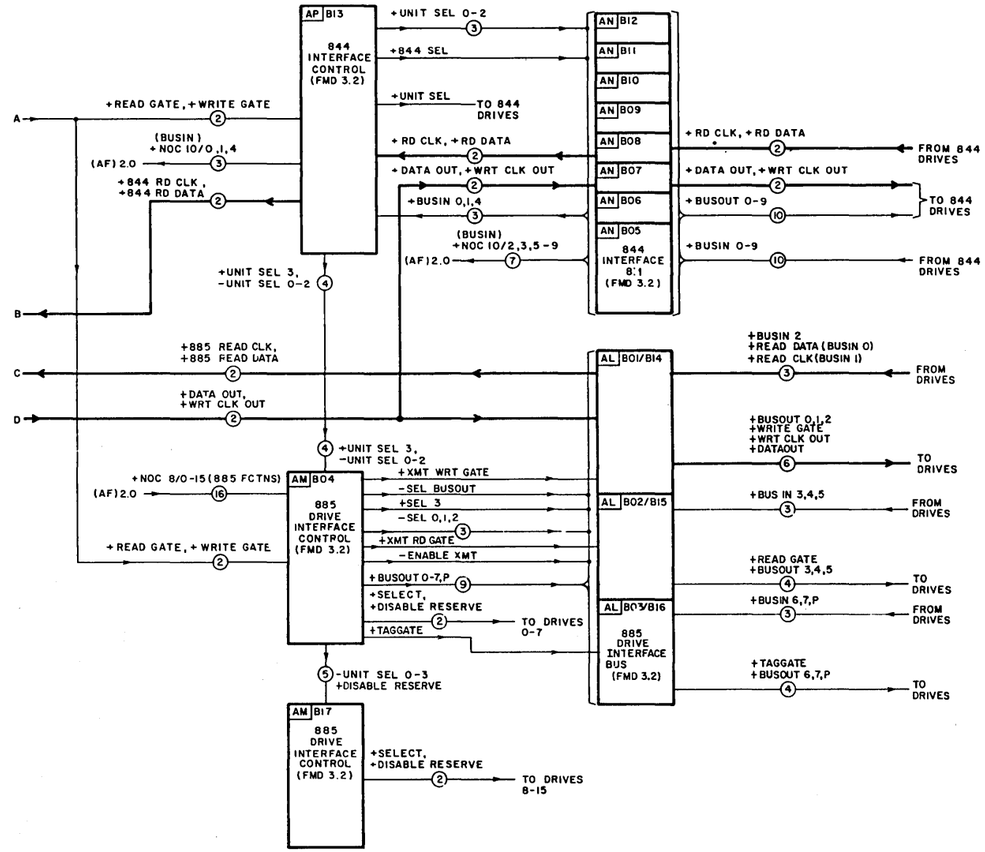
SECONDARY BLOCK DIAGRAM 2.1

This diagram shows the data paths and some control signals for the disk drive interface and data path control signals for the disk drive interface and data path control sections of the controller.

Data paths:

Buffer to disk	+Bits 0-15 from A23 through A26 (AJ) to B19 and B20 in model A controller +Bits 0-15 from A24 and A26 (BJ) to B19 and B20 in model B controller +Dataout from B20 to B22 +Dataout from B22 to B01 or B14, and B07 +Dataout to disk drive
885 to buffer	+Read Data from disk drive to B01 or B14 +885 Read Data from B01 or B14 to B22 -Rd Data from B22 to B19 -Deskew 0-15 from B19 and B20 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 (SBD 2.0) in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 (SBD 2.0) in model B controller
844 to buffer	+Rd Data from disk to B08 +Rd Data from B08 to B13 +Rd Data from B13 to B22 -Rd Data from B22 to B19 -Deskew 0-15 from B19 and B20 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 (SBD 2.0) in model A controller -Exwrt Data 0-15 from A15 to A24 and A26 (SBD 2.0) in model B controller
Buffer to PP	+Bits 0-15 from A23 through A26 to B19 and B20 +Bfr Data 0-11 from B19 and B20 to A01 +Databits 0-11 from A01 to PP





MODEL B CONTROLLER
SECONDARY BLOCK DIAGRAM

60455690 2.1

INTERCONNECTION BLOCK DIAGRAM 3.0

This diagram shows all signals used on the PP interface, the special CDC CYBER channel, and the buffer control paks.

The PP interface consists of the channel receivers and transmitters and the CDC CYBER channel multiplexer. The model A controller comes with one channel access at location A01. The Channel Access Option can add three PP channel accesses. The model B controller does not include a channel access as standard equipment. Up to four Channel Access Options can be added to a model B controller.

The model A controller has a channel multiplexer at chassis location A08. The model B controller has channel multiplexers at chassis locations A07 and A08.

NOTE

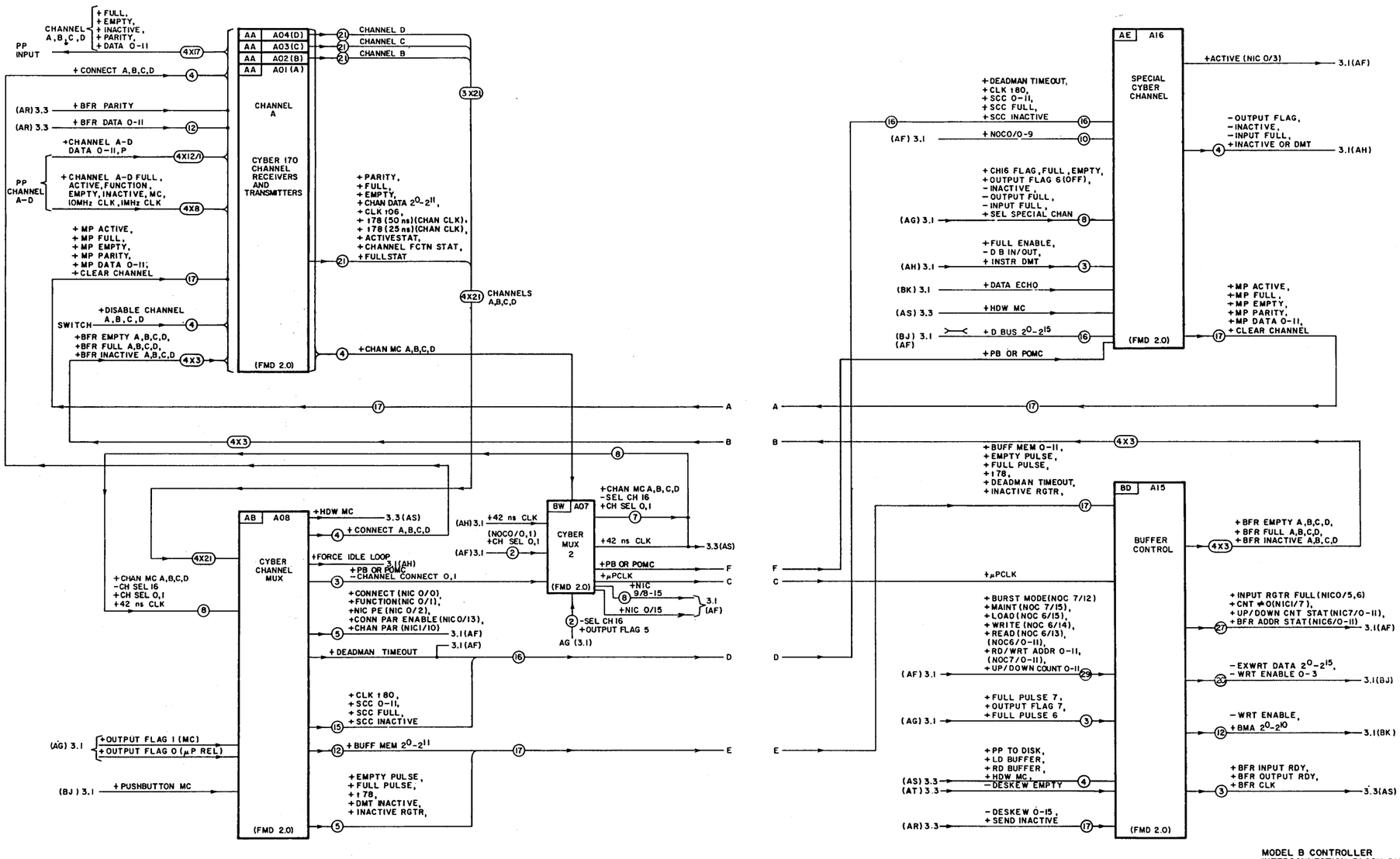
For termination reasons, location A01 must contain a 60-pak in the model A controller. The model B controller is terminated at location A07 and does not require a 60-pak at A01.

The pak at A16 contains the special CDC CYBER channel (channel 16). This is used for communication between the processor and the PP.

The buffer control controls the buffer memory read and write operations. This pak contains the up/down counter which indicates whether the buffer contains data or whether an overflow condition exists. It also has the read address counter and write address counter that determine the buffer read and write address.

Data paths:

PP to buffer	+Data 0-11 from PP to A01 (or A02, A03, or A04) +Chan Data 0-11 from A01 to A08 +Buff Mem 0-11 from A08 to A15 -Exwrt Data 0-15 from A15 to A23 through A26 in the model A controller -Exwrt Data 0-15 from A15 to A24 and A26 in the model B controller
PP to special channel	+Data 0-11 from PP to A01 +Chan Data 0-11 from A01 to A08 +SCC 0-11 from A08 to A16 +D Bus 0-15 from A16 to A23 through A26 (AJ) in the model A controller +D Bus 0-15 from A16 to A24 and A26 (BJ) in the model B controller
Special channel to PP	+D Bus 0-15 from A23 through A26 to A16 in the model A controller +D Bus 0-15 from A24 and A26 to A16 in the model B controller +MP Data 0-11 from A16 to A01 +Data 0-11 from A01 to PP



MODEL B CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

60455690 3.0

INTERCONNECTION BLOCK DIAGRAM 3.1

This diagram shows all signals used in the processor section of the controller including the processor channels.

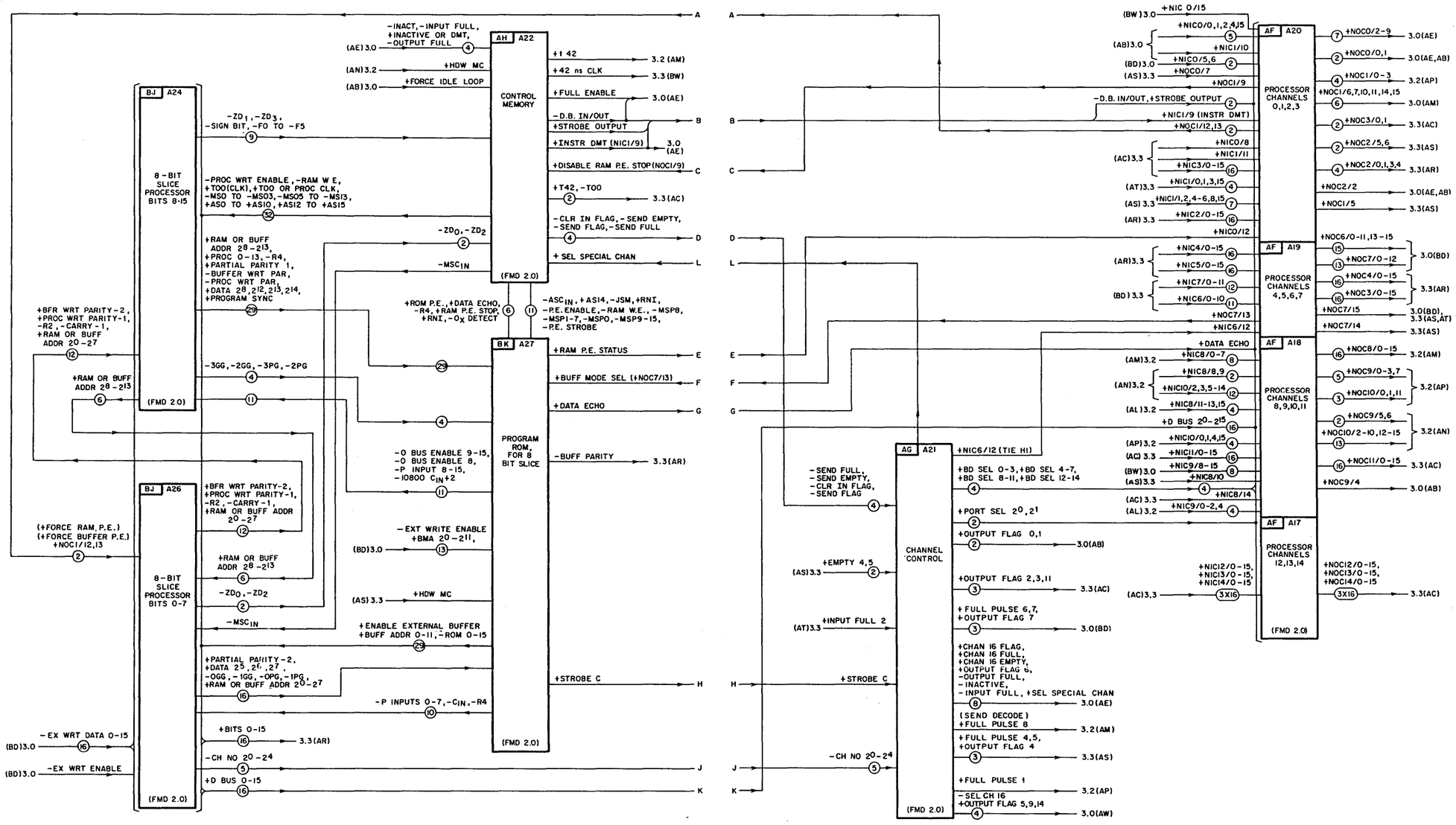
Each of the four 4-bit slice processor paks in the model A controller handles four bits of the 16-bit processor word. The four paks contain the 4-K program RAM, the 2-K buffer memory, and the 10800 and 10803 microprocessor chips.

Each of the 8-bit slice processor paks in the model B controller handles eight bits of the 16-bit processor word. The two paks contain the 4-K program RAM, the 4-K buffer memory, and the 10800 and 10803 microprocessor chips.

The pak at location A27 contains the parity RAM that holds the parity bits for words stored in the program RAM and the buffer memory. It also contains the program ROM which has a capacity of 1024 16-bit words. Program ROM contains an autoload program and some rudimentary diagnostics.

Control memory, at A22, is a ROM with a capacity of 256 60-bit words. Control memory is used primarily for processor channel control and 10800/10803 control.

The processor uses the 15 bidirectional channels at A17, A18, A19, and A20 to control and receive status from the rest of the controller hardware. Output channels are labeled NOCx/xx. For example, NOC1/15 indicates normal output channel 1, bit 15. Input channels are labeled NICx/xx. Channels 0 through 14 are used; channel 15 is not used.


BJ A24
8-BIT SLICE PROCESSOR BITS 8-15
(FMD 2.0)
BJ A26
8-BIT SLICE PROCESSOR BITS 0-7
(FMD 2.0)
AH A22
CONTROL MEMORY
(FMD 2.0)
BK A27
PROGRAM ROM, FOR 8 BIT SLICE
(FMD 2.0)
-INACT, -INPUT FULL, +INACTIVE OR DMT, -OUTPUT FULL
(AE)3.0
(AN)3.2
(AB)3.0
+HDW MC
+FORCE IDLE LOOP
+t 42
+42 ns CLK
+FULL ENABLE
-D.B. IN/OUT
+STROBE OUTPUT
+INSTR DMT (NICI/9)
+DISABLE RAM P.E. STOP (NOCI/9)
+T42, -TOO
-CLR IN FLAG, -SEND EMPTY, -SEND FLAG, -SEND FULL
+ SEL SPECIAL CHAN
-ZD1, -ZD3, -SIGN BIT, -F0 TO -F5
-PROC WRT ENABLE, -RAM W E, +TOO(CLK), +TOO OR PROC CLK, -MS0 TO -MS03, -MS05 TO -MS13, +AS0 TO +AS10, +AS12 TO +AS15
+RAM OR BUFF ADDR 28-213, +PROC 0-13, -R4, +PARTIAL PARITY 1, -BUFFER WRT PAR, -PROC WRT PAR, +DATA 28,212,213,214, +PROGRAM SYNC
-ZD0, -ZD2
-MSCIN
+ROM P.E., +DATA ECHO, -R4, +RAM P.E. STOP, +RNI, -0X DETECT
-ASCIN, +AS14, -JSM, +RNI, -P.E. ENABLE, -RAM W.E., -MSP8, -MSPI-7, -MSP0, -MSP9-15, -P.E. STROBE
+RAM P.E. STATUS
+BUFF MODE SEL (+NOC7/13)
+DATA ECHO
-BUFF PARITY
+STROBE C
+BFR WRT PARITY-2, +PROC WRT PARITY-1, -R2, -CARRY-1, +RAM OR BUFF ADDR 20-27
+RAM OR BUFF ADDR 28-213
-3GG, -2GG, -3PG, -2PG
-O BUS ENABLE 9-15, -O BUS ENABLE 8, -P INPUT 8-15, -I0800 CIN+2
-EXT WRITE ENABLE +BMA 20-211,
(BD)3.0
(AS)3.3
+ENABLE EXTERNAL BUFFER +BUFF ADDR 0-11, -ROM 0-15
+PARTIAL PARITY-2, +DATA 25,26,27, -0GG, -1GG, -0PG, -1PG, +RAM OR BUFF ADDR 20-27
-P INPUTS 0-7, -CIN, -R4
(+FORCE RAM P.E.) (+FORCE BUFFER P.E.) +NOCI/12,13
+BFR WRT PARITY-2, +PROC WRT PARITY-1, -R2, -CARRY-1, +RAM OR BUFF ADDR 20-27
+BITS 0-15
-EX WRT DATA 0-15
-EX WRT ENABLE
-CH NO 20-24
+D BUS 0-15
A
B
C
D
L
E
F
G
H
J
K

MODEL B CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

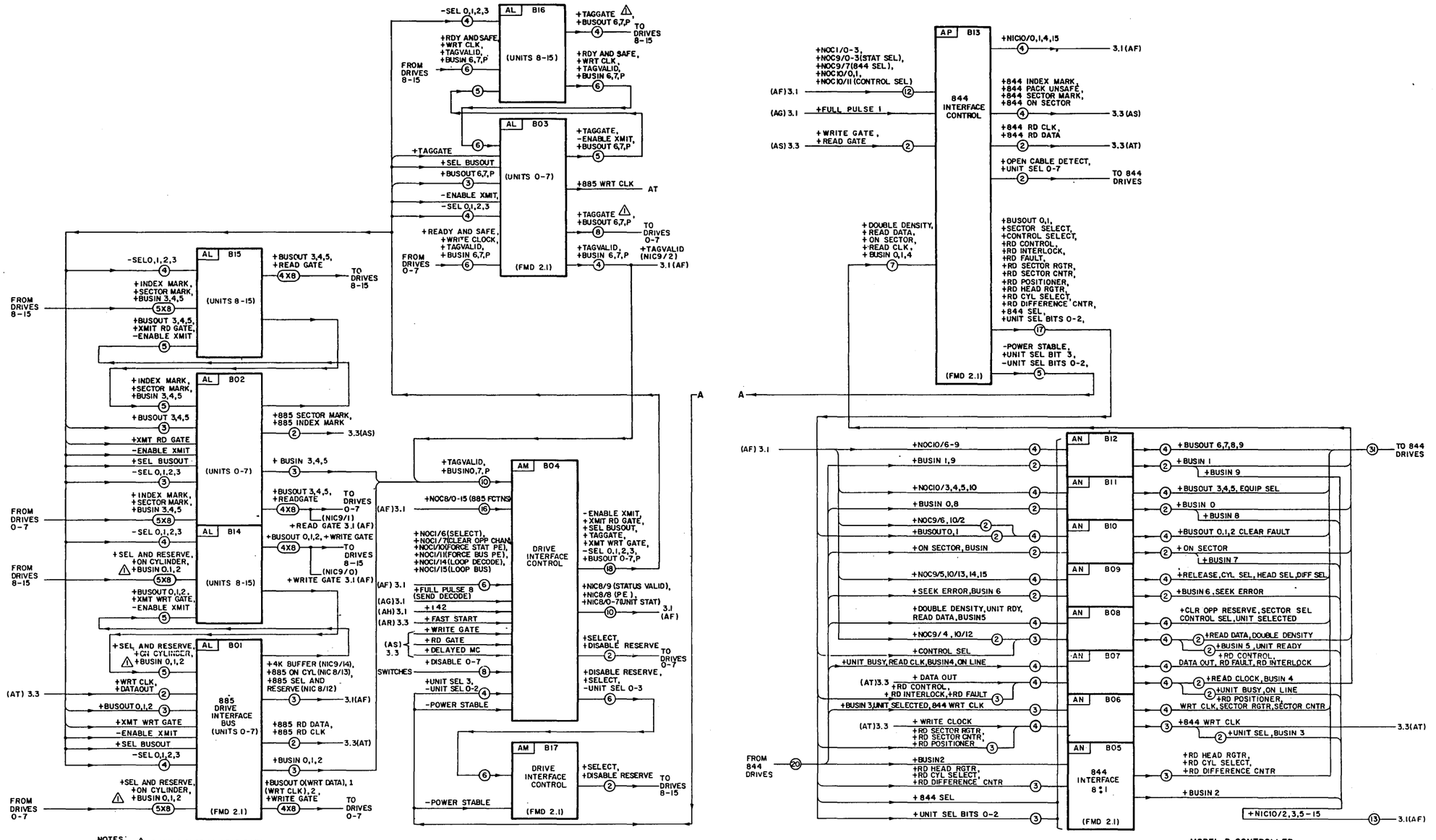
60455690 3.1

INTERCONNECTION BLOCK DIAGRAM 3.2

This diagram shows all signals used in the disk interface section of the controller. 60-paks at chassis locations B01, B02, B03, and B04 provide the interface for 885 drive units 0 through 7. 60-paks at B14, B15, B16, and B17 are part of the Four FMD Option that provides the interface for 885 drive units 8 through 15.

The paks at B05 through B12 are part of the 844 Drive Option that provides the interface for eight 844 disk storage units. The pak at B13 controls this interface.

The paks at B14, B15, B16, and B17 have a parallel function to those at B01, B02, B03, and B04. B14 receives signals from and sends signals to B01. B15/B02, B16/B03 and B17/B04 have the same relationship.



NOTES: ⚠ BUSIN 0 ALSO IS READ DATA.
BUSIN 1 ALSO IS READ CLOCK.
TAG GATE ALSO IS FASTSTART.

MODEL B CONTROLLER
INTERCONNECTION BLOCK DIAGRAM

60455690 3.2

INTERCONNECTION BLOCK DIAGRAM 3.3

This diagram shows all the signals in the data path control section of the controller and the error correction pak. This logic does the following:

Control Word Executing

The control word, sent by the processor from normal output channel 5, controls or initiates some operations in the controller and disk. The control word resides in the control word register at B19 and B20.

The bit count, sent by the processor from normal output channel 4, determines the duration of the control word sequence. The bit count resides in the bit counter at B19 and B20. When the bit counter decrements to zero the control word sequence is completed.

Mark start delay code, formed by NOC5/6 and NOC5/7, delays the start of bit counter decrementing. The delay depends upon the code which may be a sector mark delay, on sector delay, or index mark delay.

Sync Byte Generation/Detection

During a disk write, the controller generates a sync byte at B19 and B20 and NOC5/0 initiates writing sync byte. During a disk read, the controller detects the sync byte at B22 and checks it for correctness at B19 and B20.

Read/Write Control

This section of the controller provides the following part of the write data path.

+Bits 0-15 from processor to B19 and B20
+Data Out from B20 to B22
+Data Out from B22 to B01, B02, or B03 (AL, 3.2)

This section of the controller provides the following part of the read data path.

+Rd Data from B01, B02, or B03 (AL) to B22
-Read Data from B22 to B19
-Deskew 0-15 from B19 to A15 (AD or BD, 3.0)

This section of the controller provides the following part of the buffer memory to PP data path.

-Bits 0-11 from A23 through A26 (AJ, 3.1) to B19 and B20 in the model A controller
-Bits 0-11 from A24 and A26 (BJ, 3.1) to B19 and B20 in the model B controller
+Bfr Data 0-11 to A01, A02, A03, or A04 (AA, 3.0)

The byte counter and compare circuit at B22 work together to gate data into the deskew register at B19 and B20 during a disk read or to gate data into the shift register at B19 and B20 during a disk write. During a read, 12- or 16-bit bytes are assembled in the shift register from serial data. During a write, 12- or 16-bit bytes must be disassembled into serial data. A 12- or 16-bit byte is sent from the holding register at B19 and B20 into the shift register.

Clock Control

Bits 13 and 14 of the control word (selected by NOC5/13, 14) contain a code that selects one of three clocks used to drive sequence control and to provide clock pulses for the bit counter and shift register at AR, and the ECC register at AC. +Clk Select 0 (bit 13) and +Clk Select 1 (bit 14) provide the code on this pak as follows:

Clk Select 1	0	
L	L	Wrt Clk from drive
L	H	Rd Clk from drive
H	L	Processor Clk
H	H	Processor Clk

The clock period for these clocks is as follows:

Processor Clk - 85 ns

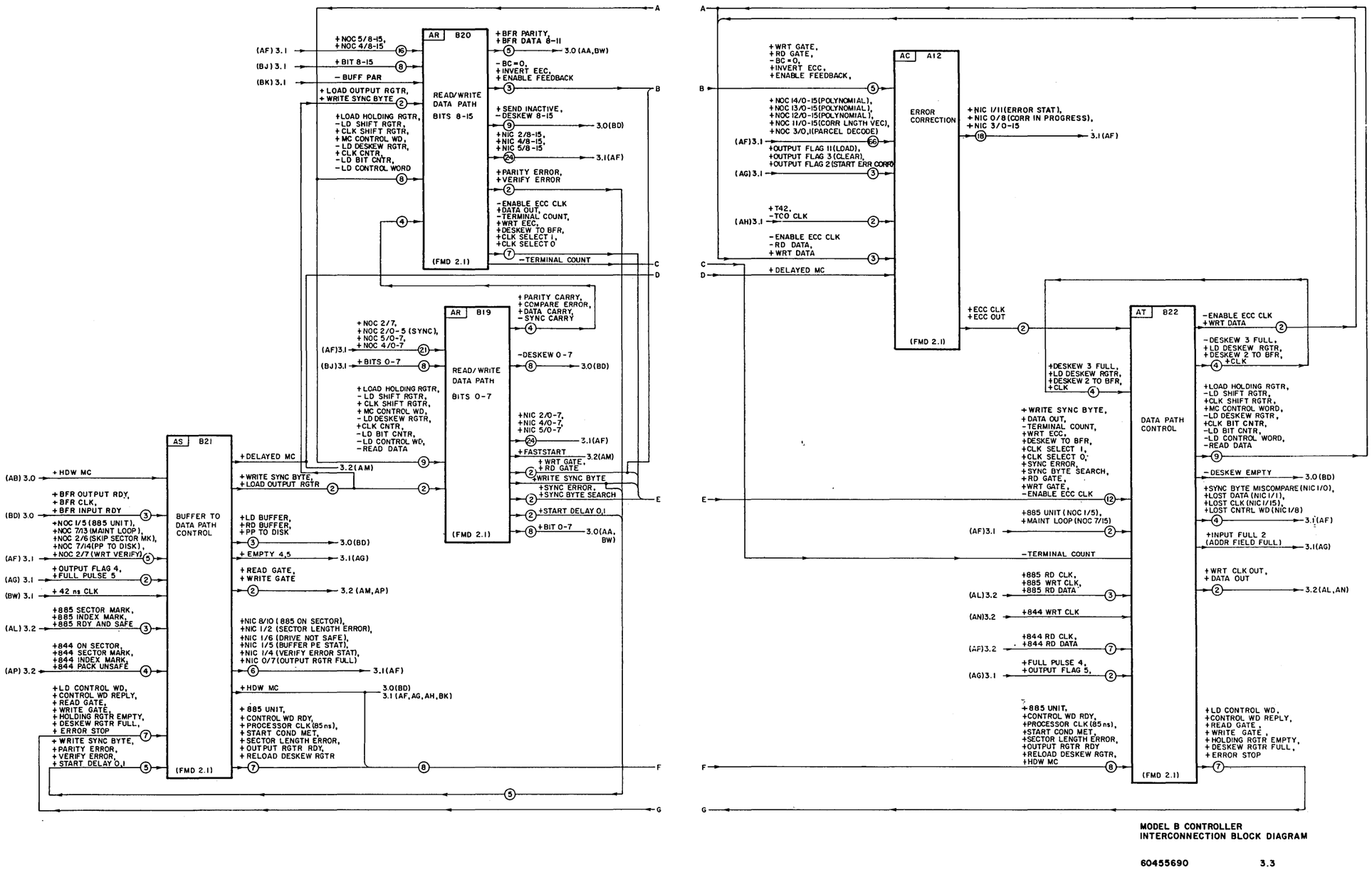
885 Rd or Wrt Clk - 104 ns

844 Rd or Wrt Clk - 144 ns

When the clock selection changes, the clock pulses for the shift register and bit counter are blocked for the next two or three full clock periods.

Error Correction

All read and write data is sent to the error correction pak. A checkword is generated and written at the end of the data record during a write. During a read, the checkword is regenerated and used to determine if there was a data error. If an error is detected, the controller attempts to correct it.


AR B20
READ/WRITE DATA PATH BITS 8-15
(FMD 2.1)
AR B19
READ/WRITE DATA PATH BITS 0-7
(FMD 2.1)
AS B21
BUFFER TO DATA PATH CONTROL
(FMD 2.1)
AC A12
ERROR CORRECTION
(FMD 2.1)
AT B22
DATA PATH CONTROL
(FMD 2.1)
(AF) 3.1
(BJ) 3.1
(BK) 3.1
+NOC 5/8-15, +NOC 4/8-15
+BIT 8-15
– BUFF PAR
+LOAD OUTPUT RGTR, +WRITE SYNC BYTE
+LOAD HOLDING RGTR, –LD SHIFT RGTR, +CLK SHIFT RGTR, +MC CONTROL WD, –LD DESKEW RGTR, +CLK CNTR, –LD BIT CNTR, –LD CONTROL WORD
+BFR PARITY, +BFR DATA 8-11
3.0 (AA,BW)
–BC=0, +INVERT EEC, +ENABLE FEEDBACK
+SEND INACTIVE, –DESKEW 8-15
3.0(BD)
+NIC 2/8-15, +NIC 4/8-15, +NIC 5/8-15
3.1(AF)
+PARITY ERROR, +VERIFY ERROR
–ENABLE ECC CLK, +DATA OUT, –TERMINAL COUNT, +WRT EEC, +DESKEW TO BFR, +CLK SELECT 1, +CLK SELECT 0
–TERMINAL COUNT
+PARITY CARRY, +COMPARE ERROR, +DATA CARRY, –SYNC CARRY
+NOC 2/7, +NOC 2/0-5 (SYNC), +NOC 5/0-7, +NOC 4/0-7
(AF)3.1
(BJ)3.1
+BITS 0-7
–DESKEW 0-7
3.0(BD)
+LOAD HOLDING RGTR, –LD SHIFT RGTR, +CLK SHIFT RGTR, +MC CONTROL WD, –LD DESKEW RGTR, +CLK CNTR, –LD BIT CNTR, –LD CONTROL WD, –READ DATA
+NIC 2/0-7, +NIC 4/0-7, +NIC 5/0-7
3.1(AF)
+FASTSTART
3.2(AM)
+WRT GATE, +RD GATE
+WRITE SYNC BYTE
+SYNC ERROR, +SYNC BYTE SEARCH
+START DELAY 0,1
+BIT 0-7
3.0(AA, BW)
(AB) 3.0
(BD) 3.0
(AF) 3.1
(AG) 3.1
(BW) 3.1
(AL) 3.2
(AP) 3.2
+HDW MC
+BFR OUTPUT RDY, +BFR CLK, +BFR INPUT RDY
+NOC 1/5 (885 UNIT), +NOC 7/13 (MAINT LOOP), +NOC 2/6 (SKIP SECTOR MK), +NOC 7/14 (PP TO DISK), +NOC 2/7 (WRT VERIFY)
+OUTPUT FLAG 4, +FULL PULSE 5
+42 ns CLK
+885 SECTOR MARK, +885 INDEX MARK, +885 RDY AND SAFE
+844 ON SECTOR, +844 SECTOR MARK, +844 INDEX MARK, +844 PACK UNSAFE
+LD CONTROL WD, +CONTROL WD REPLY, +READ GATE, +WRITE GATE, +HOLDING RGTR EMPTY, +DESKEW RGTR FULL, +ERROR STOP
+WRITE SYNC BYTE, +PARITY ERROR, +VERIFY ERROR, +START DELAY 0,1
+DELAYED MC
3.2(AM)
+WRITE SYNC BYTE, +LOAD OUTPUT RGTR
+LD BUFFER, +RD BUFFER, +PP TO DISK
3.0(BD)
+EMPTY 4,5
3.1(AG)
+READ GATE, +WRITE GATE
3.2 (AM,AP)
+NIC 8/10 (885 ON SECTOR), +NIC 1/2 (SECTOR LENGTH ERROR), +NIC 1/6 (DRIVE NOT SAFE), +NIC 1/5 (BUFFER PE STAT), +NIC 1/4 (VERIFY ERROR STAT), +NIC 0/7 (OUTPUT RGTR FULL)
3.1(AF)
+HDW MC
3.0(BD) 3.1 (AF,AG,AH,BK)
+885 UNIT, +CONTROL WD RDY, +PROCESSOR CLK (85 ns), +START COND MET, +SECTOR LENGTH ERROR, +OUTPUT RGTR RDY, +RELOAD DESKEW RGTR
+WRT GATE, +RD GATE, –BC=0, +INVERT ECC, +ENABLE FEEDBACK,
+NOC 14/0-15 (POLYNOMIAL), +NOC 13/0-15 (POLYNOMIAL), +NOC 12/0-15 (POLYNOMIAL), +NOC 11/0-15 (CORR LNGTH VEC), +NOC 3/0,1 (PARCEL DECODE)
+OUTPUT FLAG 11 (LOAD), +OUTPUT FLAG 3 (CLEAR), +OUTPUT FLAG 2 (START ERR CORR)
+T42, –TCO CLK
–ENABLE ECC CLK, –RD DATA, +WRT DATA
+DELAYED MC
+NIC 1/11 (ERROR STAT), +NIC 0/8 (CORR IN PROGRESS), +NIC 3/0-15
3.1 (AF)
+ECC CLK, +ECC OUT
+DESKEW 3 FULL, +LD DESKEW RGTR, +DESKEW 2 TO BFR, +CLK
+WRITE SYNC BYTE, +DATA OUT, –TERMINAL COUNT, +WRT EEC, +DESKEW TO BFR, +CLK SELECT 1, +CLK SELECT 0, +SYNC ERROR, +SYNC BYTE SEARCH, +RD GATE, +WRT GATE, –ENABLE ECC CLK
+885 UNIT (NOC 1/5), +MAINT LOOP (NOC 7/15)
–TERMINAL COUNT
+885 RD CLK, +885 WRT CLK, +885 RD DATA
+844 WRT CLK
+844 RD CLK, +844 RD DATA
+FULL PULSE 4, +OUTPUT FLAG 5,
+885 UNIT, +CONTROL WD RDY, +PROCESSOR CLK (85 ns), +START COND MET, +SECTOR LENGTH ERROR, +OUTPUT RGTR RDY, +RELOAD DESKEW RGTR, +HDW MC
–ENABLE ECC CLK, +WRT DATA
–DESKEW 3 FULL, +LD DESKEW RGTR, +DESKEW 2 TO BFR, +CLK
+LOAD HOLDING RGTR, –LD SHIFT RGTR, +CLK SHIFT RGTR, +MC CONTROL WORD, –LD DESKEW RGTR, +CLK BIT CNTR, –LD BIT CNTR, –LD CONTROL WORD, –READ DATA
–DESKEW EMPTY
3.0(BD)
+SYNC BYTE MISCOMPARE (NIC 1/0), +LOST DATA (NIC 1/1), +LOST CLK (NIC 1/15), +LOST CNTRL WD (NIC 1/8)
3.1(AF)
+INPUT FULL 2 (ADDR FIELD FULL)
3.1(AG)
+WRT CLK OUT, +DATA OUT
3.2(AL,AN)
+LD CONTROL WD, +CONTROL WD REPLY, +READ GATE, +WRITE GATE, +HOLDING RGTR EMPTY, +DESKEW RGTR FULL, +ERROR STOP
A
B
C
D
E
F
G

MODEL B CONTROLLER INTERCONNECTION BLOCK DIAGRAM

60455690 3.3

CONSOLIDATED LOGIC DIAGRAMS

	A	B
27	PROGRAM ROM, PARITY 22939170 TYPE:AK	
26	4 BIT SLICE PROCESSOR BITS 0-3 22932929 TYPE:AJ	
25	4 BIT SLICE PROCESSOR BITS 4-7 22932929 TYPE:AJ	
24	4 BIT SLICE PROCESSOR BITS 8-11 22932929 TYPE:AJ	
23	4 BIT SLICE PROCESSOR BITS 12-15 22932929 TYPE:AJ	
22	CONTROL MEMORY 53561078 TYPE:AH	DATA PATH CONTROL 11899014 TYPE:AT
21	CHANNEL CONTROL 11896398 TYPE:AG	BUFFER TO DATA PATH CONTROL 11899010 TYPE:AS
20	PROCESSOR CHANNELS 0-3 22934533 TYPE:AF	READ/WRITE DATA PATH 11896751 TYPE:AR
19	PROCESSOR CHANNELS 4-7 22934533 TYPE:AF	READ/WRITE DATA PATH 11896751 TYPE:AR
18	PROCESSOR CHANNELS 8-11 22934533 TYPE:AF	
17	PROCESSOR CHANNELS 12-15 22934533 TYPE:AF	DRIVE INTERFACE CONTROL (FOUR FMD OPTION) 22938728 TYPE:AM
16	SPECIAL CYBER CHANNEL 11896752 TYPE:AE	DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
15	BUFFER CONTROL 11897694 TYPE:AD	DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
14		DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
13		844 INTERFACE CONTROL 11899080 TYPE:AP
12	ERROR CORRECTION 11897798 TYPE:AC	844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
11		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
10		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
9		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
8	CYBER CHANNEL MUX 22936328 TYPE:AB	844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
7		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
6		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
5		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
4	CHANNEL R/T D (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE CONTROL 22938728 TYPE:AM
3	CHANNEL R/T C (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE BUS 22939189 TYPE:AL
2	CHANNEL R/T B (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE BUS 22939189 TYPE:AL
1	CHANNEL R/T A 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE BUS 22939189 TYPE:AL

NOTES:
1. THE FOUR FMD OPTION INCLUDES FOUR 60-PAKS AT LOCATIONS B14 THROUGH B17. THE 844 DRIVE OPTION INCLUDES EIGHT 60-PAKS AT LOCATIONS B5 THROUGH B12.

	CONTROL DATA CORPORATION / DEVELOPMENT DIVISION	CARD PLACEMENT MODEL A CONTROLLER (WITH OPTIONS)	CODE IDENT 34010	DWG NO 60455690	REV W
			SIZE C	SHEET	PAGE

	A	B
27	PROGRAM ROM FOR 8-BIT SLICE 53371068 TYPE.BK	
26	8 BIT SLICE PROCESSOR 0-7 53371069 TYPE.BJ	
25		
24	8 BIT SLICE PROCESSOR 8-15 53371069 TYPE:BJ	
23		
22	CONTROL MEMORY 53561078 TYPE:AH	DATA PATH CONTROL 11899014 TYPE:AT
21	CHANNEL CONTROL 11896398 TYPE:AG	BUFFER TO DATA PATH CONTROL 11899010 TYPE:AS
20	PROCESSOR CHANNELS 0-3 22934533 TYPE:AF	READ/WRITE DATA PATH 11896751 TYPE:AR
19	PROCESSOR CHANNELS 4-7 22934533 TYPE:AF	READ/WRITE DATA PATH 11896751 TYPE:AR
18	PROCESSOR CHANNELS 8-11 22934533 TYPE:AF	
17	PROCESSOR CHANNELS 12-15 22934533 TYPE:AF	DRIVE INTERFACE CONTROL (FOUR FMD OPTION) 22938728 TYPE:AM
16	SPECIAL CYBER CHANNEL 11896752 TYPE:AE	DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
15	BUFFER CONTROL 53560926 TYPE:BD	DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
14		DRIVE INTERFACE BUS (FOUR FMD OPTION) 22939189 TYPE:AL
13		844 INTERFACE CONTROL 11899080 TYPE:AP
12	ERROR CORRECTION 11897798 TYPE:AC	844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
11		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
10		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
9		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
8	CYBER CHANNEL MUX 22936328 TYPE:AB	844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
7	CYBER MUX 2 52681539 TYPE:BW	844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
6		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
5		844 INTERFACE 8:1 (844 DRIVE OPTION) 11899094 TYPE:AN
4	CHANNEL R/T D (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE CONTROL 22938728 TYPE:AM
3	CHANNEL R/T C (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE.AA	DRIVE INTERFACE BUS 22939189 TYPE:AL
2	CHANNEL R/T B (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE BUS 22939189 TYPE:AL
1	CHANNEL R/T A (CHANNEL ACCESS OPTION) 10353699 OR 21946254 OR 22109748 TYPE:AA	DRIVE INTERFACE BUS 22939189 TYPE:AL

NOTES:
1. THE FOUR FMD OPTION INCLUDES FOUR 60-PAKS AT LOCATIONS B14 THROUGH B17. THE 844 DRIVE OPTION INCLUDES EIGHT 60-PAKS AT LOCATIONS B5 THROUGH B12.

	CONTROL DATA CORPORATION / DEVELOPMENT DIVISION	CARD PLACEMENT MODEL B CONTROLLER (WITH OPTIONS)	CODE IDENT 34010	DWG NO 60455690	REV W
			SIZE C	SHEET	PAGE

CHANNEL RECEIVERS/TRANSMITTERS (A01, A02, A03, A04, AA)

This pak receives 21 signals from the PP. Nineteen go to the catch register. 1 MHz Clock signal is not used. The controller uses 10 MHz Clock signal to generate internal clock pulses to synchronize controller with the PP channel. Each data byte and parity bit is held in the holding register.

Transmitters send 16 signals to the PP. The 12-bit data bytes plus parity come from either the microprocessor special channel (+MP Data 0-11 signals) or the buffer memory (+Bfr Data 0-11 signals).

The four channel accesses designated channel access A, channel access B, channel access C, and channel access D correspond respectively to locations A01 (A), A02 (B), A03 (C), and A04 (D).

The model A controller contains an R/I pak at A01 to terminate the +Bfr Data signals. The Channel Access Options add channels B, C, and D with paks at locations A02, A03, and A04, respectively.

The model B controller does not include a channel access. The Channel Access Options provide for channels A, B, C, and D in locations A01, A02, A03, and A04, respectively. The +Bfr Data 0-11 signals are terminated at location A07.

Each channel access can be disabled by positioning the appropriate PP CHANNEL ENABLE/DISABLE switch located above the front of the chassis. Parity on a channel can be enabled or disabled by positioning the appropriate switch on the 60-pak at location A08 (AB).

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

+DATA 0-11
+PARITY
+FULL
+EMPTY
+ACTIVE
+INACTIVE
+FUNCTION
+MASTER CLEAR
+1 MHz CLOCK
+10 MHz CLOCK

PP CHANNEL A,B,C, OR D
PP OUTPUT
+10 MHz CLK
1 (3)
10B"
1 (2)
10 MHz
PULSE GENERATOR
1G
APPROX. 400 MHz (2)
+T03,+T27,+T51,+T75
+T15,+T39,+T63,+T87
+EMPTY
+FULL
AB
+1 MHz CLOCK
NU
+MASTER CLEAR, +FUNCTION, +INACTIVE, +ACTIVE, +EMPTY, +FULL, +PARITY, +DATA 2^0-2^{11}
CATCH REGISTER
CD 10175 C R (3)
+DATA 0-11, +PARITY
HOLDING REGISTER
CD 10176 C (3)
+DATA 2^0-2^{11}, PARITY
DELAY
.15 NS (2)
+CLK T06
+T18
NC
-T42
-T54
+T66
-T66
+CHANNEL CLK(T78)
-T78
FULL
8 (2)
AE
AD(BD)
+MP INACTIVE
+BFR INACTIVE
+CONNECT
8 1 8 (2)
+ACTIVE, +EMPTY
+FULL
+FUNCTION
1 (1) 8 (2)
+MC
+INACTIVE
1 10109 (1)
AE
+CLEAR CHANNEL
+DISABLE CHANNEL SWITCH
8 10105 (1)
AB(BW)
FUNCTION
S 10131 R (1)
+CHANNEL FCTN STAT
ACTIVE
+ACTIVE STAT
FULL
CD (1)
+FULL STAT
+FUNC
+ACTIVE
AE
AD(BD)
+MP EMPTY
+BFR EMPTY
8 1 8 (2)
AB
+CONNECT
AD(BD)
+BFR FULL
8 10104 (2)
8 10101 (2)
AE
+MP FULL
AR
+BFR FULL
+EMPTY
+INACTIVE
X÷Y 10192 F HIGH PULSE LO PULSE (2)
+FULL, +EMPTY, +INACTIVE
PP INPUT
NC +ACTIVE
+PARITY
+DATA 0-11
AE
+MP PARITY
AR
+BFR PARITY
AE
+MP DATA 2^0-2^{11}
AR
+BFR DATA 0-11
8 1 8 (2)
8 1 8 (4)
X÷Y 10192 F HIGH PULSE LO PULSE (4)

NOTES:

⚠

F INPUT	F OUTPUT
HI	
LO	±50NS

⚠ +:
−:

TXX : XX= LEADING EDGE TIME IN NANOSECONDS.

3. A01 — CHANNEL A
   A02 — CHANNEL B
   A03 — CHANNEL C
   A04 — CHANNEL D
4. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM CHANNEL RECEIVERS / TRANSMITTERS	CODE IDENT 34010	D	DWG NO 60455690	REV R
	TYPE AA LOC (A01,A02,A03,A04)			SHEET 5-31	

CYBER CHANNEL MUX (A08, AB)

This pak multiplexes the signals from the PP channel accesses at either the DATA CHAN MUX or NIC SELECT multiplexer. Data from the DATA CHAN MUX is checked for parity errors and for an autoload function.

Four switches on the pak enable or disable parity checking and generation on the respective channel. If a parity error is detected, LED 1 lights.

An autoload function (0414_8 or $01XX_8$) sent by the PP causes the controller to execute the autoload program in the ROM. If this occurs, LED 3 lights.

DEADMAN TIMEOUT

This condition occurs if a PP activated the controller but no full or empty signals are exchanged on the channel for 4.5+1.5 s. Deadman timeout stops the controller, sets NIC0/4, and lights LED 2.

The free-running oscillator causes the counter chip to increment when a +Active signal has enabled the circuit. A +Full, +Empty, or +Inactive signal resets the counter.

MASTER CLEAR

The controller is cleared by pushbutton master clear, power on master clear, channel (PP) master clear, autoload, or NOC1 flag (generated by the microprocessor).

CONNECT

A PP access can connect and reserve the controller if the controller is not connected. The PP connects the controller by sending any function. The scanner, running off the microprocessor clock, enables the connect and prevents ties if the controller receives PP functions simultaneously from different accesses. Connect lights one of the LEDs on the pak and sets a normal input channel bit (NIC0/0). Output flag pulse 0 or autoload clears the connect condition.

NIC MUX

Most signals from this multiplexer go to the special channel (channel 16) at location A16 (AE). Channel 16 is dedicated to communication between the PPs and the controller microprocessor. +SCC 0-11 signals go to channel 16. +Buff Mem 0-11 signals go to buffer memory at A23, A24, A25, and A26 (AJ) in the model A controller or A24 and A26 (BJ) in the model B controller.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

OSCILLATOR
333 ns
+ACTIVE
DEADMAN TIMER
4.8 SEC ±10%
+DEADMAN TIMEOUT
AD(BD)
DMT
+(NIC 0/4) +DEADMAN TIMEOUT
AE, AF
DMT ENABLE
+MC
+MPCLK
LED 2 DMT
+μPCLK
+INACTIVE
+EMPTY
+EMPTY
+FULL PULSE
+INACTIVE REG
+178
DATA CHAN MUX
+ACTIVE
+FUNCTION STAT
FCN STAT
LED 3 AUTOLOAD
CHANNELS A,B,C,D
+MC, +CLK 106
±DATA 2^0-2^{11} PARITY
+FULL, +EMPTY, +ACTIVE STAT
+FCNSTAT
+CLK 178 (50 ns)
+DATA 2^0-2^{11}, P
+FULL
+MC
+106
+178
+EMPTY
+106
+DATA
AA
+FCN
+MC
$+2^0,2^1,2^4,2^7,2^9,2^{11}$
$+2^2,2^3,2^8$
$+2^7,2^{11}$
$+2^6$
$04!4_8$
$01XX_8$
AUTOLOAD
PARITY ENABLE SWITCHES
SO1-(ACCESS A)
SO2-(ACCESS B)
SO3-(ACCESS C)
SO4-(ACCESS D)
OFF ON
+MC
+ACTIVE
+PAR ENABLE
+PARITY BIT
CHECK PARITY
+MC
+ACTIVE
+PAR ENABLE
+ENABLE PARITY
+PARITY ERROR
+ACCESS CODE
NOCO/1
NOCO/0
AF(BW)
AF(BW)
+RESERVED
-BD. SEL
AD(BD)
AG(BW)
(NIC1/10)
+CHANNEL PARITY ERROR
AF
LED 1 PARITY ERROR
(NICO/13)
+CONN PAR ENABLE
AF
+SCC PARITY ENABLE
+PARITY BIT
SO4
SO3
SO2
SO1
+DATA 2^0-2^{11}
+PARITY
+ACTIVE
+FCNSTAT
+DATA
+BUFF MEM 0-11
+SCCO-11
AD(BD)
+CONNECT (NICO/O)
+FUNCTION (NICO/1)
+SCC FULL
+CLOCK (T80)
AE
AF
AF
AE
AE
(NICO/2)
+NIC PE
AF
NIC SELECT
CHANNELS A,B,C,D
+FULL STAT
+CLK 178 (25 ns)
+DATA 2^0-2^{11},P,
+ACTIVE, +FCN STAT,
+FULL STAT,
+CLK 178, +CONNECT
AA
+ACTIVE
+SCC INACTIVE
AE
+CONNECT
+BCONN
+DCONN
+CCONN
-2^0
-2^1
NC(BW)
NC(BW)
1.3μ SEC FL
+HDW MC
AS
+FORCE IDLE LOOP
AH
+MC
CHAN MC
+PMC
+CHAN MC
+AUTOLD
-ANY CH CONNECTED
SCANNER(7)
1 FCN A,B,C,OR D
AJ(BJ)
+MC (PUSHBUTTON)
POMC (6)
MC1
+MC
AE(BW)
CLOCK
85 ns
-μPCLOCK
AD(NC)
+μPCLOCK
42 ns PERIOD
AS(BW)
ENABLE MUX
SCAN D
SCAN C
SCAN B
SCAN A
RESET
CONNECT
+CONNECT A-D
AA
LED 4 - CONN A
LED 5 - CONN B
LED 6 - CONN C
LED 7 - CONN D
AG
+OUTPUT FLAG 0 (μPRELEASE)
+OUTPUT FLAG 1
+PUSHBUTTON MC
MP MC
AUTOLOAD
EXTEND MC
16CNTR

NOTES:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM CYBER CHANNEL MUX	CODE IDENT 34010	D	DWG NO 60455690	REV R
	TYPE: AB LOC: A08			SHEET 5-33	

ERROR CORRECTION (A12, AC)

This pak has a 48-bit checkword generator used to detect and correct errors on data read from a disk. All 48 bits of the generator are used with 885 disks, but only 32 bits are used with 844 disks. During a write, this circuit generates a 48- or 32-bit checkword that is written on the disk at the end of the data field. During a read, data and the checkword are sent back through the generator. If the contents of the generator is zero at the end of the read, then no error was detected. If the generator does not equal zero, then the processor can determine if the error is correctable and correct it if possible.

To generate the checkword, the processor must load a 32- or 48-bit polynomial into output channels 12, 13, and 14 (844 uses NOC13 and 14 only). +Output Flag 11 signal gates the polynomial into the generator which performs an exclusive OR operation with the polynomial bits and the shift register bits. When the data has been written, the error correction checkword (ECC) is sent to B22 (AT) as +ECC Out signal.

When reading data from the disk, the data and checkword are sent through the shift register and an exclusive OR is performed with the polynomial from NOC12, 13, and 14. The processor reads the contents of the register from NIC3. If the register is all zeros, then no error was detected. If it is not all zeros, the processor must determine whether the error can be corrected and, if it can be, where the error is located in the buffer.

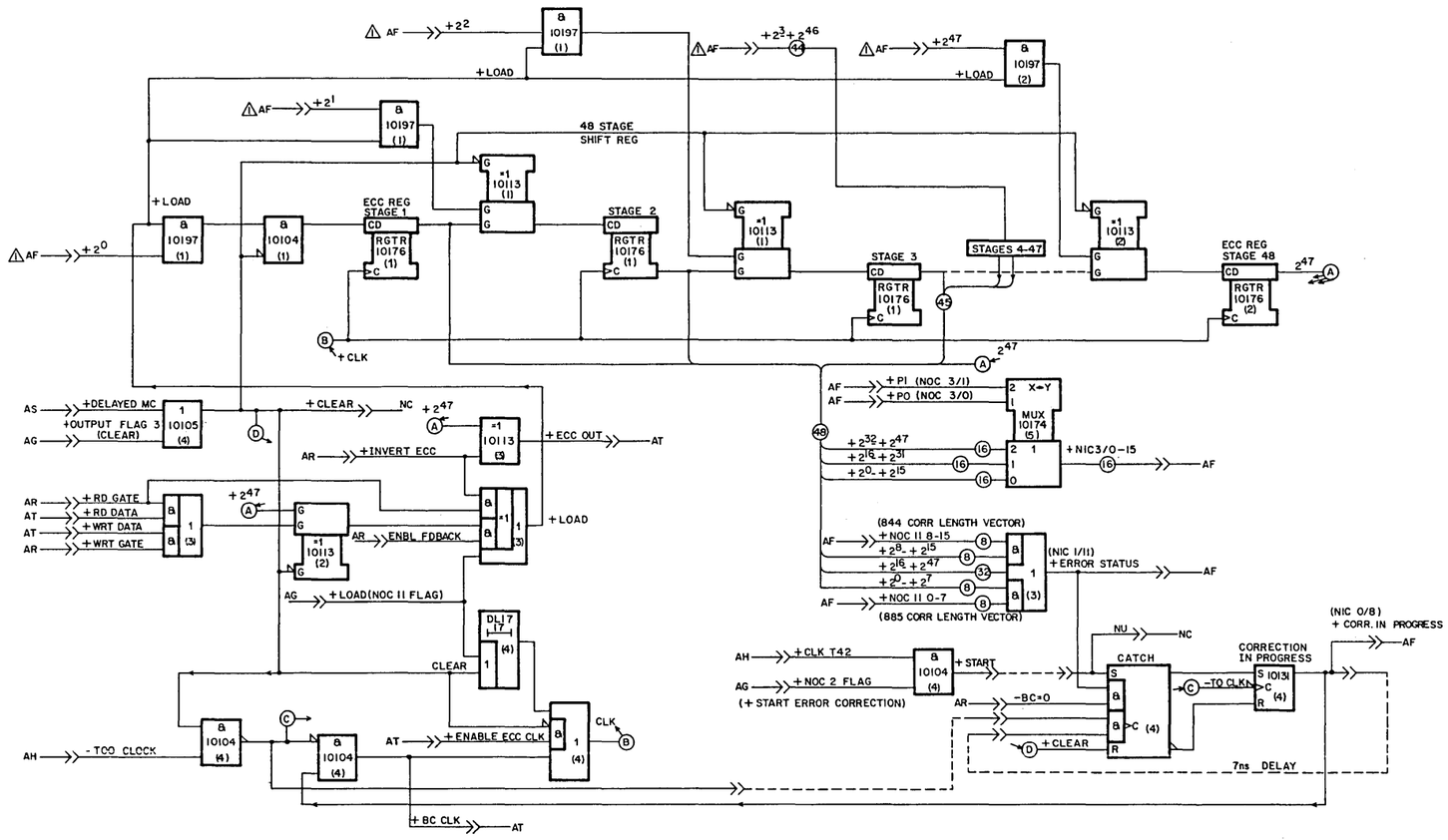
An error is correctable if it is an error burst of 8 bits or less. To determine whether it is correctable or not, the processor inputs the 32- or 48-bit byte in the shift register from NIC3. The bit order of parcels 1 (885 only), 2, and 3 is reversed. Then parcel 1 (885) or parcel 2 (844) is sent back to the shift register on NOC14, parcel 2 (885) or parcel 3 (844) is sent on NOC13, and parcel 3 (885 only) is sent on NOC12. The reversed syndrome is loaded with +Output Flag 11 signal. Next, the decode polynomial is loaded from NOC12, 13, and 14. Then the contents of the register is shifted and an exclusive OR is performed with the decode polynomial. This is done the number of times equal to the number of bits in the data field plus the number of bits in the ECC, or until the register comes up all zeros. If the syndrome shifts but does not come up all zeros, then the error is uncorrectable. This sets NIC1/11.

This sequence is initiated by +Output Flag 2 signal. NIC0/8, correction in progress, sets during this sequence.

If the error is uncorrectable, then the operation can be terminated. If it can be corrected, the processor must determine the address (in the buffer memory) of the error burst. It does this by checking NIC4, bit count status. NIC4 indicates the number of shifts that have occurred to get a zero count. The processor then sets the correction vector NOC11/0-7 for 885 or NOC11/8-15 for 844, and then performs exclusive OR of the correction vector with buffer data beginning at the address indicated by NIC4.

If two or more error bursts that are less than 8 bits long occur in a data field, the uncorrectable error status bit sets.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



NOTES

⚠ THE 48 BITS SENT TO THE SHIFT REGISTER COME FROM NOC 12 (POLYNOMIAL PARCEL I), NOC 13 (PARCEL II), AND NOC 14 (PARCEL III).

CONTROL DATA	CONSOLIDATED LOGIC DIAGRAM ERROR CORRECTION	CODE IDENT		DWG NO	REV
ARDEN HILLS OPERATIONS	TYPE: AC LOC: (A12)	34010	D	60455690	R
			SHEET	5-35	

BUFFER CONTROL (A15, AD) - Model A Controller

BUFFER CONTROL (A15, BD) - Model B Controller

This pak controls data transfers into and out of the buffer memory. In the model A controller, the buffer memory has a capacity of 2048 16-bit words, and is located at A23, A24, A25, and A26 (AJ). In the model B controller, the buffer memory holds 4096 16-bit words at locations A24 and A26 (BJ). NIC 9/4 indicates that the buffer memory is 4-K.

Buffer control deals with four data transfer paths - PP to disk operation buffer write, PP to disk operation buffer read, disk to PP operation buffer write, and disk to PP operation buffer read.

Before any buffer memory data transfer, the up/down counter must be loaded by the processor from normal output channel 7, bits 0 through 11. Whenever a word is written into the memory, this counter increments; whenever a word is read from the memory, the counter decrements. If the counter decrements to zero, the buffer read terminates to prevent attempting to read more data than has been written. NIC1/7 reflects the zero or nonzero state of the counter.

The processor loads the write address counter from normal output channel 6 before starting a buffer memory write operation. The counter provides the buffer memory address during a write and is incremented by 1 after each byte has been written.

The processor loads the read address counter from normal output channel 6 before starting a buffer memory read operation. The counter provides the buffer memory address during a read and is incremented by 1 after each byte has been read.

The sequence of events for buffer read and buffer write operations (as they pertain to this pak) follow.

PP TO DISK

The sequence of events for a buffer write:

1. Processor must establish initial conditions:
   a. Output flag 7 sets reserved flip-flop.
   b. Load write address and up/down counters.
   c. Set PP to disk bit (NOC7/14) and set disable processor to buffer bit (NOC7/13).
   d. Clear load bit (NOC6/15).
2. PP sends Full signal that sets Full Catch flip-flop.
3. Send Empty flip-flop sets at -T2. This resets Full Catch flip-flop and generates a +Bfr Empty signal. A +Bfr Empty signal causes a +Empty signal to be returned to the connected PP in response to the Full signal from the PP.
4. Catching Reg Full flip-flop sets at +T1. This resets the +Send Empty flip-flop, sets the Write Enable flip-flop, and enables +Buff Mem 0-11 signals data byte into the catching register.
5. Up/down counter and write address counter increment.

Steps 2 through 5 repeat until the PP completes the data transfer.

The sequence of events for a buffer read:

1. Same as step 1 for buffer write except that the read address counter must be loaded.
2. Enable Output Rgtr flip-flop sets, allowing the read address counter to increment and the up/down counter to decrement at +T1.
3. Output Reg Full flip-flop sets generating a +Buffer Output Rdy signal. This resets the Enable Output Rgtr flip-flop.
4. Read Buffer flip-flop sets, indicating that the output register at B19 and B20 (AR) can accept another data byte. This resets the Output Reg Full flip-flop.

Steps 2 through 4 repeat until the operation finishes.

DISK TO PP

The sequence of events for a buffer write:

1. Processor must establish initial conditions:
   a. NOC7/14 must be clear to select the disk-to-PP path.
   b. Processor loads write address and up/down counters.
2. Load Buffer flip-flop sets, indicating that the buffer input register (at AJ or BJ) can receive data.
3. Catching Reg Full sets, gating -Deskew 0-15 signals into the catching register.
4. Write Enable flip-flop sets.
5. Buffer Input Rdy flip-flop sets.
6. Write address counter increments and Catching Reg Full flip-flop resets.

Steps 2 through 6 repeat until the processor terminates the operation.

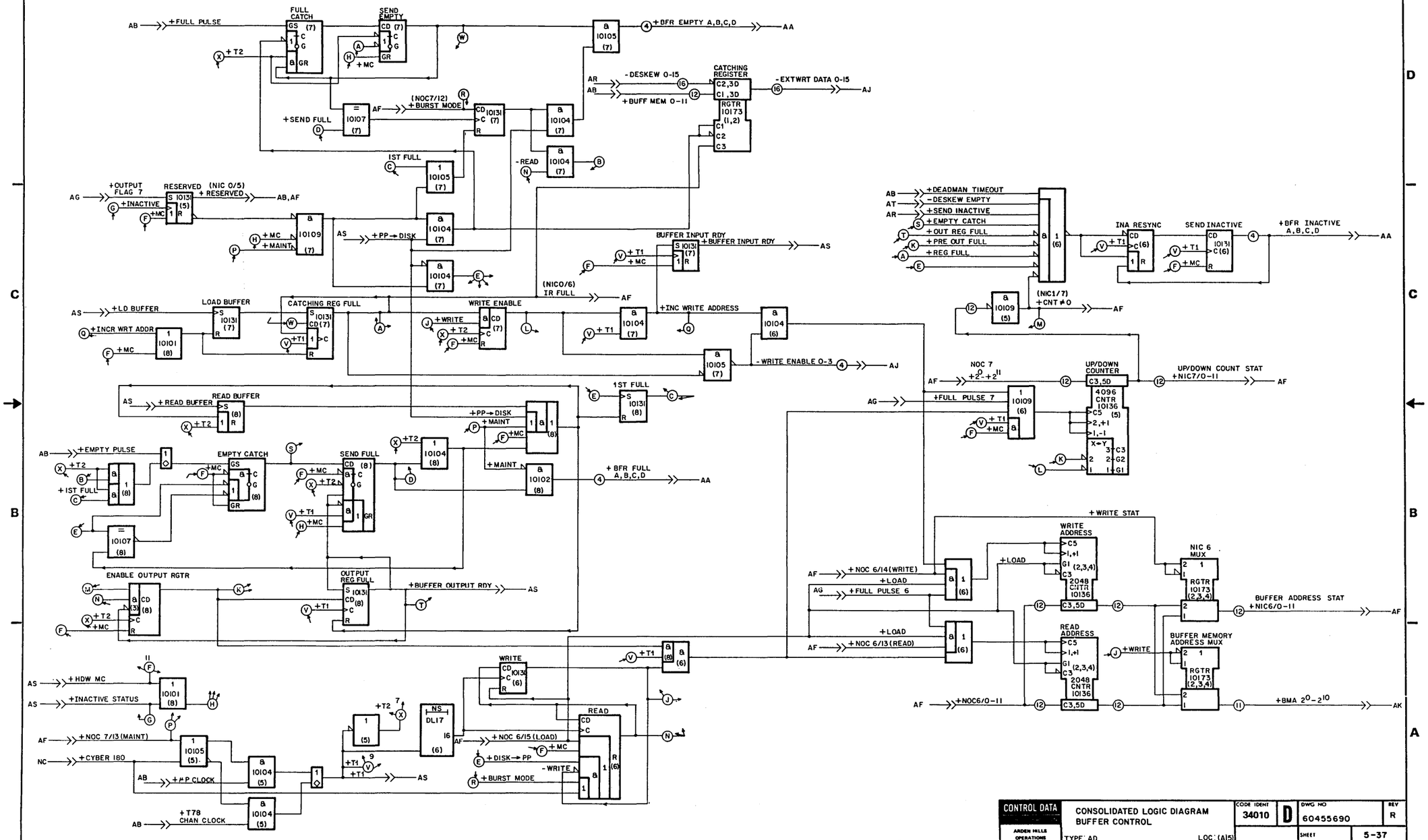
The sequence of events for a buffer read:

1. Same as step 1 for buffer write except read address counter must be loaded.
2. 1st Full flip-flop sets.
3. Empty Catch flip-flop sets.
4. Send Full flip-flop sets.
5. Enable Output Rgtr flip-flop sets.

6. Read address counter increments and up/down counter decrements.
7. +Out Reg Full signal sets. This resets Enable Output Rgtr flip-flop.
8. Buffer Output Rdy signal enables loading the output.
9. Register at B19 and B20 (AR) is loaded.
10. Read Buffer flip-flop sets. This resets 1st Full and Output Reg Full flip-flops.
11. Full data sent to PP.
12. PP sends empty pulse. This sets (indirectly) Empty Catch flip-flop.

Steps 4 through 12 repeat until the PP or processor terminates the operation.

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHKD	APP



CONTROL DATA	CONSOLIDATED LOGIC DIAGRAM BUFFER CONTROL	CODE IDENT 34010	D	DWG NO 60455690	REV R
ARDEN HILLS OPERATIONS	TYPE: AD LOC: (A15)			SHEET 5-37	

SPECIAL CYBER CHANNEL (CHANNEL 16) (A16, AE)

This pak controls the special CDC CYBER channel (also referred to as channel 16), which is a bidirectional channel between the PP and processor. The processor selects the channel and the PP channel access with NOCO/0,1 as indicated below.

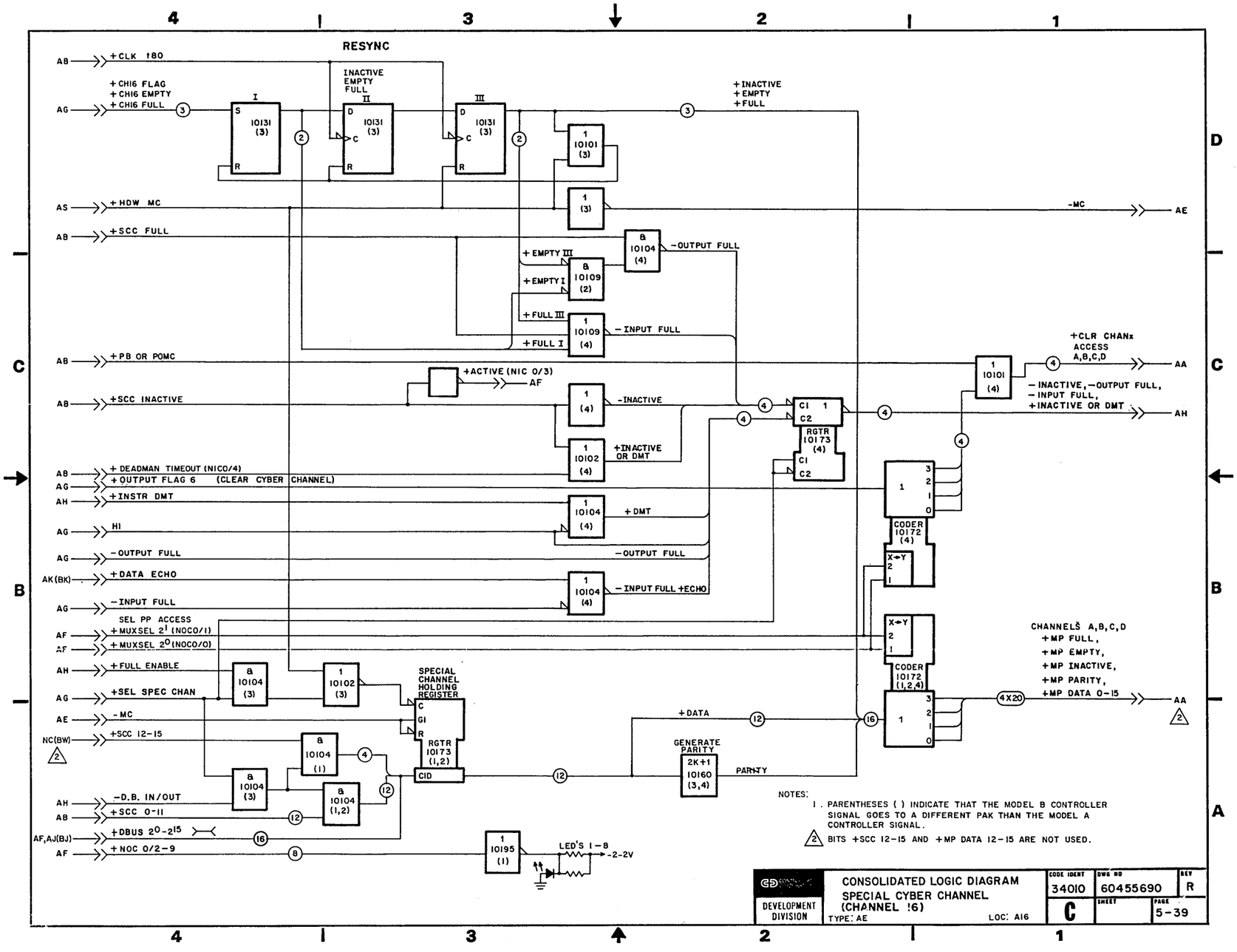
Bit 1	Bit 0	PP Access
L	L	A
L	H	B
H	L	C
H	H	D

Information sent from the PP to the processor comes into this pak as +SCC 0-11 signals and goes to the processor on the D bus. Information going to the PP from the special channel goes on the D bus to the holding register and to the R/Ts as +MP Data 0-11 signals.

Inactive, Empty, and Full flip-flops I, II, and III synchronize these signals with the channel clock before they are sent to the PP.

NOCO/2-9 control LEDs 1 through 8, NOCO/2 controls LED 1, NOCO/3 controls LED 2, and so forth. If all appear to be lighted, the controller is in the idle loop and is probably operating properly. If all are not lighted, then the A and P registers have probably stopped and the controller may have a failure.

The Inactive, -Output Full, -Input Full, and +Inactive or DMT signals are sent to the control memory pak at A22(AH) where they are used to alter the next address in the control memory. These can be generated either from the special channel or PP during a transfer on the special channel, or by the processor during a transfer on a normal processor channel.



NOTES:

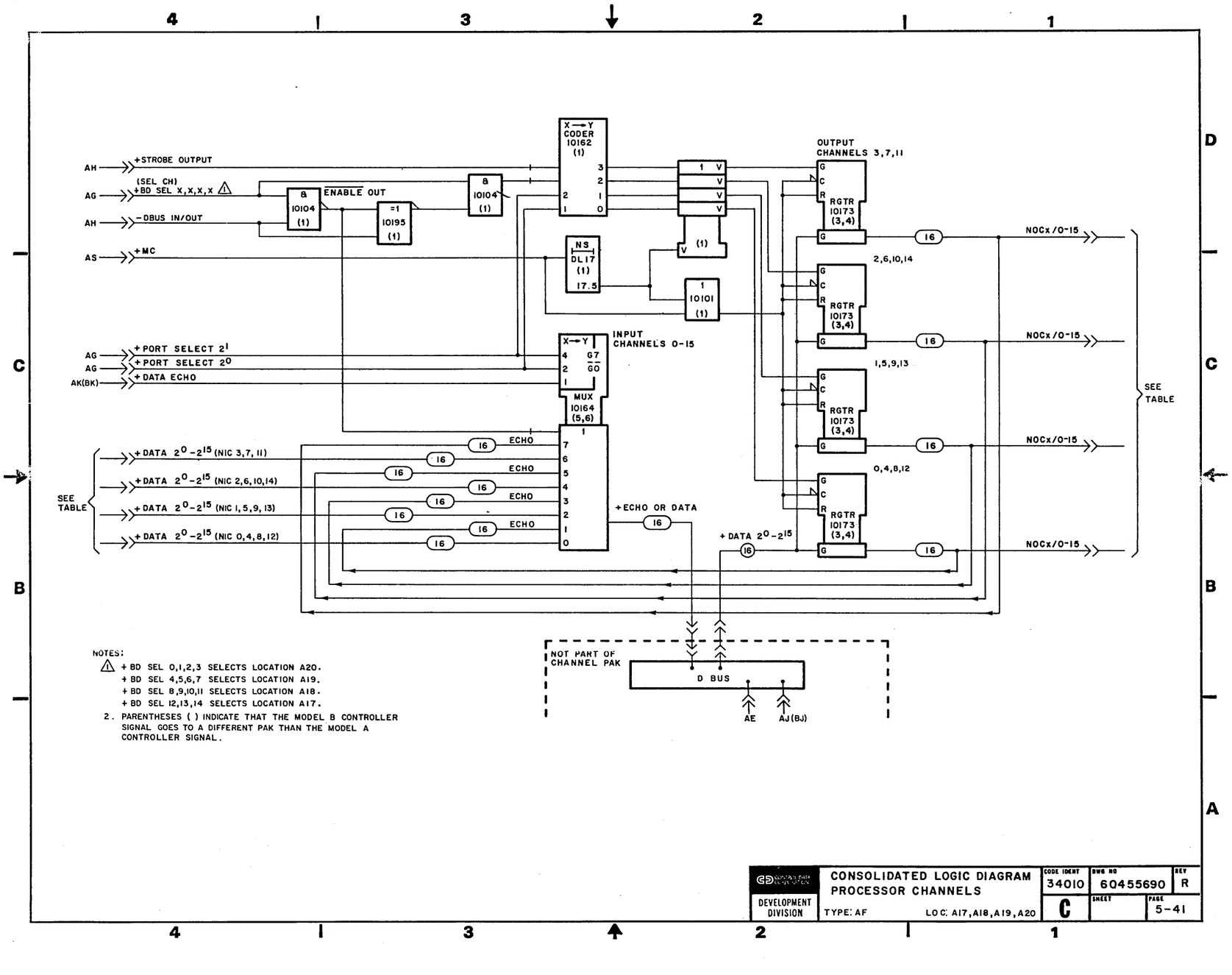
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
2. BITS +SCC 12-15 AND +MP DATA 12-15 ARE NOT USED.

DEVELOPMENT DIVISION	CONSOLIDATED LOGIC DIAGRAM SPECIAL CYBER CHANNEL (CHANNEL 16) TYPE: AE LOC: A16	CODE IDENT 34010	DWG NO 60455690	REV R
		SIZE C	SHEET	PAGE 5-39

PROCESSOR CHANNELS (A17, A18, A19, A20, AF)

The processor communicates with and controls the rest of the controller through fifteen 16-bit bidirectional channels. Channels 0, 1, 2, and 3 are located at A20; channels 4, 5, 6, and 7 are located at A19; channels 8, 9, 10, and 11 are located at A18; and channels 12, 13, 14, and 15 are located at A17. Channel 15 is not used.

The processor uses its D bus to read the input channels and to set bits in the output channel registers. Processor channel bits are defined in section 4.



NOTES:

⚠ + BD SEL 0,1,2,3 SELECTS LOCATION A20.
+ BD SEL 4,5,6,7 SELECTS LOCATION A19.
+ BD SEL 8,9,10,11 SELECTS LOCATION A18.
+ BD SEL 12,13,14 SELECTS LOCATION A17.

2. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

DEVELOPMENT DIVISION	CONSOLIDATED LOGIC DIAGRAM PROCESSOR CHANNELS	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AF LOC: A17,A18,A19,A20	C	SHEET	PAGE 5-41

CHANNEL CONTROL (A21, AG)

CHANNEL SELECTION

The channel number register contains the code for the input/output channel selected by the processor. Bit 2^4 selects the special CDC CYBER channel (channel 16).

OUTPUT FULL

The -Send Full signal from control memory generates a +Full Pulse signal for the selected channel. The functions of the used +Full Pulse signals are defined below.

Signal	Function
+Full Pulse 1	Load unit number
+Full Pulse 4	Load bit count
+Full Pulse 5	Load control word
+Full Pulse 6	Load buffer address
+Full Pulse 7	Load up/down counter
+Full Pulse 8	Initiate FMD function

Output Full stat flip-flops are not used except for channels 4 and 5. When +Empty 4 and +Empty 5 signals clear these flip-flops, it indicates that the control word and bit count have been loaded into the control word register and bit counter, respectively.

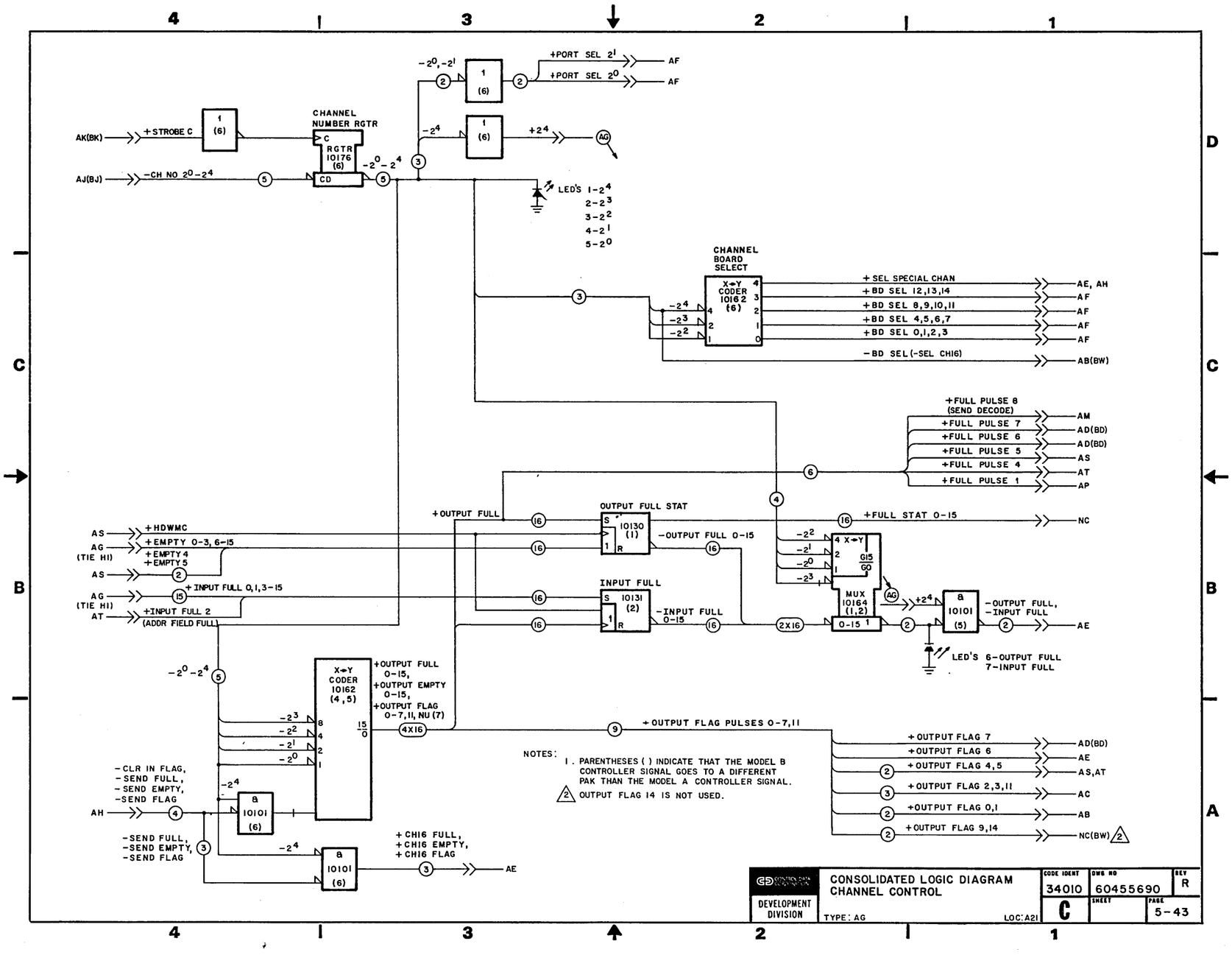
INPUT FULL

All Input Full signals, except +Input Full 2, are tied high. +Input Full 2 sets when the deskew register at B22 (AT) contains the address field. +Input Full 2 allows the processor to input, NIC2. The processor can read all other input channels at any time. -Send Empty signal, enabled by selection of channel 2, clears the input full flip-flop.

OUTPUT FLAGS

The -Send Flag signal from the control memory generates a +Output Flag signal for the selected channel. Following are the functions of the used +Output Flag signals.

Signal	Function
+Output Flag 0	Clear connect
+Output Flag 1	Master clear control logic
+Output Flag 2	Start error correction
+Output Flag 3	Clear ECC register
+Output Flag 4	Clear external status
+Output Flag 5	Terminate control word sequence
+Output Flag 6	Clear CDC CYBER interface
+Output Flag 7	Set reserve flip-flop
+Output Flag 9	Clear MC status (model B controller only)
+Output Flag 11	Load ECC register


AK(BK)
+STROBE C
AJ(BJ)
-CH NO 2⁰-2⁴
CHANNEL NUMBER RGTR
RGTR 10176 (6)
CD
-2⁰-2⁴
-2⁰,-2¹
-2⁴
+PORT SEL 2¹
+PORT SEL 2⁰
+2⁴
LED'S 1-2⁴ 2-2³ 3-2² 4-2¹ 5-2⁰
CHANNEL BOARD SELECT
X↔Y CODER 10162 (6)
+SEL SPECIAL CHAN
+BD SEL 12,13,14
+BD SEL 8,9,10,11
+BD SEL 4,5,6,7
+BD SEL 0,1,2,3
-BD SEL(-SEL CH16)
AE, AH
AB(BW)
+FULL PULSE 8 (SEND DECODE)
+FULL PULSE 7
+FULL PULSE 6
+FULL PULSE 5
+FULL PULSE 4
+FULL PULSE 1
AM
AD(BD)
AS
AT
AP
+OUTPUT FULL
OUTPUT FULL STAT
10130 (1)
-OUTPUT FULL 0-15
+FULL STAT 0-15
NC
INPUT FULL
10131 (2)
-INPUT FULL 0-15
MUX 10164 (1,2)
0-15
2X16
GI5 60
-OUTPUT FULL, -INPUT FULL
AE
LED'S 6-OUTPUT FULL 7-INPUT FULL
AS
AG (TIE HI)
AT
+HDWMC
+EMPTY 0-3, 6-15
+EMPTY 4
+EMPTY 5
+INPUT FULL 0,1,3-15
+INPUT FULL 2
(ADDR FIELD FULL)
X↔Y CODER 10162 (4,5)
+OUTPUT FULL 0-15,
+OUTPUT EMPTY 0-15,
+OUTPUT FLAG 0-7,11,NU (7)
4X16
+OUTPUT FLAG PULSES 0-7,11
+OUTPUT FLAG 7
+OUTPUT FLAG 6
+OUTPUT FLAG 4,5
+OUTPUT FLAG 2,3,11
+OUTPUT FLAG 0,1
+OUTPUT FLAG 9,14
AD(BD)
AE
AS,AT
AC
AB
NC(BW)
-CLR IN FLAG, -SEND FULL, -SEND EMPTY, -SEND FLAG
AH
-SEND FULL, -SEND EMPTY, -SEND FLAG
+CH16 FULL, +CH16 EMPTY, +CH16 FLAG
AE
NOTES:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
2 OUTPUT FLAG 14 IS NOT USED.
CONSOLIDATED LOGIC DIAGRAM
CHANNEL CONTROL
DEVELOPMENT DIVISION
TYPE: AG
LOC: A21
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
PAGE 5-43

CONTROL MEMORY (A22, AH)

This pak contains the 256-word, 60-bit-per-word control ROM. The ROM contains the modified PP instruction repertoire. The pak checks parity on every 60-bit word read from memory and lights LED 1 if an error is detected.

ADDRESSING

The address multiplexer outputs the next execution address for control memory. This address may be:

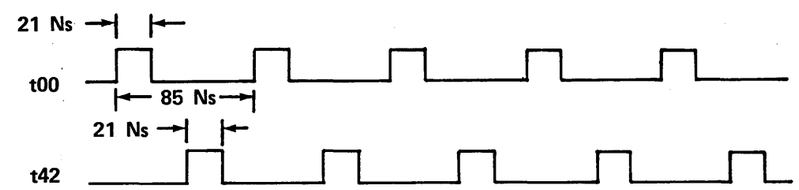
- Location 370_8 if a force idle loop or master clear condition exists.
- RNI condition causes the -F0 to -F5 (f segment) of the instruction to select the next address.
- -NA00 to -NA07 (next address 00 to 07). The two lowest order bits can be toggled to select a branch condition. The branch condition is determined by -CS00, -CS01, and -CS02, and the outputs AD0 and AD1 from the branch multiplexer toggle these two address bits.

DEFINITION OF CONTROL MEMORY OUTPUT BITS

NEXT ADDRESS NA00-NA07	10803 CONTROL MS00-MS13	10800 CONTROL AS00-AS14	MISCELLANEOUS CONTROL	PARITY PAR00-PAR04

CLOCKS

The 42.5-ns pulse generator provides the clock pulses used by the processor, t00 and t42. These have the following waveform.



INSTRUCTION DEADMAN TIMEOUT

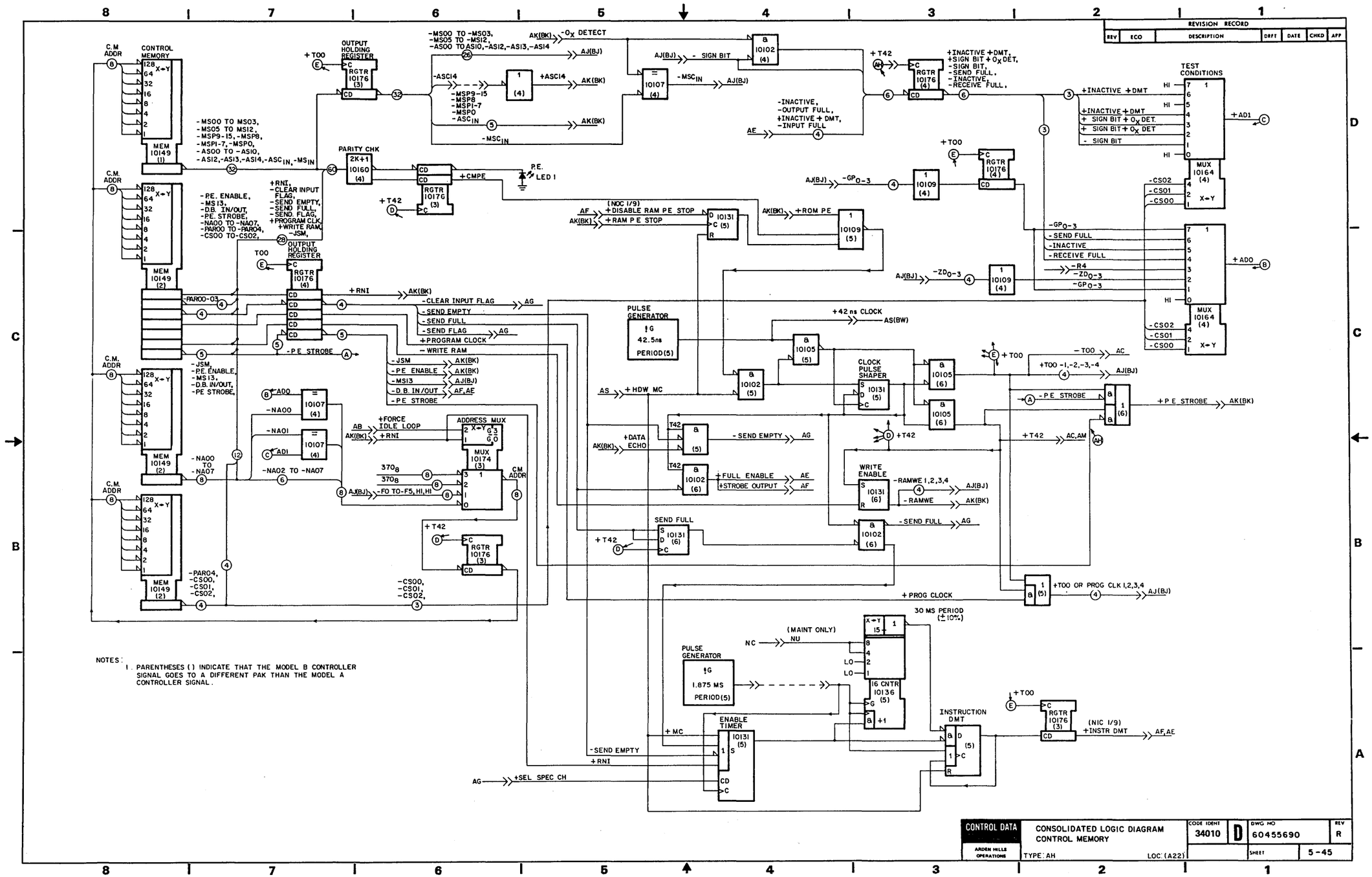
When the processor is executing a 70, 71, 72, or 73 instruction, instruction deadman timeout occurs if a full or empty is not generated for 30 ms (+10%) (on channels 0 through 14 only). When this happens, the normal channels are limited to one-word inputs. This condition sets NIC1/9. Master clear clears the condition.

WRITE ENABLE FF

The control ROM sends a +Write RAM signal to set the Write Enable flip-flop. +t42 clears this flip-flop. The -Ramwe signal enables the write cycle in the RAM and parity RAM.

SEND EMPTY, SEND FULL, SEND FLAG

The control ROM generates these signals to control the processor channels. +Send Full signal causes a full to be sent to the PP from the special channel or an output full to be sent from the selected processor channel. +Send Empty signal causes an empty to be sent to the PP from the special channel or to clear the input full on the selected processor channel. The +Send Flag signal causes an inactive to be sent to the PP on the special channel or an output flag on the selected processor channel.


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
C.M ADDR
CONTROL MEMORY
MEM 10149 (1)
MEM 10149 (2)
OUTPUT HOLDING REGISTER
RGTR 10176 (3)
RGTR 10176 (4)
RGTR 10176 (5)
RGTR 10176 (6)
RGTR 10176 (4)
RGTR 10176 (3)
RGTR 10176 (4)
RGTR 10176 (3)
PARITY CHK
2K+1 10160 (4)
RGTR 10176 (3)
P.E. LED 1
+CMPE
+T42
+T00
-MSOO TO -MS03, -MS05 TO -MSI2, -MSP9-15, -MSP8, -MSPI-7, -MSPO, -ASOO TO -ASI0, -ASI2, -ASI3, -ASI4, -ASC IN, -MS IN
-PE. ENABLE, -MSI3, -D.B. IN/OUT, -PE. STROBE, -NAOO TO -NAO7, -PAROO TO -PARO4, -CSOO TO -CS02
+RNI, -CLEAR INPUT FLAG, -SEND EMPTY, -SEND FULL, -SEND FLAG, +PROGRAM CLK, +WRITE RAM, -JSM,
-JSM, -PE. ENABLE, -MSI3, -D.B. IN/OUT, -PE STROBE,
-PARO4, -CSOO, -CSO1, -CSO2,
-NAOO TO -NAO7
-NAO2 TO -NAO7
-ASCI4
-MSP9-15 -MSP8 -MSPI-7 -MSPO -ASC IN
-MSC IN
-OX DETECT
-SIGN BIT
-INACTIVE, -OUTPUT FULL, +INACTIVE + DMT, -INPUT FULL
+INACTIVE +DMT, +SIGN BIT + OX DET, -SIGN BIT, -SEND FULL, -INACTIVE, -RECEIVE FULL,
TEST CONDITIONS
+INACTIVE +DMT
+INACTIVE +DMT + SIGN BIT + OX DET.
+ SIGN BIT + OX DET
- SIGN BIT
MUX 10164 (4)
+AD1
+AD0
-CSO2 -CSO1 -CSOO
X=Y
-GP0-3
-SEND FULL
-INACTIVE
-RECEIVE FULL
-R4
-ZD0-3
-GP0-3
AJ(BJ) -GP0-3
AJ(BJ) -ZD0-3
10109 (4)
10109 (5)
(NOC 1/9) +DISABLE RAM PE STOP
+RAM P E STOP
+ROM PE
AF
AK(BK)
10131 (5)
PULSE GENERATOR
42.5ns PERIOD(5)
+42 ns CLOCK
AS(BW)
AS
+HDW MC
10105 (5)
10102 (5)
CLOCK PULSE SHAPER
10131 (5)
10105 (6)
10102 (6)
+T00
-T00
AC
+T00 -1,-2,-3,-4
AJ(BJ)
-P.E STROBE
+P E STROBE
AK(BK)
1 (6)
+T42
AC,AM
+DATA ECHO
-SEND EMPTY
AG
+FULL ENABLE
+STROBE OUTPUT
AE
AF
WRITE ENABLE
-RAMWE 1,2,3,4
-RAMWE
10131 (6)
SEND FULL
-SEND FULL
+PROG CLOCK
+T00 OR PROG CLK 1,2,3,4
1 (5)
-CLEAR INPUT FLAG
-SEND EMPTY
-SEND FULL
-SEND FLAG
+PROGRAM CLOCK
-WRITE RAM
-JSM
-PE ENABLE
-MSI3
-D.B. IN/OUT
-PE STROBE
AK(BK)
AJ(BJ)
AF, AE
ADDRESS MUX
MUX 10174 (3)
CM ADDR
+FORCE IDLE LOOP
+RNI
AB
-FO TO-F5, HI, HI
370 8
-ADO
-NAOO
-NAO1
-ADI
10107 (4)
PULSE GENERATOR
1.875 MS PERIOD(5)
(MAINT ONLY)
NC
NU
LO
30 MS PERIOD (±10%)
16 CNTR 10136 (5)
+1
ENABLE TIMER
+MC
-SEND EMPTY
+RNI
AG
+SEL SPEC CH
INSTRUCTION DMT
(NIC 1/9) +INSTR DMT
AF,AE
NOTES:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL DATA
ARDEN HILLS OPERATIONS
CONSOLIDATED LOGIC DIAGRAM
CONTROL MEMORY
TYPE: AH
LOC: (A22)
CODE IDENT 34010
D
DWG NO 60455690
REV R
SHEET 5-45

4-BIT SLICE PROCESSOR (A23, A24, A25, A26, AJ) - Model A Controller

8-BIT SLICE PROCESSOR (A24, A26, BJ) - Model B Controller

These 60-paks comprise the central part of the processor. In the model A controller, each of the four paks is dedicated to four bits of the 16-bit processor word. The bits are distributed as follows:

Bits 0 through 3	A26	Slice 1
Bits 4 through 7	A25	Slice 2
Bits 8 through 11	A24	Slice 3
Bits 12 through 15	A23	Slice 4

In the model B controller, both paks are dedicated to eight bits of the 16-bit processor word. The bits are distributed as follows:

Bits 0 through 7	A26	Slice 1
Bits 8 through 15	A24	Slice 2

The paks contain the following circuits.

PROGRAM RAM

This 4096-word, 16-bit-per-word RAM stores controlware. Addresses from 0000_8 to 7777_8 select this memory. The P register LEDs indicate the address selected. The LEDs are located at A23 through A26 in the model A controller and at A27 on the model B controller.

BUFFER MEMORY

The buffer memory provides 2048 words of RAM for the model A controller and 4096 words RAM for the model B controller. Addresses 10000_8 through 13777_8 in the model A controller and 10000_8 through 17777_8 in the model B controller select this memory.

Buffer memory provides a temporary storage area during disk data transfers.

PARITY

The processor generates a parity bit for each byte written into the buffer and program RAM. Odd parity is used. The program memory parity bit is produced at location A25 (+Parity Data 1 signal). This parity bit is stored in the RAM at location A27. Setting NOC1/12 forces a program memory parity error.

The buffer memory parity bit is produced at location A24 (+Parity Data 2 signal). It is written into the buffer parity memory chip at location A27. Setting NIC1/13 forces a buffer memory parity error.

Parity checking is done at locations A26 and A27.

10800 - This microprocessor chip provides general hardware control in the processor.

10803 - This microprocessor chip performs the ALU function in the processor. It uses the D bus to set bits on the processor output channels and to read status from the processor input channels.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

+RAM OR BUFF ADDR 2^{13}
+RAM OR BUFF ADDR 2^{12}
+RAM OR BUFF ADDR 2^{11}
+RAM OR BUFF ADDR 2^{10}
+RNI 1
-ROM $2^{12},2^{13},2^{14},2^{15}$
+RAM OR BUFF ADDR 2^{0}-2^{9}
-RAM W.E.-1
AJ
AK
AK
AJ
AH

GROUP ENABLE
X↔Y 10161 CODER (6)
GRP 6
GRP 5
GRP 4
GRP 3
GRP 2
GRP 1

ALU 10803 (7)
REG FILE ADDR SEL
ALU FCTN
AR & RF DATA TRANSFER POINTER
D BUS DB3 DB2 DB1 DB0
RG/ZD
GG/OF
C_0
A3 A2 A1 A0
ADDRESS OUTPUT
C_{IN}
CLK
O BUS OB3 OB2 OB1 OB0
I BUS IB3 IB2 IB1 IB0

+D BUS 2^{15}
+D BUS 2^{14}
+D BUS 2^{13}
+D BUS 2^{12}
AE, AF
$-GP_3$
NU
AH
NC
+RAM OR BUFF ADDR $2^{12},2^{13}$, NU, NU
NC
AJ, AK

AN -MS00 to-MS03, -MS05 to-MS13
AK -PINPUT 12,13,14,15
(A24)AJ $-CO_3$
AH +T00 OR PROG CLK

1 10101 (7)
C RGTR 10176 (7) CO
ADDRESS OUT
LED 5-NU 6-NU 7-2^{13} 8-2^{12}

PROGRAM RAM
X↔Y
$+2^9$ 512
$+2^8$ 256
$+2^7$ 128
$+2^6$ 64
$+2^5$ 32
$+2^4$ 16
$+2^3$ 8
$+2^2$ 4
$+2^1$ 2
$+2^0$ 1
A1023 A0000
RAM GROUPS 1,2
B C G
MEM 10415 (3,4)
ACD AG ACD AG

DATA MUX
X↔Y 2 1 CO
MUX 10174 (1)
3 2 1 0
8 10101 (1) +DATA 2^{12}-2^{15} AK
-F3,-F4,-F5,NU AH
8 10105 (1) A

LED 1-
LED 2-
LED 3-
LED 4-
LED

AK +ENABLE EXTERNAL BUFFER 1
AD -WRITE ENABLE 3
AK +BUFF ADDR 2^{10}
AD -EXTERNAL WRITE DATA $2^{12},2^{13},2^{14},2^{15}$

GROUP 5 AND 6 ENABLE MUX
G2 G1 RGTR 10173 (6)
GROUP 6
GROUP 5
1 10105 (6)
G2 G1 RGTR 10173 (8)
×1 10113 (8)

X↔Y AI023 A0000 512 1
RAM GROUPS 3,4
MEM 10415 (2,4)
-2^0-2^9
+BUFF ADDR 2^0-2^9
AK
RAM GROUPS 5,6
BUFFER MEMORY
MEM 10415 (4,5)

CONTROL 10800 (8)
I BUS IB3 IB2 IB1 IB0
AS15
AS16
AS12-AS14
AS11
ADDRESS OUT A3 A2 A1 A0
SHIFT
CARRY
CLK
O BUS OB3 OB2 OB1 OB0
PC PR ZD OF
(CARRY) C_0
(GENERATE) GG
(PROPAGATE) PG
(SHIFT) R1

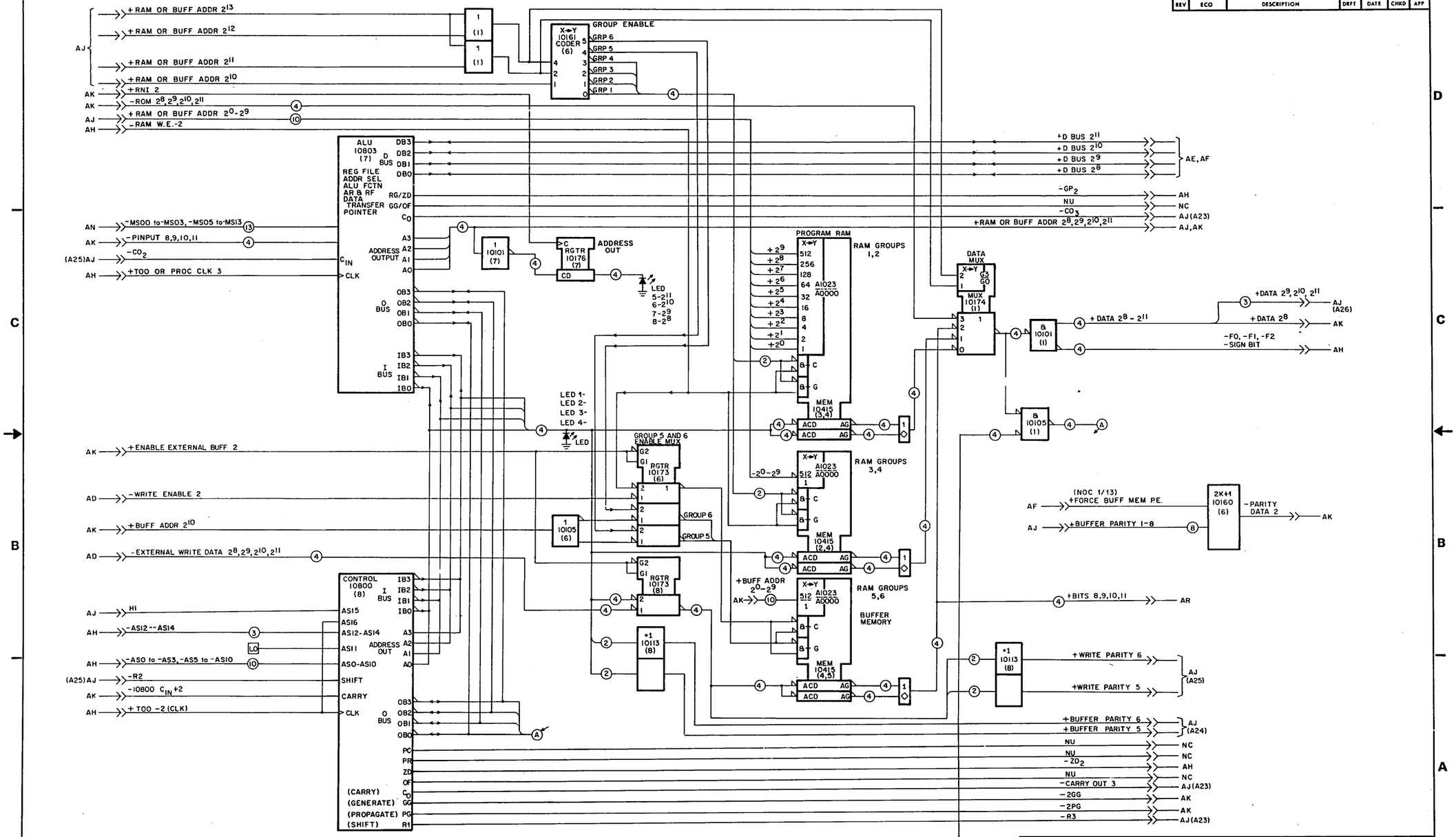
AJ HI
AH -AS12--AS14
LO
AH -AS0 to -AS3, -AS5 to -AS10
(A24)AJ -R3
(A24)AJ -CARRY OUT 3
AH +T00 (CLK)

+BITS 12,13,14,15 AR
×1 10113 (8)
+WRITE PARITY 8
+WRITE PARITY 7
AJ (A25)
+BUFFER PARITY 8
+BUFFER PARITY 7
AJ (A24)
NU NC
NU NC
$-ZD_3$ AH
NU NC
$-C_0$ NC
-3GG
-3PG
-R4
AK

AK -O BUS ENABLE -1,-2,-3,-4

CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM 4-BIT SLICE PROCESSOR (12-15) TYPE: AJ LOC: A23	CODE IDENT 34010	D	DWG NO 60455690	REV R
				SHEET 5-47	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM 4-BIT SLICE PROCESSOR (8-11) TYPE: AJ LOC: A24	CODE IDENT 34010	D	DWG NO 60455690	REV R
				SHEET 5-48	

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

+RAM OR BUFF ADDR 2^{13}
+RAM OR BUFF ADDR 2^{12}
+RAM OR BUFF ADDR 2^{11}
+RAM OR BUFF ADDR 2^{10}
+RNI 3
-ROM $2^4,2^5,2^6,2^7$
+RAM OR BUFF ADDR 2^{0}-29
-RAM W.E.-3

1 (1)
1 (1)
X↔Y 10161 CODER (6)
GROUP ENABLE
GRP 6
GRP 5
GRP 4
GRP 3
GRP 2
GRP 1

ALU 10803 (7)
REG FILE ADDR SEL ALU FCTN AR & RF DATA TRANSFER POINTER
D BUS
DB3
DB2
DB1
DB0
RG/ZD
GG/OF
C_O
A3
A2
A1
A0
ADDRESS OUTPUT
C_{IN}
CLK
OB3
OB2
OB1
OB0
O BUS
IB3
IB2
IB1
IB0
I BUS

-MS00 to-MS03, -MS05 to-MS13
-PINPUT 4,5,6,7
$-CO_1$
+TOO OR PROC CLK 2

1 10101 (7)
C RGTR 10176 (7) CD
ADDRESS OUT
LED 5-27 6-26 7-25 8-24

+D BUS 2^7
+D BUS 2^6
+D BUS 2^5
+D BUS 2^4
AE, AF
$-GP_1$
NU
$-CO_2$
+RAM OR BUFF ADDR $2^4,2^5,2^6,2^7$
AH
NC
AJ(A24)
AJ, AK

PROGRAM RAM
X↔Y
$+2^9$ 512
$+2^8$ 256
$+2^7$ 128
$+2^6$ 64
$+2^5$ 32
$+2^4$ 16
$+2^3$ 8
$+2^2$ 4
$+2^1$ 2
$+2^0$ 1
A1023 A0000
RAM GROUPS 1,2
8 C
8 G
MEM 10415 (3,4)
ACD AG
ACD AG
1

DATA MUX
X↔Y
MUX 10174 (1)
8 10101 (1)
+DATA 2^4
+DATA $2^5,2^6,2^7$
AJ(A26)
AK
-CH. NO. 2^4
AG
NC
8 10105 (1)

LED 1-
LED 2-
LED 3-
LED 4-
LED

GROUP 5 AND 6 ENABLE MUX
G2
G1
RGTR 10173 (6)
GROUP 6
GROUP 5
1 10105 (6)

-2^0-2^9
X↔Y
512 A1023 A0000
RAM GROUPS 3,4
MEM 10415 (2,4)

+BUFF ADDR 2^0-2^9
AK
RAM GROUPS 5,6
BUFFER MEMORY
MEM 10415 (4,5)

(NOC 1/12)
+FORCE PROG MEM P.E.
+WRITE PARITY 1-8
2K+1 10160 (6)
-PARITY DATA 1
AK

+BITS 4,5,6,7
AR

×1 10113 (8)
+WRITE PARITY 4
+WRITE PARITY 3
AJ (A25)

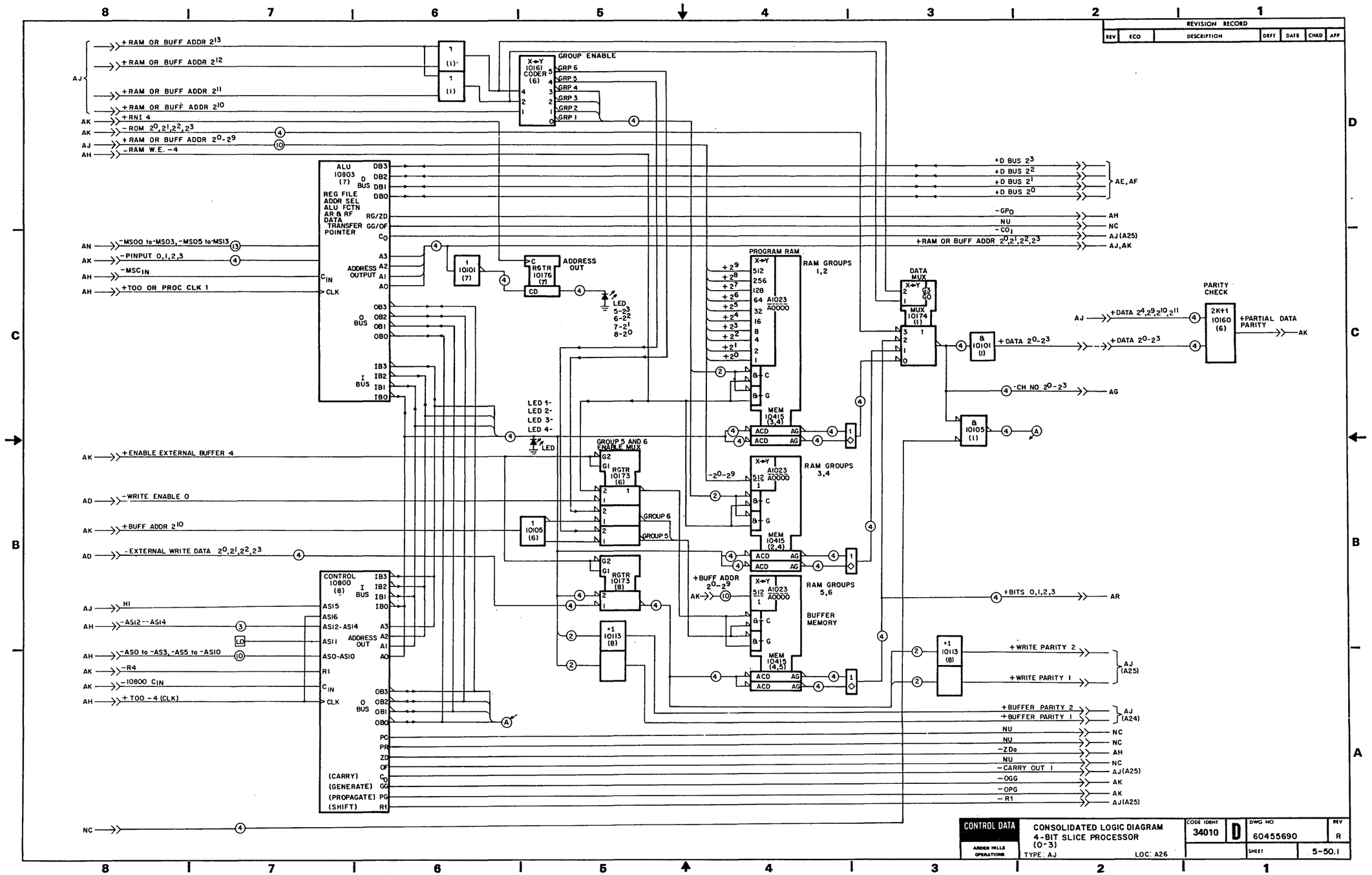
+BUFFER PARITY 4
+BUFFER PARITY 3
AJ (A24)
NU
NC
NU
NC
$-ZD_1$
AH
NU
NC
NC
-IGG
AK
-IPG
AK
-R2
AJ(A24)

+ENABLE EXTERNAL BUFFER 3
-WRITE ENABLE 1
+BUFF ADDR 2^{10}
-EXTERNAL WRITE DATA $2^4,2^5,2^6,2^7$

CONTROL 10800 (8)
HI
-AS12--AS14
-ASO to -AS3, -AS5 to -ASIO
-R4
-CARRY OUT 1
+TOO -3 (CLK)
ASI5
ASI6
ASI2-ASI4
ASI1
ASO-ASI0
RI
CLK
(CARRY) C_O
(GENERATE) GG
(PROPAGATE) PG
(SHIFT) RI
PC
PR
ZD
OF

NU

CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM 4-BIT SLICE PROCESSOR (4-7) TYPE: AJ LOC: A25	CODE IDENT 34010	D	DWG NO 60455690	REV R
				SHEET 5-49	


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
+RAM OR BUFF ADDR 2^13
+RAM OR BUFF ADDR 2^12
+RAM OR BUFF ADDR 2^11
+RAM OR BUFF ADDR 2^10
+RNI 4
-ROM 2^0,2^1,2^2,2^3
+RAM OR BUFF ADDR 2^0-2^9
-RAM W.E. -4
GROUP ENABLE
X=Y 10161 CODER (6)
GRP 6
GRP 5
GRP 4
GRP 3
GRP 2
GRP 1
ALU 10803 (7)
REG FILE ADDR SEL
ALU FCTN
AR & RF
DATA TRANSFER
POINTER
D BUS
DB3
DB2
DB1
DB0
RG/ZD
GG/OF
C0
A3
A2
A1
A0
ADDRESS OUTPUT
CIN
CLK
OB3
OB2
OB1
OB0
O BUS
IB3
IB2
IB1
IB0
I BUS
+D BUS 2^3
+D BUS 2^2
+D BUS 2^1
+D BUS 2^0
AE, AF
-GP0
NU
-CO1
+RAM OR BUFF ADDR 2^0,2^1,2^2,2^3
AH
NC
AJ (A25)
AJ, AK
-MS00 to -MS03, -MS05 to -MS13
-PINPUT 0,1,2,3
-MSCIN
+T00 OR PROC CLK 1
1 10101 (7)
C RGTR 10176 (7) CD
ADDRESS OUT
LED 5-2^3 6-2^2 7-2^1 8-2^0
PROGRAM RAM
RAM GROUPS 1,2
A1023 A0000
MEM 10415 (3,4)
ACD AG
DATA MUX
MUX 10174 (1)
PARITY CHECK
2K+1 10160 (6)
AJ
+DATA 2^4,2^9,2^10,2^11
+DATA 2^0-2^3
+PARTIAL DATA PARITY
AK
8 10101 (1)
-CH NO 2^0-2^3
AG
8 10105 (1)
A
LED 1-
LED 2-
LED 3-
LED 4-
LED
GROUP 5 AND 6 ENABLE MUX
RGTR 10173 (6)
GROUP 6
GROUP 5
1 10105 (6)
RAM GROUPS 3,4
-2^0-2^9
RAM GROUPS 5,6
+BUFF ADDR 2^0-2^9
AK
BUFFER MEMORY
RGTR 10173 (8)
=1 10113 (8)
+BITS 0,1,2,3
AR
+WRITE PARITY 2
+WRITE PARITY 1
AJ (A25)
+BUFFER PARITY 2
+BUFFER PARITY 1
AJ (A24)
NU
NC
-ZD0
AH
-CARRY OUT 1
AJ (A25)
-OGG
AK
-OPG
AK
-R1
AJ (A25)
+ENABLE EXTERNAL BUFFER 4
-WRITE ENABLE 0
+BUFF ADDR 2^10
-EXTERNAL WRITE DATA 2^0,2^1,2^2,2^3
CONTROL 10800 (8)
HI
-AS12 -- AS14
-AS0 to -AS3, -AS5 to -AS10
-R4
-10800 CIN
+T00 -4 (CLK)
AS15
AS16
AS12-AS14
AS11
AS0-AS10
R1
CIN
CLK
PC
PR
ZD
OF
(CARRY) C0
(GENERATE) GG
(PROPAGATE) PG
(SHIFT) R1
LO
NC
CONTROL DATA
ARDEN HILLS OPERATIONS
CONSOLIDATED LOGIC DIAGRAM
4-BIT SLICE PROCESSOR
(0-3)
TYPE: AJ
LOC: A26
CODE IDENT 34010
D
DWG NO 60455690
REV R
SHEET 5-50.1

PROGRAM ROM, PARITY RAM (A27, AK) - Model A Controller

PROGRAM ROM FOR 8-BIT SLICE (A27, BK) - Model B Controller

PROGRAM ROM

The program ROM has a capacity of 1024 16-bit words. The ROM contains an autoload subroutine, some function routines, and some rudimentary diagnostics. Addresses 20000_8 to 21777_8 select the program ROM.

PROGRAM MEMORY PARITY RAM

This RAM contains the parity bit for the 4096 16-bit words in the program memory RAM. The same address is used for both the program memory and the parity RAM.

LOOK AHEAD CARRY

The propagate and generate outputs from the 10800 chips are sent to the look-ahead carry ALU chip. This is a time-saving device to determine whether a carry will be generated in the 10800.

PARITY ERROR

A high from the read parity check circuit indicates that an error has been detected during a read from the program ROM, program RAM, or buffer memory. Because the program ROM uses addresses 20000_8 to 21777_8, +RAM or Buff Addr 2^{13} signal enables the ROM P.E. signal.

STROBE C

When low, this signal strobes the processor channel number into the channel number register at A21. This goes low when the -P.E. Strobe signal goes low and when a +RNI signal is high during a 6X or 7X instruction.

DATA ECHO

The +Data Echo signal goes high when bit 2^8 is high during a 70 instruction. +Data Echo causes the processor output channels to loop back into the respective input channel.

PROGRAM SYNC

Testpoint 50 reflects the state of bit 15 of all processor instructions. Bit 15 is not used for the instructions but can be set or cleared from the console for maintenance purposes.

-P INPUTS 0-15

These signals set up a mask that is used by the 10803 chip. During a 76 or 77 instruction, the -JSM signal enables the coder to determine the contents of the -P Input signals. Any other time the -MSP0, -MSP1-7, -MSP8, and -MSP9-15 signals from control memory determine the -P Input signal.

-Ox DETECT

The $-O_X$ Detect signal goes low when memory sends an O_X (jump type) instruction. This signal modifies the control memory address causing a branch operation in certain conditions.

This signal also enables the -R4 signals that are used for an end-around shift in the 10800 chips. The -R4 signals also modify the control memory address.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

PROGRAM MEM

+ENABLE EXTERNAL BUFF 1,2,3,4 → AJ

(NOC 7113) +BUFF MODE SEL

AF

+RAM OR BUFF ADDR 2^0-2^9

AJ / AD

+BMA 2^0-2^9

ADDRESS RGTR — RGTR 10173 (3)

+BUFF ADDR 2^0-2^9 → AJ

$+2^8+2^9$

AH — −RAM W.E.

PARITY RAM — A1023 A000 — MEM 10415 (4) — ACD AG

0,1,2,3

AJ — −PARITY DATA 1

CHIP SELECTOR — X=Y CODER 10161 (6)

$+2^9$, $+2^8$, $+2^{13}$

PROGRAM ROM — A255 A000

LO

0-4

MEM 10149 (6,7) — AG

−ROM 2^0+2^{15} → AJ

ROM PARITY — −ROM 2^3, −ROM 2^2, −ROM 2^1, −ROM 2^0 → −ROM PARITY

MUX 10164 (6)

CHIP SELECTOR — X=Y CODER 10161 (4)

+RAM OR BUFF +ADDR 2^{12}, +ADDR 2^{11}, +ADDR 2^{10}, $+2^{13}$

BUFF PAR ADDR RGTR — RGTR 10173 (5)

AD — −WRITE ENABLE

AD — +BMA 2^{10}

BUFFER PARITY — A1023 A000 — MEM 10415 (5)

$+2^0$-$+2^9$

+BUFF ADDR 2^{10} → AJ

AJ (A24) — −PARITY DATA 2

−BUFF PAR → AR (B20)

RAM OR BUFF 2^{12}, 2^{11}, 2^{10}

RAM PARITY — MUX 10164 (4) → −RAM PARITY

10800 PROPAGATE/GENERATE: −3GG, −3PG, −2GG, −2PG, −1GG, −1PG, −0GG, −0PG

LOOK-AHEAD CARRY: 65536, 61440, 4096, 3840, 256, 240, 16, 15, 1

ALU 10179 (2)

AH — −ASC_{IN} → 1 (2) → −10800 C_{IN} → AJ (A26)

ΣA,B ≥ 65536

ΣA,B = 65535

ΣB,C ≥ 256

−10800 C_{IN}+2 → AJ (A24)

READ PARITY CHECK — 2K+1 10160 (1)

(A26) AJ — −ROM PARITY

AJ — +PARTIAL DATA PARITY

AJ — $+2^{12}$-$+2^{15}$

AH — −PARITY ENBL

AH — P.E. STROBE

'DL17' (1) 11.5 10NS

AS — +HDW MC — CATCH P.E.

+RAM OR BUFF ADDR 2^{13}

AJ (A23)

D 10131 (1) C R

8 10105 (1)

ROM P.E. — LED1

LED2 PARITY ERROR

+ROM P.E. → AH

+RAM P.E. STOP → AH

+RAM P.E. STATUS → AF

8 (1) — +RNI $+2^{13}$, $+2^{14}$ — −STROBE C → AG

B REGISTER — CD, CD, CD — RGTR 10176 (1) — TP50 PROGRAM SYNC

$+2^{15}$, -2^8, $+2^5$-$+2^8$

1 (1) — $+2^8$

8 (1) — −O BUS ENABLE → AJ; $-O_x$ DETECT → AH

AH — +RNI

AH — −JSM

−O BUS ENABLE → AJ

+RNI → AH, AJ

8 10104 (2) — +DATA ECHO → AE, AF, AH

1 10104 (1)

AH — −ASI4

AJ (A23) — −R4

8 ◇

AH — −MSP9-15 — 1 10101 10102 (2) — −P INPUT 9-15 → AJ (A25, A26)

X=Y CODER 10162 (2) — $+2^7$, $+2^6$, $+2^5$, -2^8

AH — −MSP8 — 1 10102 (2) — −P INPUT 8 → AJ (A25)

AH — −MSPI-7 — 1 10102 (2) — −P INPUT I-7 → AJ (A23, A24)

X=Y CODER 10162 (2) — $+2^7$, $+2^6$, $+2^5$, $+2^8$

AH — −MSP0 — 1 10102 (2) — −P INPUT 0 → AJ (A23)

−R4 ① → AJ (A26)

−R4 ① → AH

NOTES: ① BIDIRECTIONAL LINES.

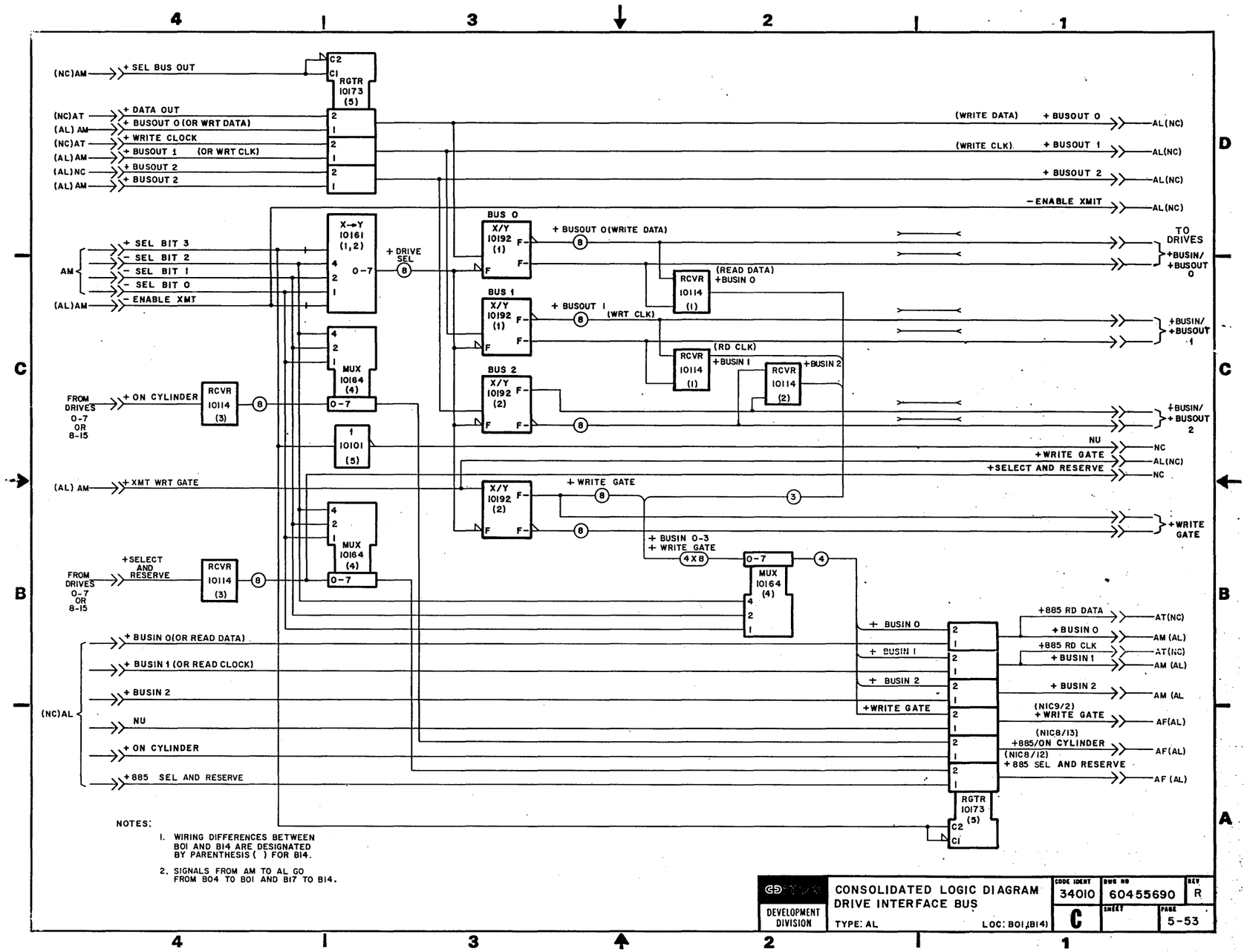
CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM PROGRAM ROM, PARITY RAM	CODE IDENT 34010	D	DWG NO 60455690	REV R
	TYPE: AK LOC: (A27)			SHEET 5-51	

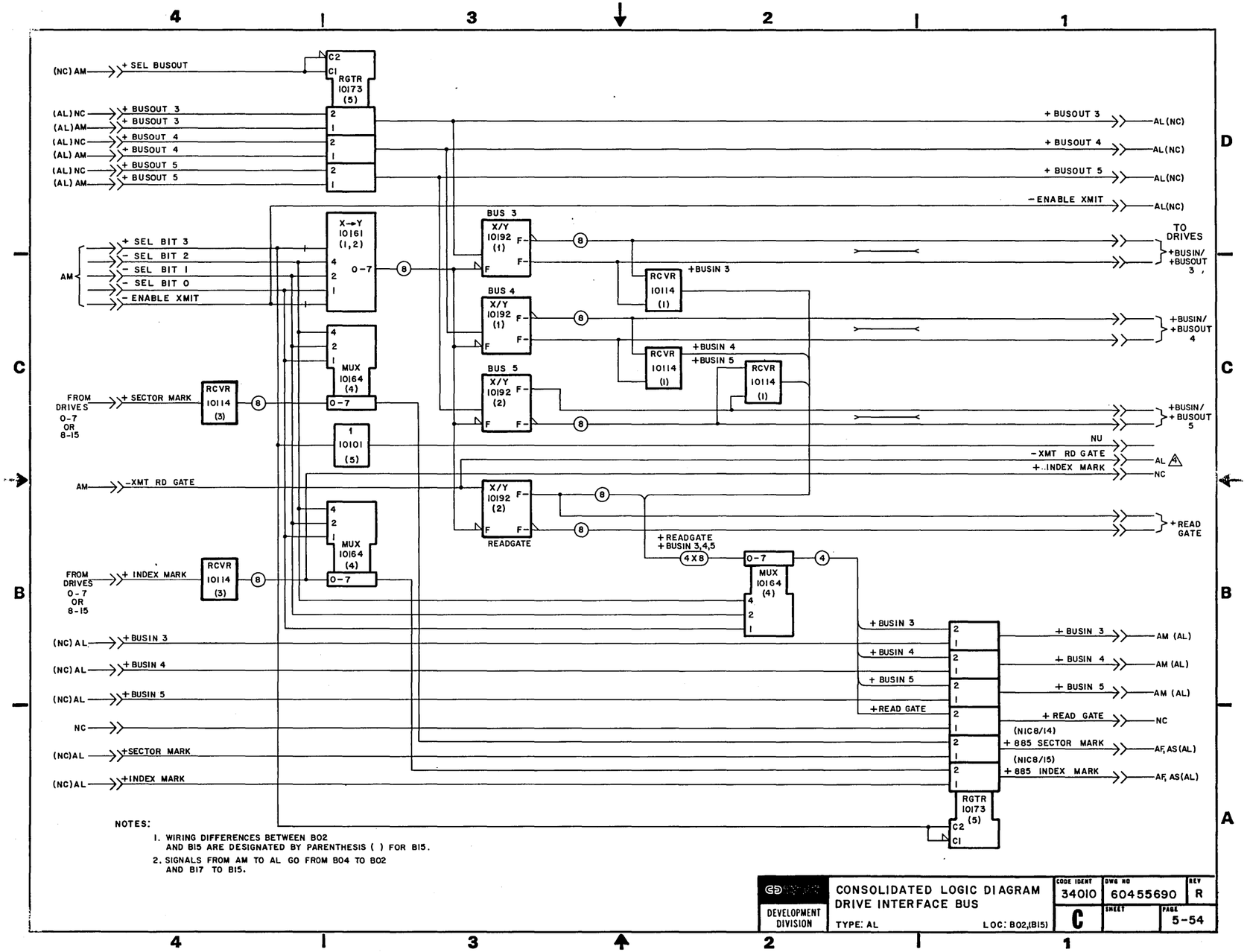
DRIVE INTERFACE BUS (B01, (B14), B02, (B15), B03, (B16), AL)

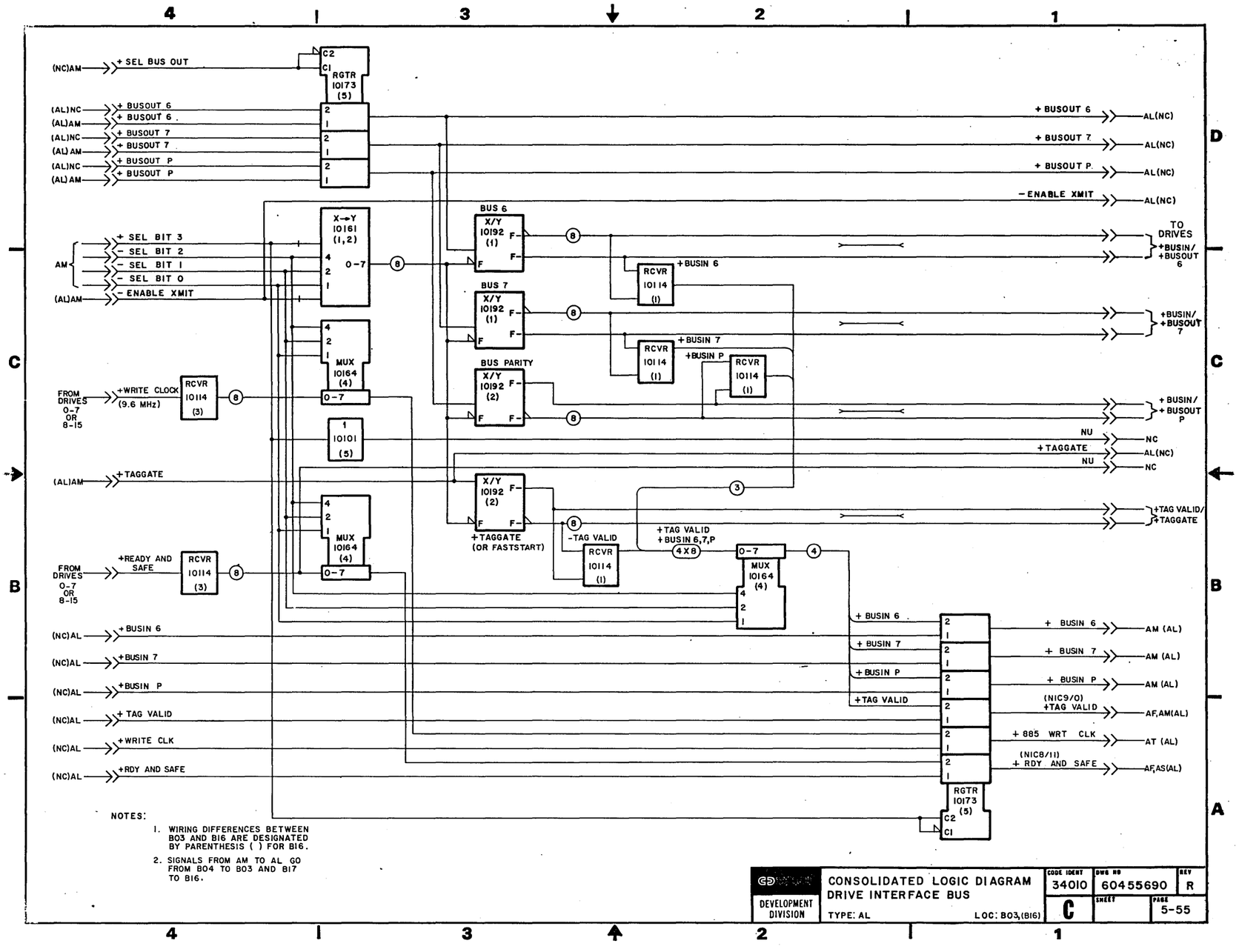
These 60-paks constitute the interface with the FMD. Paks at locations B01, B02, and B03 connect to drives 0 through 7. Paks at locations B14, B15, and B16 connect to drives 8 through 15 and are part of the Four FMD Option.

The paks at B01 and B14, B02 and B15, and B03 and B16 have a parallel function. They transfer the same signals. Drive interface control at location B04 selects one of drives 0 through 7. Drive interface control at location B17 selects one of drives 8 through 15. +Sel Bit 3 signal selects B01, B02, or B03 if low or B14, B15, or B16 if high.

Paks at B01, B02, and B03 multiplex signals to/from B14, B15, and B16 as well as signals intended for drives 0 through 7.


(NC)AM
+ SEL BUS OUT
C2
CI
RGTR 10173 (5)
(NC)AT
(AL) AM
(NC)AT
(AL)AM
(AL)NC
(AL)AM
+ DATA OUT
+ BUSOUT 0 (OR WRT DATA)
+ WRITE CLOCK
+ BUSOUT 1 (OR WRT CLK)
+ BUSOUT 2
+ BUSOUT 2
(WRITE DATA) + BUSOUT 0 AL(NC)
(WRITE CLK) + BUSOUT 1 AL(NC)
+ BUSOUT 2 AL(NC)
- ENABLE XMIT AL(NC)
AM
(AL)AM
+ SEL BIT 3
- SEL BIT 2
- SEL BIT 1
- SEL BIT 0
- ENABLE XMT
X→Y 10161 (1,2)
+ DRIVE SEL
BUS 0
BUS 1
BUS 2
X/Y 10192 (1)
X/Y 10192 (2)
+ BUSOUT 0(WRITE DATA)
+ BUSOUT 1 (WRT CLK)
RCVR 10114 (1)
(READ DATA) +BUSIN 0
(RD CLK) +BUSIN 1
RCVR 10114 (2)
+BUSIN 2
TO DRIVES +BUSIN/ +BUSOUT 0
+BUSIN/ +BUSOUT 1
+BUSIN/ +BUSOUT 2
FROM DRIVES 0-7 OR 8-15
+ ON CYLINDER
RCVR 10114 (3)
MUX 10164 (4)
1 10101 (5)
NU
NC
+ WRITE GATE
AL(NC)
+SELECT AND RESERVE
NC
(AL) AM
+ XMT WRT GATE
+ WRITE GATE
+ WRITE GATE
+ BUSIN 0-3
+ WRITE GATE
4X8
FROM DRIVES 0-7 OR 8-15
+SELECT AND RESERVE
(NC)AL
+ BUSIN 0(OR READ DATA)
+ BUSIN 1 (OR READ CLOCK)
+ BUSIN 2
NU
+ ON CYLINDER
+885 SEL AND RESERVE
+ BUSIN 0
+ BUSIN 1
+ BUSIN 2
+WRITE GATE
+885 RD DATA AT(NC)
+ BUSIN 0 AM (AL)
+885 RD CLK AT(NC)
+ BUSIN 1 AM (AL)
+ BUSIN 2 AM (AL
(NIC9/2) +WRITE GATE AF(AL)
(NIC8/13) +885/ON CYLINDER AF(AL)
(NIC8/12) +885 SEL AND RESERVE AF (AL)
RGTR 10173 (5)
NOTES:
1. WIRING DIFFERENCES BETWEEN B01 AND B14 ARE DESIGNATED BY PARENTHESIS ( ) FOR B14.
2. SIGNALS FROM AM TO AL GO FROM B04 TO B01 AND B17 TO B14.
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
DRIVE INTERFACE BUS
TYPE: AL
LOC: B01,(B14)
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET
PAGE 5-53


(NC) AM
+ SEL BUSOUT
C2
C1
RGTR 10173 (5)
(AL) NC
(AL) AM
+ BUSOUT 3
+ BUSOUT 4
+ BUSOUT 5
2
1
+ BUSOUT 3 AL(NC)
+ BUSOUT 4 AL(NC)
+ BUSOUT 5 AL(NC)
- ENABLE XMIT AL(NC)
AM
+ SEL BIT 3
- SEL BIT 2
- SEL BIT 1
- SEL BIT 0
- ENABLE XMIT
X→Y 10161 (1,2)
4
2
1
0-7
8
BUS 3
BUS 4
BUS 5
X/Y 10192 (1)
X/Y 10192 (2)
F
RCVR 10114 (1)
+BUSIN 3
+BUSIN 4
+BUSIN 5
TO DRIVES
+BUSIN/ +BUSOUT 3
+BUSIN/ +BUSOUT 4
+BUSIN/ +BUSOUT 5
FROM DRIVES 0-7 OR 8-15
+ SECTOR MARK
RCVR 10114 (3)
MUX 10164 (4)
1 10101 (5)
NU
- XMT RD GATE
+ INDEX MARK
AL
NC
AM
- XMT RD GATE
READGATE
+ READGATE
+ BUSIN 3,4,5
4X8
+ READ GATE
+ INDEX MARK
(NC) AL
+ BUSIN 3
+ BUSIN 4
+ BUSIN 5
NC
+ SECTOR MARK
+ INDEX MARK
+ BUSIN 3 AM (AL)
+ BUSIN 4 AM (AL)
+ BUSIN 5 AM (AL)
+ READ GATE NC
(NIC8/14)
+ 885 SECTOR MARK AF, AS(AL)
(NIC8/15)
+ 885 INDEX MARK AF, AS(AL)
NOTES:
1. WIRING DIFFERENCES BETWEEN B02 AND B15 ARE DESIGNATED BY PARENTHESIS ( ) FOR B15.
2. SIGNALS FROM AM TO AL GO FROM B04 TO B02 AND B17 TO B15.
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
DRIVE INTERFACE BUS
TYPE: AL
LOC: B02,(B15)
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET
PAGE 5-54


4
3
2
1
D
C
B
A
(NC)AM
+ SEL BUS OUT
C2
C1
RGTR
10173
(5)
(AL)NC
(AL)AM
+ BUSOUT 6
+ BUSOUT 7
+ BUSOUT P
2
1
AM
(AL)AM
+ SEL BIT 3
- SEL BIT 2
- SEL BIT 1
- SEL BIT 0
- ENABLE XMIT
X→Y
10161
(1,2)
4
2
1
0-7
8
MUX
10164
(4)
FROM DRIVES 0-7 OR 8-15
+WRITE CLOCK
(9.6 MHz)
RCVR
10114
(3)
1
10101
(5)
+TAGGATE
+READY AND SAFE
BUS 6
X/Y
10192
(1)
F
BUS 7
BUS PARITY
X/Y
10192
(2)
+TAGGATE
(OR FASTSTART)
RCVR
10114
(1)
+BUSIN 6
+BUSIN 7
+BUSIN P
-TAG VALID
+TAG VALID
+BUSIN 6,7,P
4X8
3
+ BUSOUT 6
+ BUSOUT 7
+ BUSOUT P.
- ENABLE XMIT
AL(NC)
TO DRIVES
+BUSIN/
+BUSOUT
6
7
P
NU
NC
+TAGGATE
+TAG VALID/
(NC)AL
+BUSIN 6
+BUSIN 7
+BUSIN P
+TAG VALID
+WRITE CLK
+RDY AND SAFE
AM (AL)
(NIC9/0)
(NIC8/11)
+ 885 WRT CLK
AT (AL)
AF,AM(AL)
AF,AS(AL)
NOTES:
1. WIRING DIFFERENCES BETWEEN B03 AND B16 ARE DESIGNATED BY PARENTHESIS ( ) FOR B16.
2. SIGNALS FROM AM TO AL GO FROM B04 TO B03 AND B17 TO B16.
GD
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
DRIVE INTERFACE BUS
TYPE: AL
LOC: B03,(B16)
CODE IDENT
34010
DWG NO
60455690
REV
R
C
SHEET
PAGE
5-55

DRIVE INTERFACE CONTROL (B04, (B17), AM)

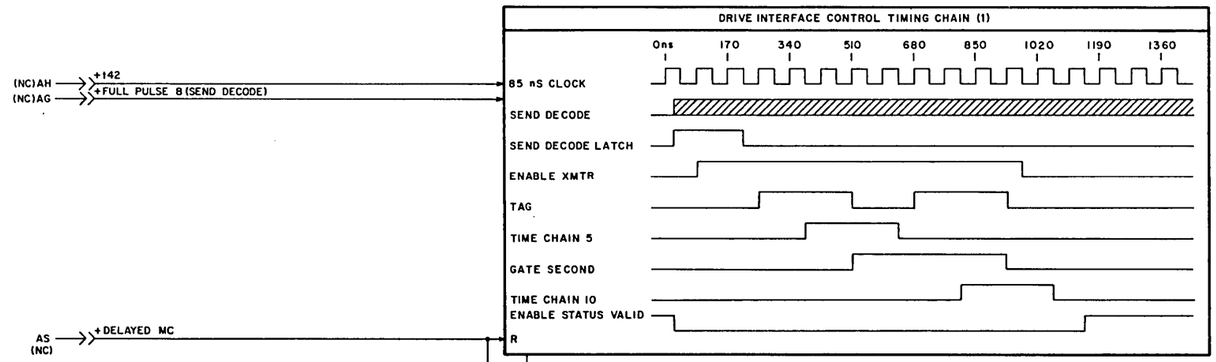
The 60-pak at location B04 controls the 885 interface at locations B01, B02, and B03, and communicates with drives 0 through 7. The pak at location B17 controls the 885 interface at locations B14, B15, and B16, and communicates with drives 8 through 15. B17 is a part of the Four FMD Option.

The +Disable Reserve signal is set by NOC1/7. This signal, when sent to the 885 with the FMD select bit (that is set by NOC1/6), releases the reserve on the other access of the selected drive. The drive ignores the +Disable Reserve signal if the +Select signal is not present.

Eight disable switches, located on the switch panel at the top front of the cabinet, enable or disable the controller access to the respective drive.

885 status is received on the busin 0 through 7 lines from the selected drive. The Drive Status Valid flip-flop must be set to read status. This sets NIC8/9, indicating that contents of the status holding register can be sampled. Another 885 function sequence clears Status Valid flip-flop. 885 functions are carried on the busout 0 through 7 lines. NOC8/0-7 contain the tag decode portion of 885 functions and NOC8/8-15 contain bus information. +Full Pulse 8 signal initiates the 885 function sequence.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



(NC)AH → +142
(NC)AG → +FULL PULSE 8 (SEND DECODE)

AS (NC) → +DELAYED MC

AR (NC) → +FAST START

AS (NC) → +READ GATE

AF (NC) → +NOC8/0-7 (TAG DECODE)

AF (NC) → +BUS 0-7 (NOC8/8-15)

(NC)AF → +FORCE BUS PE (NOC1/11)

AF (NC) → +LOOP DECODE (NOC1/14)

AF (NC) → +LOOP BUS (NOC1/15)

AL (NC) → +TAG VALID

AS (NC) → +WRITE GATE

(AM)AP → (-UNIT SEL BIT 3) +UNIT SEL BIT 3

(AM)AP → -UNIT SEL BIT 0-2

AL → +BUS IN 0-7,P

AF → +FORCE STATUS PE (NOC1/10)

(AM) → -SEL 0-2

(AM) → +SEL 3 (-SEL 3)

AF (AM) → +DISABLE RESERVE (NOC1/7)

HI → DISABLE SWITCHES → (AM) AF +SELECT (NOC1/6); +DISABLE 0-7 ⚠; AP -POWER STABLE

+TAG
+ENABLE XMTR
+GATE SECOND
+TIME CHAIN 5
+TIME CHAIN 10
+ENABLE STATUS VALID
+MC
+SEND DECODE LATCH
+ENABLE XMTR
+DISABLE RESERVE TO DRIVE
+SELECT TO DRIVES

10105 (1) → +TAG GATE → AL (B03)

10105 (1) → -XMT RD GATE → AL (B02)

+XMT RD GATE → AL (B01)

885 FUNCTIONS: 1 (3)

PARITY GENERATE: 2K+1 10160 +P

+BUS OUT 0-7,P → AL (NC)

DRIVE STATUS VALID: 1 (3) S (1) R

(NIC8/9) + TAG VALID LATCH → AF

70-140 NS (1) R

8 10104 (1)

1 (1)

+XMT WRT GATE → AL (B01)

+SEL BUS OUT → AL

-ENABLE XMT → AL

(-SEL 3) +SEL 3 → AL, AM, AM(NC)

+SEL 0-2 → AL, AM, AM(NC)

-UNIT SEL BIT → AM (NC) (B04 TO B17)

1 (2)

1 (2)

CD RGTR 10171 C (2) STATUS HOLDING REGISTER

(885 STATUS) + NIC8/0-7 BUSIN 0-7 → AF

PARITY CHECK: 2K+1 10160 (2)

8 10104 (2)

(NIC8/8) +STATUS PE → AF

+DISABLE RESERVE 0-7(8-15) → TO 885

X→Y CODER 10162 (4) 0-7

X/Y 10192 (4)

+DISABLE RESERVE → AM(NC) (B04 TO B17)

-UNIT SEL BIT 0-2 → AM (NC)

X→Y CODER 10161 (4) 0-7

8 X/Y (4) F

(+SELECT 8-15) +SELECT 0-7 → TO 885

+SELECT → AM (B04 TO B17) (NC)

NOTES:

⚠ DISABLE SWITCHES FOR UNITS 0-7 ARE LOCATED AT B01. THOSE FOR 8-15 ARE LOCATED AT B17.

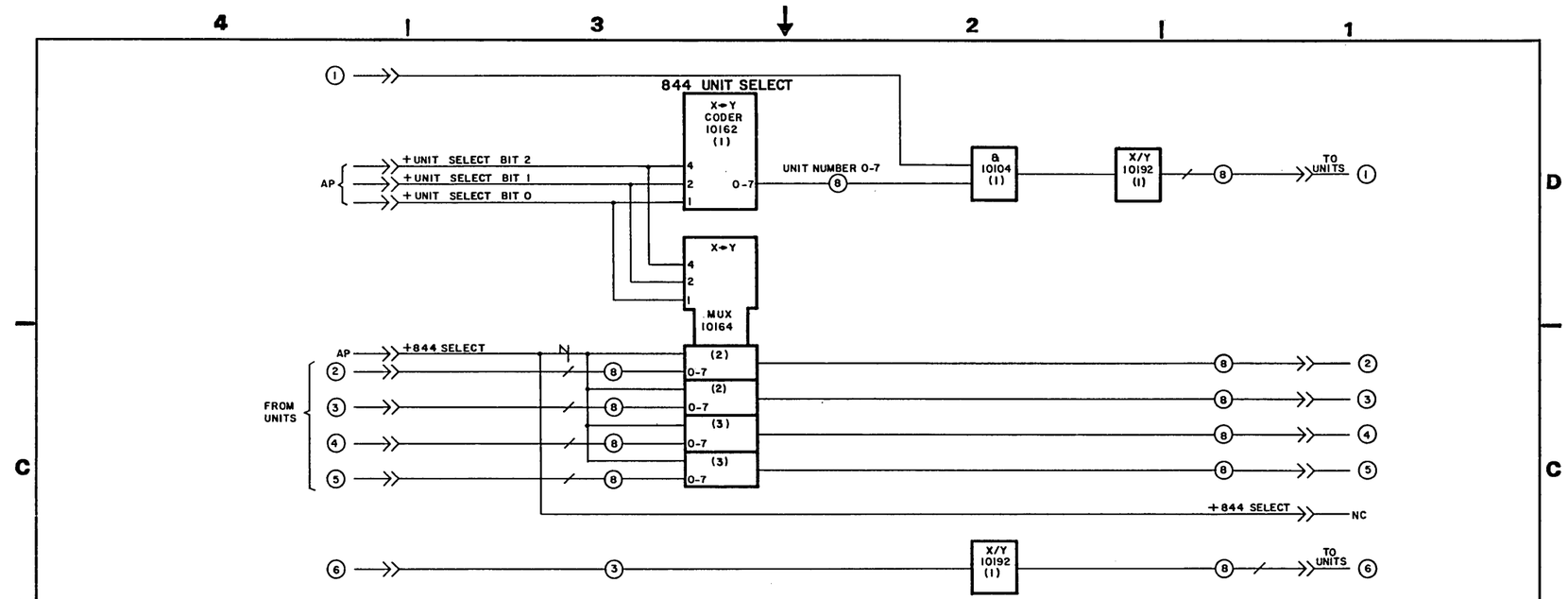
2. WHERE B17 ORIGIN/DESTINATION INFORMATION DIFFERS FROM B04, B17 INFORMATION WILL BE ENCLOSED IN PARENTHESIS.

CONTROL DATA	CONSOLIDATED LOGIC DIAGRAM	CODE IDENT		DWG NO	REV
ARDEN HILLS OPERATIONS	DRIVE INTERFACE CONTROL	34010	D	60455690	R
	TYPE: AM LOC: B04, B17			SHEET	5-57

844 8:1 INTERFACE (B05-B12, AN)

These eight 60-paks constitute all the logic for the 844 Drive Option. They contain the receivers and transmitters connected to the eight 844 disk units. The processor selects a disk unit by setting bits in +Unit Select 0, 1, and 2 signals.

The chart shows the signals associated with each pak.



LOC:	SIGNAL ASSIGNMENT (ALL POSITIVE POLARITY)							
	B05	B06	B07	B08	B09	B10	B11	B12
1	NU	WRITE CLOCK	DATA OUT	CLEAR OR RESERVE	RELEASE	CLEAR FAULT	EQUIP SELECT 0-7	BUSOUT 9
2	NU	UNIT 0-7 SELECTED AF	UNIT 0-7 BUSY AF	UNIT 0-7 READY AF	SEEK ERROR 0-7 AF	ON SECTOR 0-7 AN	BUSIN 0 0-7 AN	BUSIN 1 0-7 AN
3	NU	WRITE CLOCK AT	READ CLOCK AP	READ DATA AP	NU	NU	NU	NU
4	BUSIN 2 AF	BUSIN 3 AF	BUSIN 4 AP	BUSIN 5 AF	BUSIN 6 AF	BUSIN 7 AF	BUSIN 8 AP	BUSIN 9 AP
5	NU	NU	ON LINE AF	DOUBLE DENSITY AP	NU	NU	NU	NU
6	READ CYL SELECT	READ SECTOR COUNT	READ INTLK	CONTROL SELECT	HEAD SELECT	BUSOUT 0 AP	BUSOUT 3 AF	BUSOUT 6 AF
	READ DIFF CNTR	READ SECTOR RGTR	READ FAULT	SECTOR SELECT	CYL SELECT	BUSOUT 1 AP	BUSOUT 4 AF	BUSOUT 7 AF
	READ HEAD RGTR	READ POSN	READ CONTROL	NU	DIFFER SELECT	BUSOUT 2 AF	BUSOUT 5 AF	BUSOUT 8 AF

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CONSOLIDATED LOGIC DIAGRAM 844 8:1 INTERFACE TYPE: AN LOC: B05-B12	CODE IDENT 34010 C	DWG NO 60455690 SHEET	REV R PAGE 5-59

844 INTERFACE CONTROL (B13, AP)

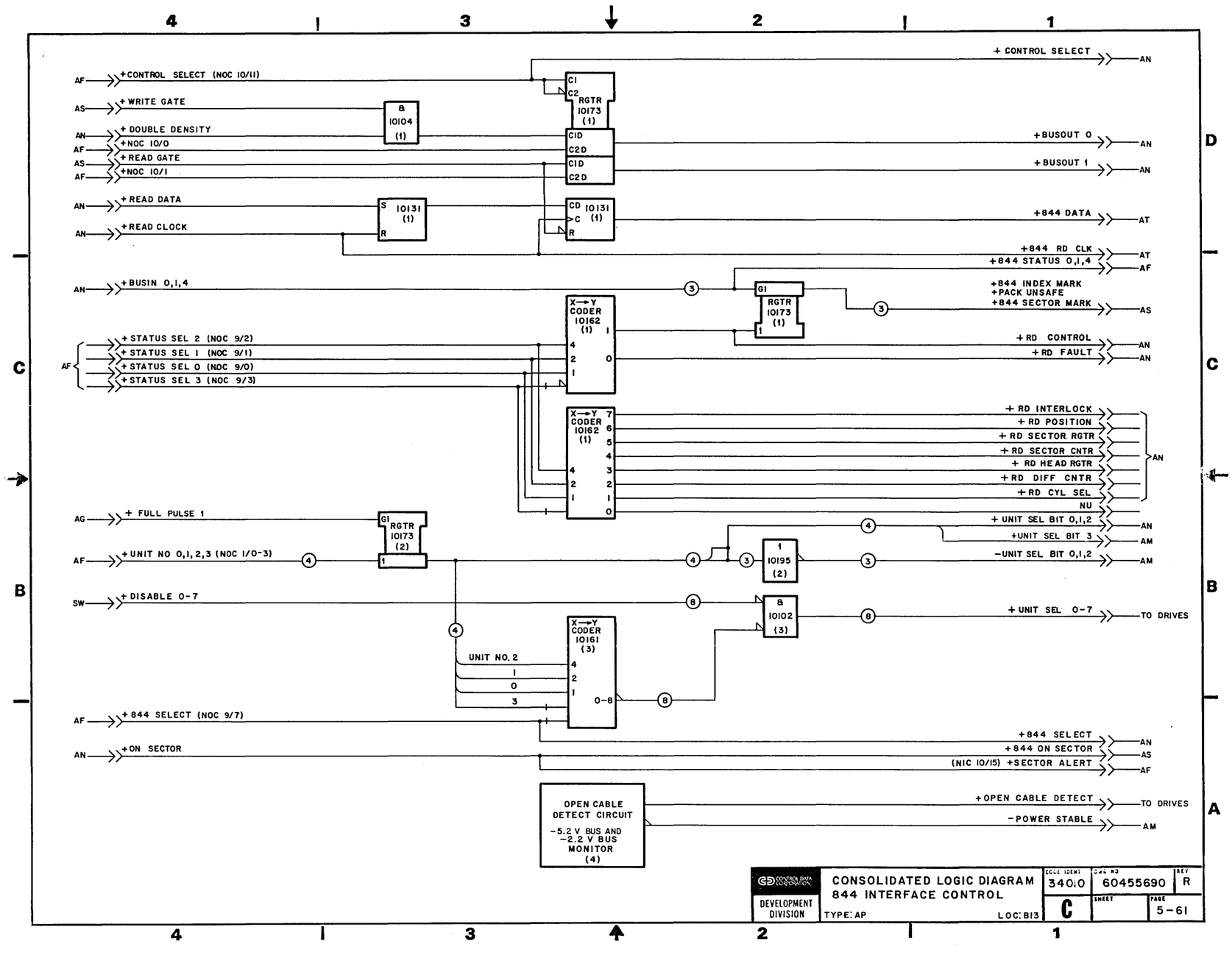
This pak sends the unit select (+Unit Sel 0-7 signals) to one of the 844 units. The processor determines the selection by sending the select code in NOC1/0-3. This code also is used to select a FMD. The +844 Select signal (NOC9/7) enables 844 selection.

NOC9/0-3 select one of nine 844 status codes. These are defined in section 4.

The power loss detect circuit protects the disk drive interface when applying or removing power to/from the controller. A switch on the pak can disable the circuit when running voltage margins. The power loss detect circuit disables the 885 select transmitters and the 844 open cable detect transmitters if power drops by more than 5%.

WARNING

Put the protected/disable switch in the disable (down) position when running voltage margins.


+CONTROL SELECT
AN
AF
+CONTROL SELECT (NOC 10/11)
C1
C2
RGTR
10173
(1)
AS
+WRITE GATE
8
10104
(1)
AN
+DOUBLE DENSITY
AF
+NOC 10/0
AS
+READ GATE
AF
+NOC 10/1
C1D
C2D
+BUSOUT 0
+BUSOUT 1
AN
+READ DATA
S
10131
(1)
R
CD
C
+844 DATA
AT
AN
+READ CLOCK
+844 RD CLK
+844 STATUS 0,1,4
AF
AN
+BUSIN 0,1,4
3
G1
RGTR
10173
(1)
+844 INDEX MARK
+PACK UNSAFE
+844 SECTOR MARK
AS
X→Y
CODER
10162
(1)
+STATUS SEL 2 (NOC 9/2)
+STATUS SEL 1 (NOC 9/1)
+STATUS SEL 0 (NOC 9/0)
+STATUS SEL 3 (NOC 9/3)
+RD CONTROL
+RD FAULT
+RD INTERLOCK
+RD POSITION
+RD SECTOR RGTR
+RD SECTOR CNTR
+RD HEAD RGTR
+RD DIFF CNTR
+RD CYL SEL
NU
AG
+FULL PULSE 1
+UNIT NO 0,1,2,3 (NOC 1/0-3)
+UNIT SEL BIT 0,1,2
+UNIT SEL BIT 3
AM
-UNIT SEL BIT 0,1,2
1
10195
(2)
SW
+DISABLE 0-7
+UNIT SEL 0-7
TO DRIVES
UNIT NO. 2
0-8
+844 SELECT (NOC 9/7)
+844 SELECT
+844 ON SECTOR
(NIC 10/15) +SECTOR ALERT
+ON SECTOR
OPEN CABLE
DETECT CIRCUIT
-5.2 V BUS AND
-2.2 V BUS
MONITOR
(4)
+OPEN CABLE DETECT
-POWER STABLE
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
844 INTERFACE CONTROL
TYPE: AP
LOC: B13
ECLE IDENT
340:0
DWG NO
60455690
REV
R
SHEET
C
PAGE
5-61

READ/WRITE DATA PATH (B19, B20, AR)

WRITE DATA PATH

The write operation transfers data from the buffer memory to the disk. +Bits 0-15 are sent from the buffer memory to the output register at B19/B20. From there data goes to the parity test circuit and to the holding register. A 16-bit byte is entered into the data shift register and then these 16 bits are shifted out serially from B20 as +Data Out. Then another 16-bit byte is entered into the data shift register. The byte counter at B22 (AT) provides the enable to load the data shift register.

DATA COMPARE

The processor can initiate a write verify operation by setting NOC2/7. This causes a bit-by-bit comparison of data from the disk with data from the buffer memory. Any miscompare sets NIC1/4.

READ DATA PATH

The read operation transfers data from the disk to the buffer memory. +Read Data is serial data sent to the data shift register from B22 (AT). The data shift register assembles serial data into 16-bit bytes which are sent to the deskew register. From there each byte goes to the catching register at A15, and from there to the buffer memory.

During a buffer-to-PP operation, read data comes back to B19/B20 as +Bits 0-15 signals enter the output register and go to A01, A02, A03, and A04 (AA) as a 12-bit byte (+Bfr Data 0-11 signals). +Bits 12-15 signals are not used.

SYNC BYTES

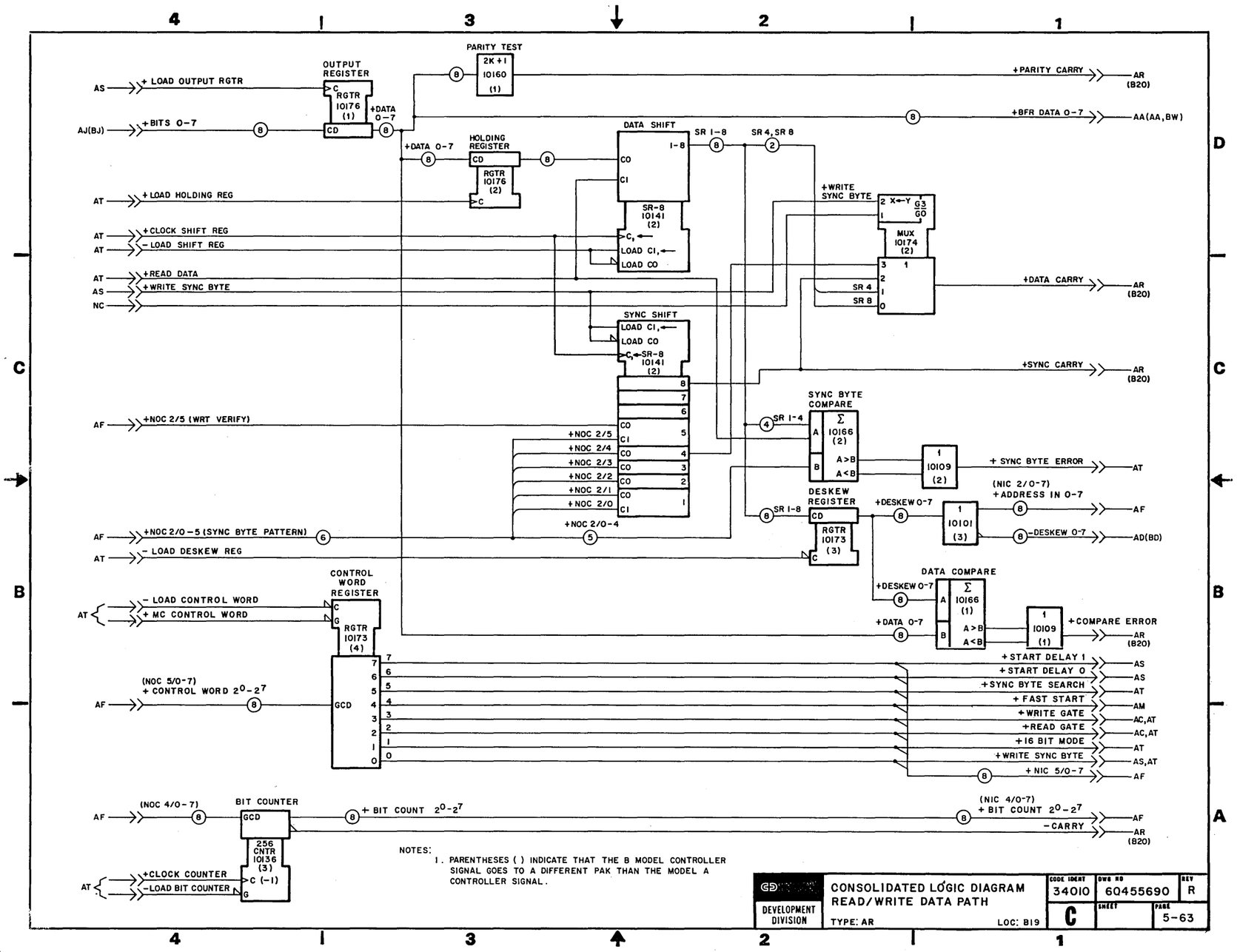
During a write operation, a sync byte is written on the disk. NOC5/0 causes the sync byte to be written. The lower 6 bits are taken from NOC2/0-5. The upper 6 bits are all zeros. The sync pattern for 844-4x is 110011 and for 885 is 11001. The sync pattern goes through the sync shift register and then the multiplexer to B22 (AT).

During a read operation, the controller reads the sync byte from the disk. The sync byte compare circuit determines whether the sync byte matched NOC2/0-5. If it did not, +Sync Byte Error signal goes high at B19.

CONTROL WORD REGISTER/BIT COUNTER

The control word register is loaded by the processor from NOC5. Each bit in the control word is used to start or control some operation in the controller or disk.

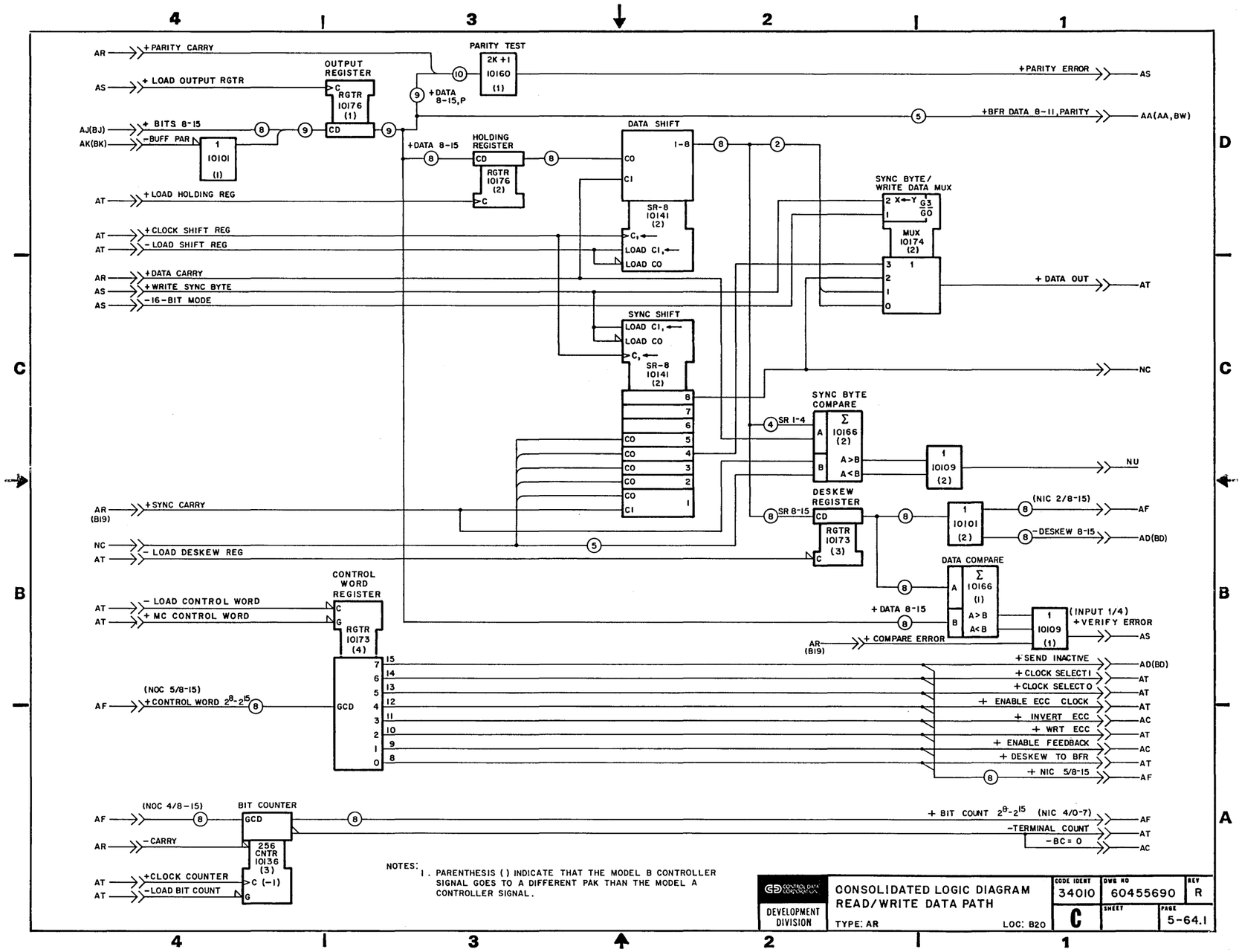
The bit counter must be loaded with a count from NOC4 every time a new control word sequence is to be executed. One sequence step consists of first issuing a bit count and then issuing a control word. The selected clock generates the +Clock Counter signal that decrements the counter. The sequence completes when the counter decrements to zero. This enables loading the counter and register again.



NOTES:

1. PARENTHESES ( ) INDICATE THAT THE B MODEL CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CONSOLIDATED LOGIC DIAGRAM READ/WRITE DATA PATH	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AR LOC: B19	C	SHEET	PAGE 5-63


AR
+PARITY CARRY
AS
+ LOAD OUTPUT RGTR
AJ(BJ)
AK(BK)
+ BITS 8-15
-BUFF PAR
1
10101
(1)
OUTPUT REGISTER
RGTR 10176 (1)
CD
PARITY TEST
2K+1
10160
(1)
+DATA 8-15,P
+PARITY ERROR
AS
+BFR DATA 8-11,PARITY
AA(AA,BW)
+DATA 8-15
HOLDING REGISTER
CD
RGTR 10176 (2)
AT
+ LOAD HOLDING REG
DATA SHIFT
1-8
CO
CI
SR-8 10141 (2)
LOAD CI,
LOAD CO
AT
+CLOCK SHIFT REG
AT
-LOAD SHIFT REG
AR
+DATA CARRY
AS
+WRITE SYNC BYTE
AS
-16-BIT MODE
SYNC BYTE/ WRITE DATA MUX
2 X←Y G3
1 GO
MUX 10174 (2)
3 1
2
1
0
+ DATA OUT
AT
SYNC SHIFT
LOAD CI,
LOAD CO
C,
SR-8 10141 (2)
NC
SYNC BYTE COMPARE
SR 1-4
A
B
Σ 10166 (2)
A>B
A<B
1 10109 (2)
NU
AR (B19)
+SYNC CARRY
NC
AT
-LOAD DESKEW REG
DESKEW REGISTER
SR 8-15
CD
RGTR 10173 (3)
1 10101 (2)
(NIC 2/8-15)
AF
-DESKEW 8-15
AD(BD)
DATA COMPARE
Σ 10166 (1)
+DATA 8-15
AR (B19)
+ COMPARE ERROR
1 10109 (1)
(INPUT 1/4)
+VERIFY ERROR
AS
CONTROL WORD REGISTER
AT
- LOAD CONTROL WORD
AT
+ MC CONTROL WORD
RGTR 10173 (4)
GCD
(NOC 5/8-15)
AF
+CONTROL WORD 2^8-2^15
+SEND INACTIVE
+CLOCK SELECT1
+CLOCK SELECT0
+ ENABLE ECC CLOCK
+ INVERT ECC
+ WRT ECC
+ ENABLE FEEDBACK
+ DESKEW TO BFR
+ NIC 5/8-15
AD(BD)
AT
AT
AC
AT
AC
AT
AC
AT
AF
(NOC 4/8-15)
AF
BIT COUNTER
GCD
AR
-CARRY
256 CNTR 10136 (3)
AT
+CLOCK COUNTER
AT
-LOAD BIT COUNT
C (-1)
G
+ BIT COUNT 2^8-2^15 (NIC 4/0-7)
-TERMINAL COUNT
-BC=0
AF
AT
AC
NOTES:
1. PARENTHESIS ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
READ/WRITE DATA PATH
TYPE: AR
LOC: B20
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET
PAGE 5-64.1

BUFFER TO DATA PATH CONTROL (B21, AS)

MARK START FLIP-FLOP

+Start Delay 0 and +Start Delay 1 signals are derived from bits 6 and 7 of the control word (NOC5). These two bits are coded as follows:

1	0	
L	L	No delay
L	H	Sector mark delay
H	L	On sector delay
H	H	Index mark delay

The selection of sector mark delay, on sector delay, or index mark delay delays setting the Mark Start flip-flop until the disk sends the sector mark, on sector, or index mark signal to the controller. The Mark Start flip-flop causes +Start Condition Met signal to go high, allowing the bit counter (on the paks at B19/B20) to start decrementing.

A delay circuit allows the controller to determine if the 885 is on sector. The drive is on sector if the +885 Sector Mark signal stays high more than 470 ns.

SECTOR MARK VIOLATION FLIP-FLOP

This flip-flop sets if the controller detects a sector mark when the +Read Gate or +Write Gate signal is high. This error halts the operation in progress and sets NIC1/2. Skipping sector mark (NOC2/6) disables this circuit.

CONTROL WORD READY FLIP-FLOP

The +Full Pulse 5 signal sets the Control Word Ready flip-flop, causing the control word in normal output channel 5 to become available to the control word register at B19/B20 (AR). When the control word sequence begins execution, the +Control Wd Reply signal clears the Control Word Rdy flip-flop. This causes a +Empty signal to be sent to A21 (AG), which allows the controller to output another control word sequence.

READ BUFFER FLIP-FLOP

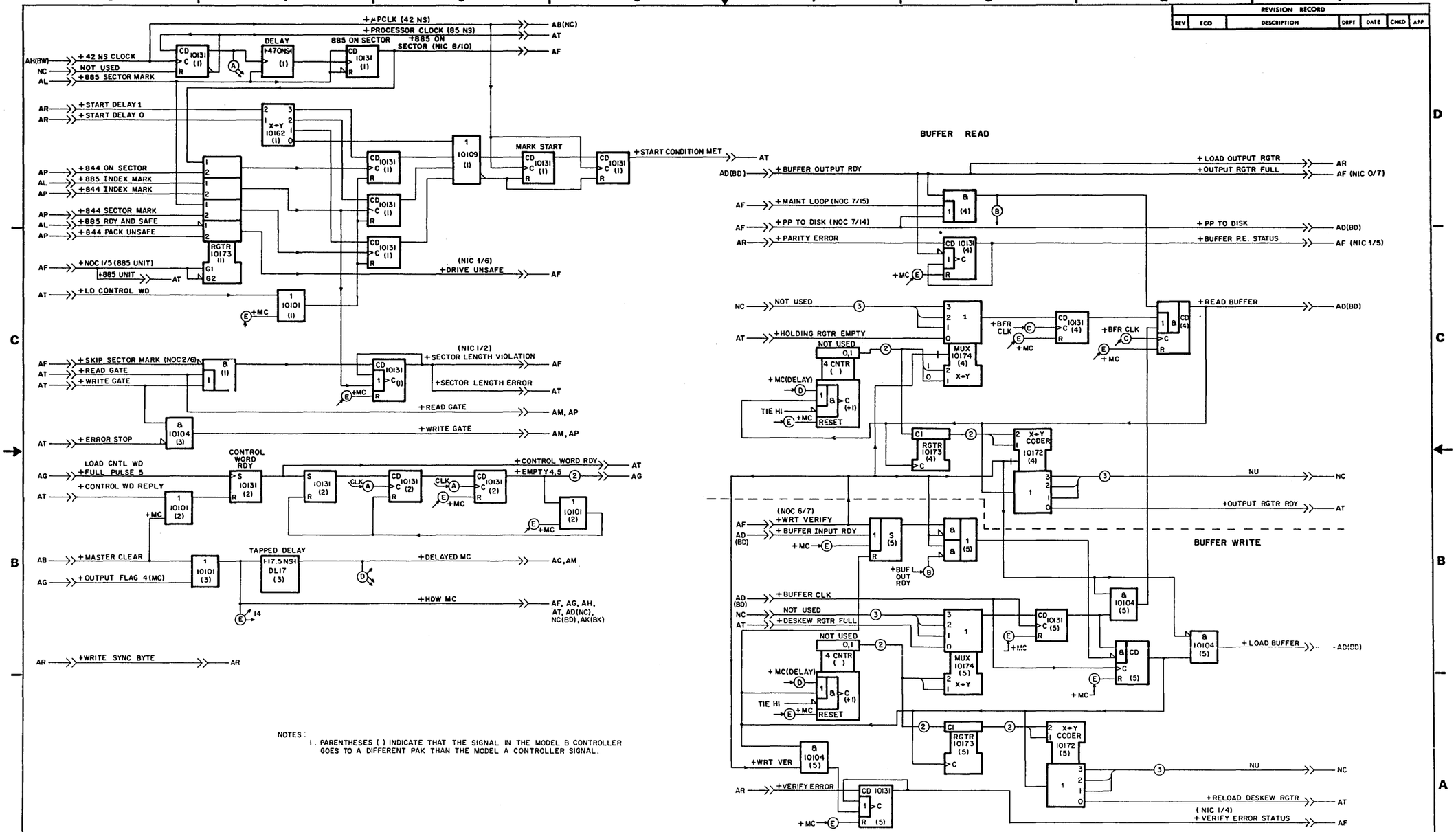
This flip-flop sets during a PP to disk buffer read operation to indicate that the holding register at B19/B20 (AR) has sent a byte into the shift register and can receive another byte from the output register. The +Read Buffer signal resets the Output Reg Full flip-flop at A15 (AD or BD), dropping the +Buffer Output Rdy signal. Logic on A15 (AD or BD) then reads the next buffer address and generates the +Output Rgtr Rdy signal. Note that some of the logic on this pak is not used; it is present for other applications only.

LOAD BUFFER FLIP-FLOP

The +Buffer Input Rdy signal indicates that buffer memory is ready to receive a data word to be written. When +Buffer Input Rdy and +Deskew Rgtr Full signals are both high, the +Load Buffer flip-flop sets, enabling the loading of another word into the buffer memory. The +Buffer Input Rdy signal drops until the buffer is ready to receive another data word.

+Lost Control Word (NIC1/8) sets if the bit counter decremented to zero (-Terminal Count low) and no new control word was available. A +Output Flag 5 signal must terminate a control word sequence.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



NOTES:
1. PARENTHESES ( ) INDICATE THAT THE SIGNAL IN THE MODEL B CONTROLLER GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CONTROL DATA ARDEN HILLS OPERATIONS	CONSOLIDATED LOGIC DIAGRAM BUFFER TO DATA PATH CONTROL	CODE IDENT 34010	D	DWG NO 60455690 REV R
TYPE: A5	LOC: B2I		SHEET	5-65

DATA PATH CONTROL (B22, AT)

DESKEW

Deskew 3 Full flip-flop sets when the deskew register at B19/B20 (AR) contains data and resets when it does not. +Reload Deskew Rgtr signal resets Deskew 3 Full flip-flop when a data byte has been sent from the deskew register to the buffer memory during a disk to PP buffer write. Note that some of the deskew control logic is not used; it is present for other applications only.

CONTROL WORD

The control word consists of 16 bits loaded by the processor from normal output channel 5. These bits are used to start or control some operation in the controller or disk. Control word sequences are controlled by logic at B19, B20 (AR), and B21 (AS) as well as on this pak. Control word sequence is as follows:

1. Processor places the appropriate count in NOC4/0-15 and sets +Full Pulse 4 signal. This sets the Ld Cnt flip-flop.
2. Processor sets appropriate bits in NOC5 and sets Full Pulse 5 signal. This sets the Control Word Rdy flip-flop at B21 (AS).
3. CW2 flip-flop sets.
4. -LD Control Wd and -LD Bit Count signals go low loading control word and bit count at B19/B20 (AR). The -Terminal Count signal must be low to enable the load signals. This indicates that the preceding control word sequence has been completed.
5. The +Control Word Reply signal resets the Control Word Ready flip-flop.
6. Seq In Progress flip-flop sets when the +Control Word Reply signal is generated.
7. The +Output Flag 5 (terminate) signal resets Seq In Progress flip-flop. This completes the control word sequence.

NOTE

The +Output Flag 5 (terminate) signal should never be sent before the +Full Pulse 4 signal, or a control word sequence may terminate prematurely. The terminate resets Seq In Progress flip-flop after the +Control Word Reply signal has been generated. Terminate could hang the processor if Seq In Progress flip-flop resets too soon.

READ/WRITE CONTROL

The byte counter and compare circuit work together to gate data into the deskew register at B19/B20 (AR) during a disk read, or to gate data into the shift register at B19/B20 during a disk write.

During a read, 12- or 16-bit bytes are assembled in the shift register from serial data. The byte counter counts the serial bits being transferred into the shift register. When the output of the counter matches the compare chip inputs (indicating 12 or 16 bits in the shift register), then this 12- or 16-bit byte is loaded into the deskew register, gated by the -Load Deskew Rgtr signal.

During a write, 12- or 16-bit bytes must be disassembled into serial data. A 12- or 16-bit byte is sent from the holding register at B19/B21 (AR) into the shift register. Serial data is shifted out of the shift register and sent to the disk. The byte counter and compare determine when the shift register can receive another byte from the holding register.

The +Lost Data (NIC1/1) signal sets if the buffer memory could not supply data to the shift register fast enough to keep up with the disk transfer rate or the buffer memory could not remove data from the shift register fast enough to keep up with the disk transfer rate. The +Lost Data signal halts a disk read or write.

CLOCK CONTROL

Bits 13 and 14 of the control word (selected by NOC5/13, 14) contain a code that selects one of three clocks used to drive sequence control and to provide clock pulses for the bit counter and shift register at AR, and the ECC register at AC. +Clk Sel 0 (bit 13) and +Clk Sel 1 (bit 14) provide the code on this pak as follows:

+Clk Sel 1	0	
L	L	+Wrt Clk from drive
L	H	+Rd Clk from drive
H	L	+Processor Clk
H	H	+Processor Clk

The clock period for these clocks is as follows:

+Processor Clock - 85 ns

885 Rd or Wrt Clk - 104 ns

844 Rd or Wrt Clk - 144 ns

When the clock selection changes, the clock pulses for the shift register and bit counter are blocked for the next two or three full clock periods.

The +Lost Clk signal goes high if disk read clock pulses or write clock pulses are not detected for 256 to 340 ns (three to four 85-ns processor clock periods). The reset pulse for the +Lost Clk signal timeout normally occurs every half cycle (42 ns for processor clock, 52 ns for 885 clocks, and 72 ns for 844 clocks).

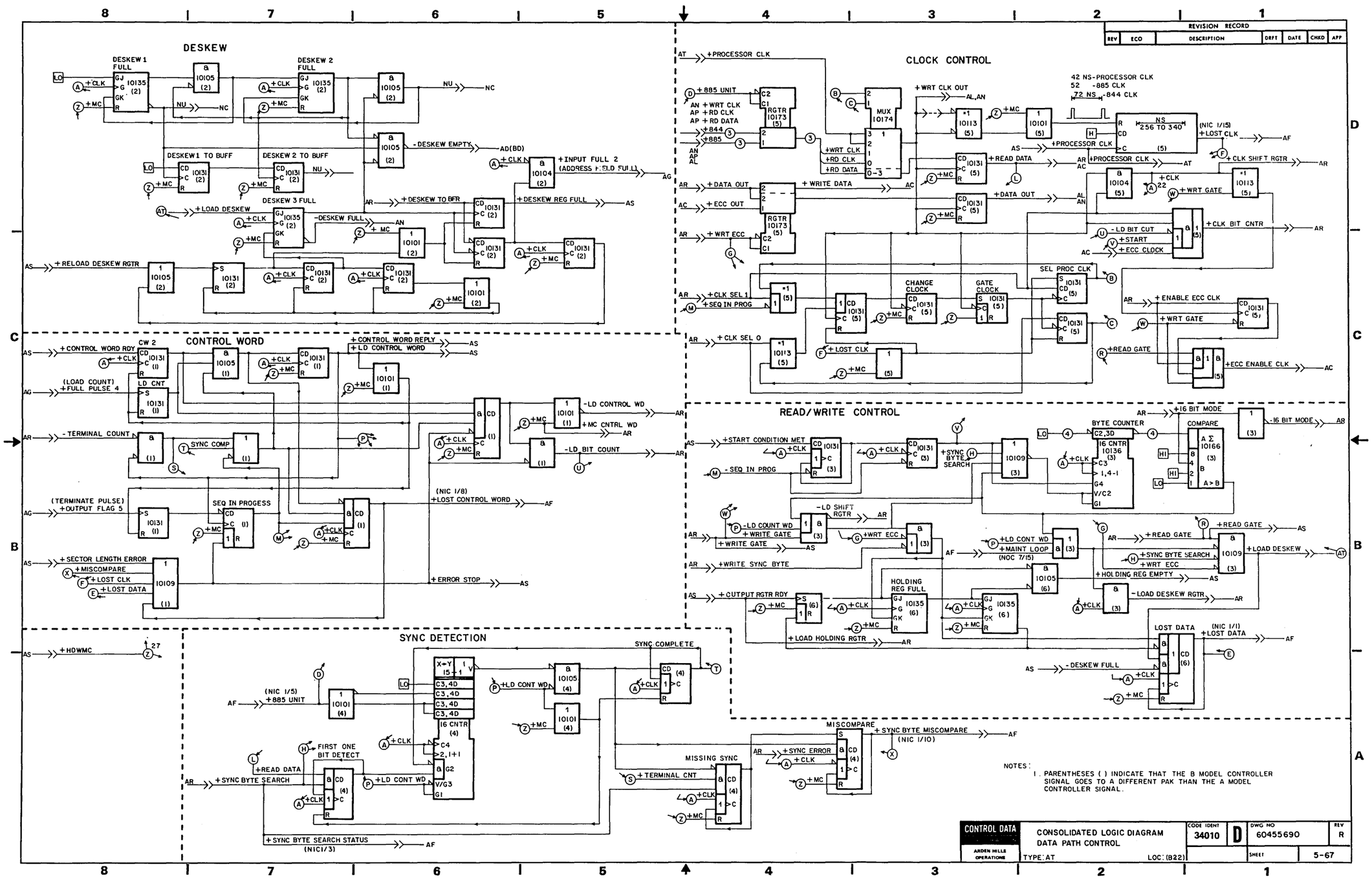
SYNC DETECTION

First one Bit Detect flip-flop sets when a sync byte search control word sequence is selected. The first one bit that the disk sends the controller sets the Read Data flip-flop. This enables the sync detection counter. The +Clk Pulse signal decrements the counter four counts for the 844 or three counts for the 885 before setting the Sync Complete flip-flop.

Two error conditions set Miscompare flip-flop.

- Missing Sync flip-flop sets if the bit counter decrements to zero during a sync byte search sequence but the controller has not detected a one bit.

- The +Sync Error signal goes high, indicating that the sync pattern checked at B19/B20 (AR) was incorrect.


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
DESKEW
DESKEW 1 FULL
DESKEW 2 FULL
DESKEW 3 FULL
DESKEW 1 TO BUFF
DESKEW 2 TO BUFF
+LOAD DESKEW
+RELOAD DESKEW RGTR
-DESKEW FULL
-DESKEW EMPTY
+DESKEW TO BFR
+DESKEW REG FULL
+INPUT FULL 2 (ADDRESS FIELD FULL)
CONTROL WORD
CW 2
+CONTROL WORD RDY
+CONTROL WORD REPLY
+LD CONTROL WORD
LD CNT
(LOAD COUNT) +FULL PULSE 4
- TERMINAL COUNT
SYNC COMP
-LD CONTROL WD
+MC CNTRL WD
-LD BIT COUNT
(TERMINATE PULSE) +OUTPUT FLAG 5
SEQ IN PROGESS
(NIC 1/8) +LOST CONTROL WORD
+SECTOR LENGTH ERROR
+MISCOMPARE
+LOST CLK
+LOST DATA
+ERROR STOP
CLOCK CONTROL
+PROCESSOR CLK
+885 UNIT
AN +WRT CLK
AP +RD CLK
AP +RD DATA
+844
+885
+WRT CLK OUT
42 NS-PROCESSOR CLK
52 -885 CLK
72 NS -844 CLK
+DATA OUT
+ECC OUT
+WRT ECC
+WRITE DATA
+READ DATA
+CLK SEL 1
+SEQ IN PROG
+CLK SEL 0
CHANGE CLOCK
GATE CLOCK
SEL PROC CLK
+ENABLE ECC CLK
+WRT GATE
+READ GATE
+ECC ENABLE CLK
-LD BIT CUT
+START
+ECC CLOCK
+CLK BIT CNTR
+CLK SHIFT RGTR
(NIC 1/15) +LOST CLK
READ/WRITE CONTROL
+START CONDITION MET
- SEQ IN PROG
-LD SHIFT RGTR
-LD COUNT WD
+WRITE GATE
+WRITE SYNC BYTE
+OUTPUT RGTR RDY
+LOAD HOLDING RGTR
HOLDING REG FULL
+HOLDING REG EMPTY
-LOAD DESKEW RGTR
+LOAD DESKEW
+SYNC BYTE SEARCH
+WRT ECC
+LD CONT WD
+MAINT LOOP
(NOC 7/15)
BYTE COUNTER
16 CNTR 10136
COMPARE
+16 BIT MODE
-16 BIT MODE
LOST DATA
(NIC 1/1) +LOST DATA
-DESKEW FULL
SYNC DETECTION
+HDWMC
SYNC COMPLETE
(NIC 1/5) +885 UNIT
FIRST ONE BIT DETECT
+READ DATA
+SYNC BYTE SEARCH
+LD CONT WD
+SYNC BYTE SEARCH STATUS (NIC1/3)
MISSING SYNC
+TERMINAL CNT
MISCOMPARE
+SYNC ERROR
+SYNC BYTE MISCOMPARE (NIC 1/10)
NOTES:
1. PARENTHESES ( ) INDICATE THAT THE B MODEL CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE A MODEL CONTROLLER SIGNAL.
CONTROL DATA
ARDEN HILLS OPERATIONS
CONSOLIDATED LOGIC DIAGRAM
DATA PATH CONTROL
TYPE: AT
LOC: (B22)
CODE IDENT 34010
D
DWG NO 60455690
REV R
SHEET 5-67

BUFFER CONTROL (A15, AD) - Model A Controller

BUFFER CONTROL (A15, BD) - Model B Controller

This pak controls data transfers into and out of the buffer memory. In the model A controller, the buffer memory has a capacity of 2048 16-bit words, and is located at A23, A24, A25, and A26 (AJ). In the model B controller, the buffer memory holds 4096 16-bit words at locations A24 and A26 (BJ). NIC 9/4 indicates that the buffer memory is 4-K.

Buffer control deals with four data transfer paths - PP to disk operation buffer write, PP to disk operation buffer read, disk to PP operation buffer write, and disk to PP operation buffer read.

Before any buffer memory data transfer, the up/down counter must be loaded by the processor from normal output channel 7, bits 0 through 11. Whenever a word is written into the memory, this counter increments; whenever a word is read from the memory, the counter decrements. If the counter decrements to zero, the buffer read terminates to prevent attempting to read more data than has been written. NIC1/7 reflects the zero or nonzero state of the counter.

The processor loads the write address counter from normal output channel 6 before starting a buffer memory write operation. The counter provides the buffer memory address during a write and is incremented by 1 after each byte has been written.

The processor loads the read address counter from normal output channel 6 before starting a buffer memory read operation. The counter provides the buffer memory address during a read and is incremented by 1 after each byte has been read.

The sequence of events for buffer read and buffer write operations (as they pertain to this pak) follow.

PP TO DISK

The sequence of events for a buffer write:

1. Processor must establish initial conditions:
   a. Output flag 7 sets reserved flip-flop.
   b. Load write address and up/down counters.
   c. Set PP to disk bit (NOC7/14) and set disable processor to buffer bit (NOC7/13).
   d. Clear load bit (NOC6/15).
2. PP sends Full signal that sets Full Catch flip-flop.
3. Send Empty flip-flop sets at -T2. This resets Full Catch flip-flop and generates a +Bfr Empty signal. A +Bfr Empty signal causes a +Empty signal to be returned to the connected PP in response to the Full signal from the PP.
4. Catching Reg Full flip-flop sets at +T1. This resets the +Send Empty flip-flop, sets the Write Enable flip-flop, and enables +Buff Mem 0-11 signals data byte into the catching register.
5. Up/down counter and write address counter increment.

Steps 2 through 5 repeat until the PP completes the data transfer.

The sequence of events for a buffer read:

1. Same as step 1 for buffer write except that the read address counter must be loaded.
2. Enable Output Rgtr flip-flop sets, allowing the read address counter to increment and the up/down counter to decrement at +T1.
3. Output Reg Full flip-flop sets generating a +Buffer Output Rdy signal. This resets the Enable Output Rgtr flip-flop.
4. Read Buffer flip-flop sets, indicating that the output register at B19 and B20 (AR) can accept another data byte. This resets the Output Reg Full flip-flop.

Steps 2 through 4 repeat until the operation finishes.

DISK TO PP

The sequence of events for a buffer write:

1. Processor must establish initial conditions:
   a. NOC7/14 must be clear to select the disk-to-PP path.
   b. Processor loads write address and up/down counters.
2. Load Buffer flip-flop sets, indicating that the buffer input register (at AJ or BJ) can receive data.
3. Catching Reg Full sets, gating -Deskew 0-15 signals into the catching register.
4. Write Enable flip-flop sets.
5. Buffer Input Rdy flip-flop sets.
6. Write address counter increments and Catching Reg Full flip-flop resets.

Steps 2 through 6 repeat until the processor terminates the operation.

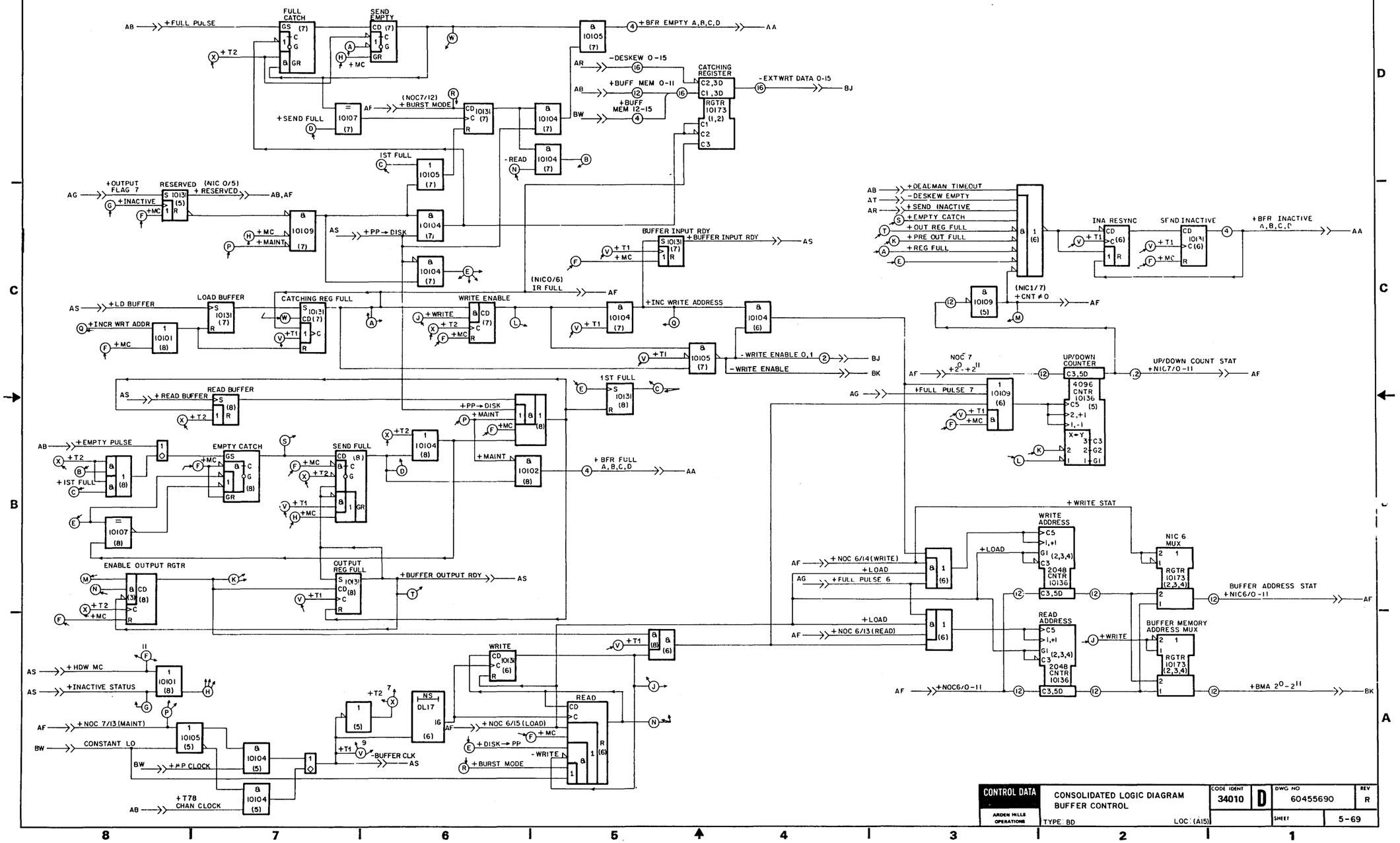
The sequence of events for a buffer read:

1. Same as step 1 for buffer write except read address counter must be loaded.
2. 1st Full flip-flop sets.
3. Empty Catch flip-flop sets.
4. Send Full flip-flop sets.
5. Enable Output Rgtr flip-flop sets.

6. Read address counter increments and up/down counter decrements.
7. +Out Reg Full signal sets. This resets Enable Output Rgtr flip-flop.
8. Buffer Output Rdy signal enables loading the output.
9. Register at B19 and B20 (AR) is loaded.
10. Read Buffer flip-flop sets. This resets 1st Full and Output Reg Full flip-flops.
11. Full data sent to PP.
12. PP sends empty pulse. This sets (indirectly) Empty Catch flip-flop.

Steps 4 through 12 repeat until the PP or processor terminates the operation.

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



CONTROL DATA	CONSOLIDATED LOGIC DIAGRAM BUFFER CONTROL	CODE IDENT		DWG NO	REV
ARDEN HILLS OPERATIONS	TYPE: BD LOC: (A15)	34010	D	60455690	R
			SHEET	5-69	

4-BIT SLICE PROCESSOR (A23, A24, A25, A26, AJ) - Model A Controller

8-BIT SLICE PROCESSOR (A24, A26, BJ) - Model B Controller

These 60-paks comprise the central part of the processor. In the model A controller, each of the four paks is dedicated to four bits of the 16-bit processor word. The bits are distributed as follows:

Bits 0 through 3	A26	Slice 1
Bits 4 through 7	A25	Slice 2
Bits 8 through 11	A24	Slice 3
Bits 12 through 15	A23	Slice 4

In the model B controller, both paks are dedicated to eight bits of the 16-bit processor word. The bits are distributed as follows:

Bits 0 through 7	A26	Slice 1
Bits 8 through 15	A24	Slice 2

The paks contain the following circuits.

PROGRAM RAM

This 4096-word, 16-bit-per-word RAM stores controlware. Addresses from 0000_8 to 7777_8 select this memory. The P register LEDs indicate the address selected. The LEDs are located at A23 through A26 in the model A controller and at A27 on the model B controller.

BUFFER MEMORY

The buffer memory provides 2048 words of RAM for the model A controller and 4096 words RAM for the model B controller. Addresses 10000_8 through 13777_8 in the model A controller and 10000_8 through 17777_8 in the model B controller select this memory.

Buffer memory provides a temporary storage area during disk data transfers.

PARITY

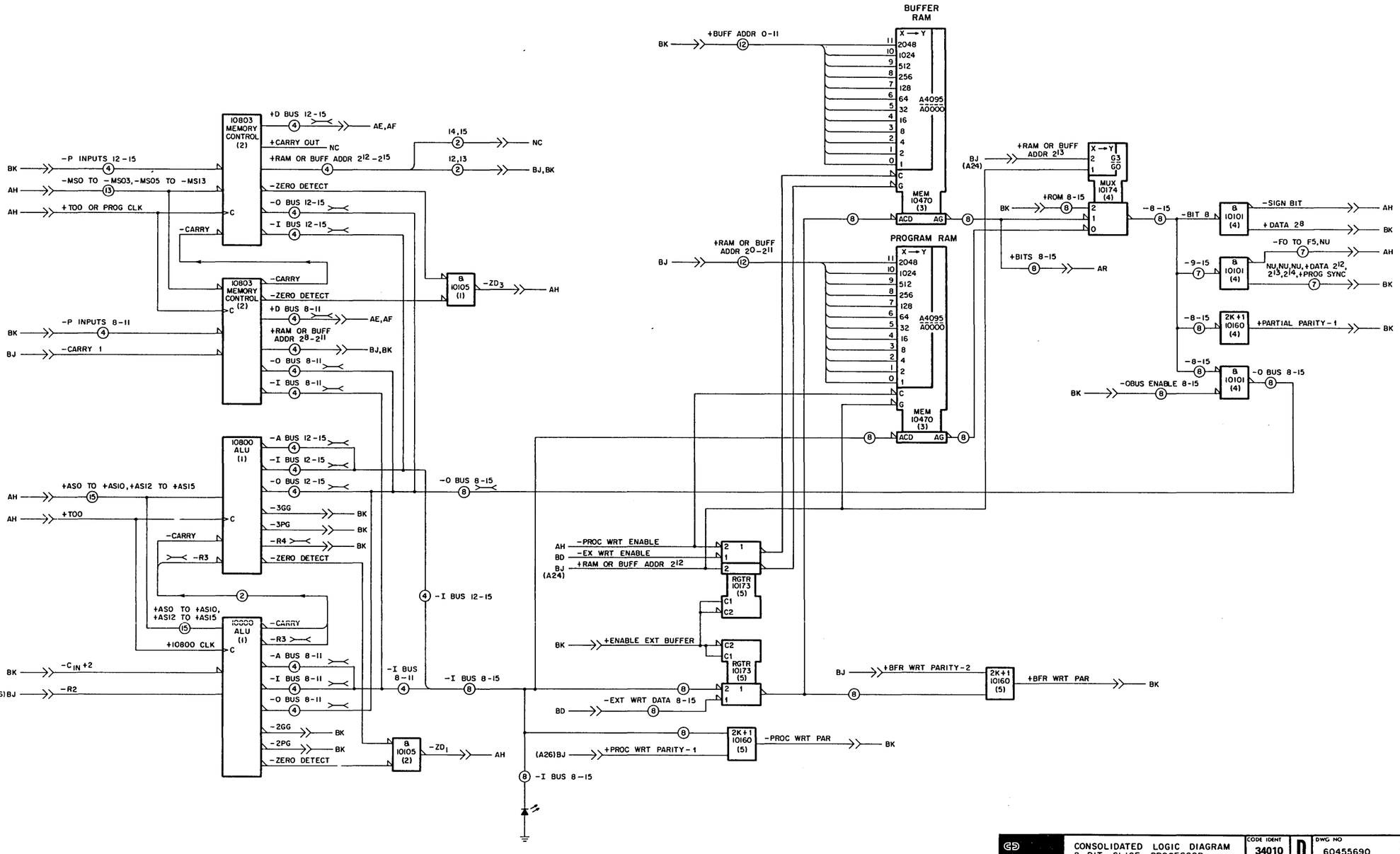
The processor generates a parity bit for each byte written into the buffer and program RAM. Odd parity is used. The program memory parity bit is produced at location A25 (+Parity Data 1 signal). This parity bit is stored in the RAM at location A27. Setting NOC1/12 forces a program memory parity error.

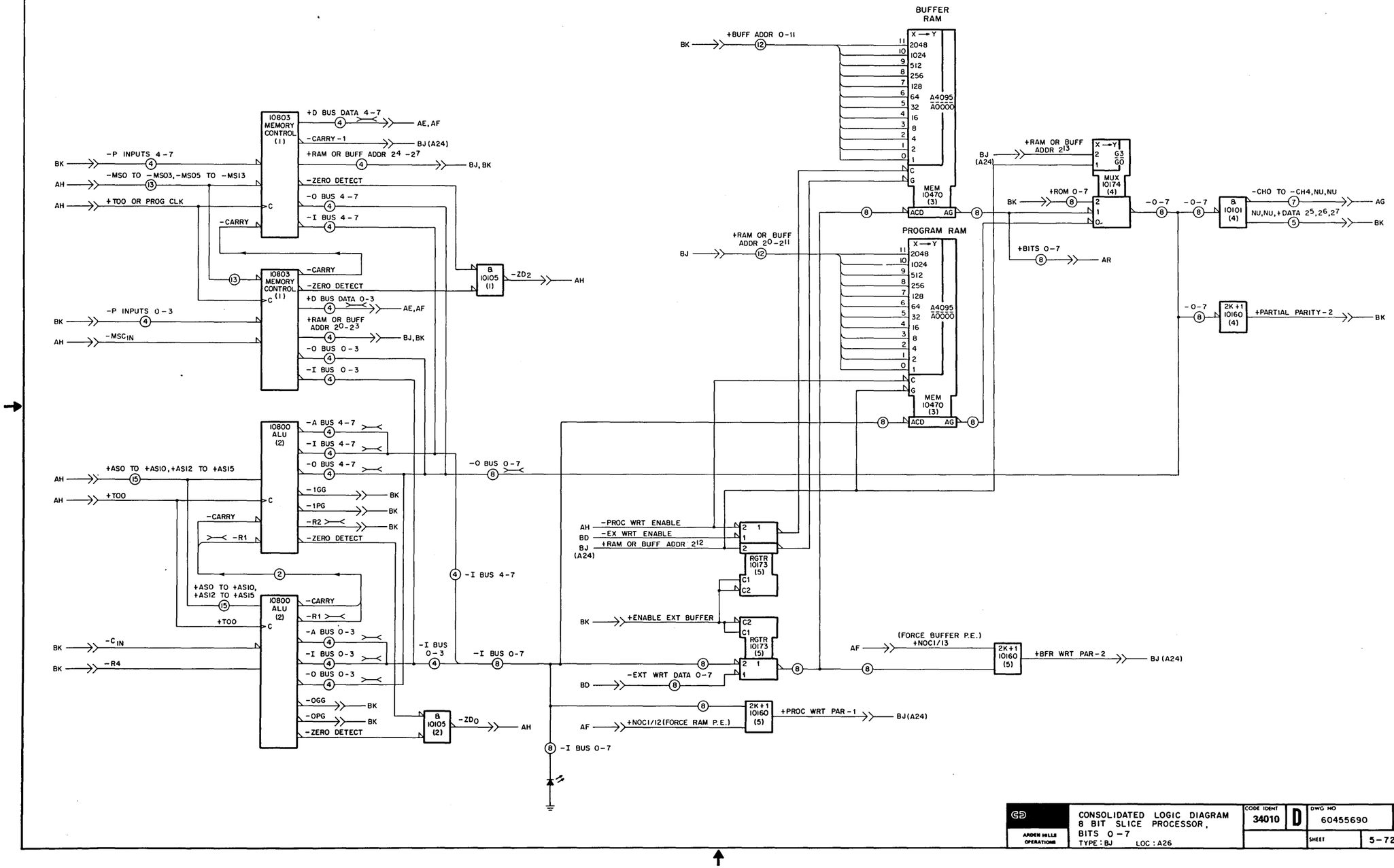
The buffer memory parity bit is produced at location A24 (+Parity Data 2 signal). It is written into the buffer parity memory chip at location A27. Setting NIC1/13 forces a buffer memory parity error.

Parity checking is done at locations A26 and A27.

10800 - This microprocessor chip provides general hardware control in the processor.

10803 - This microprocessor chip performs the ALU function in the processor. It uses the D bus to set bits on the processor output channels and to read status from the processor input channels.


10803 MEMORY CONTROL (2)
+D BUS 12-15
AE,AF
+CARRY OUT
NC
+RAM OR BUFF ADDR 2^12-2^15
14,15
NC
12,13
BJ,BK
-P INPUTS 12-15
-MSO TO -MS03, -MS05 TO -MS13
+TOO OR PROG CLK
-CARRY
-ZERO DETECT
-O BUS 12-15
-I BUS 12-15
B 10105 (1)
-ZD3
AH
10803 MEMORY CONTROL (2)
-P INPUTS 8-11
-CARRY 1
+D BUS 8-11
+RAM OR BUFF ADDR 2^8-2^11
-O BUS 8-11
-I BUS 8-11
10800 ALU (1)
-A BUS 12-15
+ASO TO +AS10, +AS12 TO +AS15
+TOO
-3GG
-3PG
-R4
-R3
+10800 CLK
10000 ALU (1)
-A BUS 8-11
-C IN +2
-R2
-2GG
-2PG
B 10105 (2)
-ZD1
-I BUS 8-11
-I BUS 8-15
-O BUS 8-15
BUFFER RAM
+BUFF ADDR 0-11
MEM 10470 (3)
A4095 A0000
PROGRAM RAM
+RAM OR BUFF ADDR 2^0-2^11
+RAM OR BUFF ADDR 2^13
BJ (A24)
MUX 10174 (4)
+ROM 8-15
+BITS 8-15
AR
-8-15
-BIT 8
B 10101 (4)
-SIGN BIT
+DATA 2^8
-FO TO F5, NU
-9-15
NU,NU,NU,+DATA 2^12, 2^13,2^14,+PROG SYNC
2K+1 10160 (4)
+PARTIAL PARITY-1
-OBUS ENABLE 8-15
-PROC WRT ENABLE
-EX WRT ENABLE
+RAM OR BUFF ADDR 2^12
RGTR 10173 (5)
+ENABLE EXT BUFFER
-EXT WRT DATA 8-15
+BFR WRT PARITY-2
+BFR WRT PAR
+PROC WRT PARITY-1
-PROC WRT PAR
CONSOLIDATED LOGIC DIAGRAM
8 BIT SLICE PROCESSOR,
BITS 8-15
TYPE: BJ LOC: A24
ARDEN HILLS OPERATIONS
CODE IDENT 34010
D
DWG NO 60455690
REV R
SHEET 5-71


BUFFER RAM
PROGRAM RAM
10803 MEMORY CONTROL (1)
10800 ALU (2)
MEM 10470 (3)
MUX 10174 (4)
RGTR 10173 (5)
8 10105 (1)
8 10101 (4)
2K+1 10160 (4)
2K+1 10160 (5)
A4095 A0000
+BUFF ADDR 0-11
+RAM OR BUFF ADDR 20-211
+RAM OR BUFF ADDR 213
+ROM 0-7
+BITS 0-7
-CHO TO -CH4,NU,NU
NU,NU,+DATA 25,26,27
+PARTIAL PARITY-2
-P INPUTS 4-7
-MSO TO -MSO3,-MSO5 TO -MSI3
+TOO OR PROG CLK
-CARRY
+D BUS DATA 4-7
-CARRY-1
+RAM OR BUFF ADDR 24-27
-ZERO DETECT
-O BUS 4-7
-I BUS 4-7
-ZD2
-P INPUTS 0-3
-MSCIN
+D BUS DATA 0-3
+RAM OR BUFF ADDR 20-23
-O BUS 0-3
-I BUS 0-3
-A BUS 4-7
-1GG
-1PG
-R2
-R1
+ASO TO +ASI0,+ASI2 TO +ASI5
+TOO
-CIN
-R4
-A BUS 0-3
-OGG
-OPG
-ZDO
-O BUS 0-7
-I BUS 0-7
-PROC WRT ENABLE
-EX WRT ENABLE
+RAM OR BUFF ADDR 212
+ENABLE EXT BUFFER
-EXT WRT DATA 0-7
(FORCE BUFFER P.E.) +NOC1/13
+BFR WRT PAR-2
+NOC1/12(FORCE RAM P.E.)
+PROC WRT PAR-1
AE,AF
BJ(A24)
BJ,BK
AH
BK
BJ
BD
AF
AR
AG
-0-7
-I BUS 0-3
-I BUS 4-7
CONSOLIDATED LOGIC DIAGRAM
8 BIT SLICE PROCESSOR,
BITS 0-7
TYPE : BJ LOC : A26
ARDEN HILLS OPERATIONS
CODE IDENT 34010
D
DWG NO 60455690
REV R
SHEET 5-72

PROGRAM ROM, PARITY RAM (A27, AK) - Model A Controller

PROGRAM ROM FOR 8-BIT SLICE (A27, BK) - Model B Controller

PROGRAM ROM

The program ROM has a capacity of 1024 16-bit words. The ROM contains an autoload subroutine, some function routines, and some rudimentary diagnostics. Addresses 20000_8 to 21777_8 select the program ROM.

PROGRAM MEMORY PARITY RAM

This RAM contains the parity bit for the 4096 16-bit words in the program memory RAM. The same address is used for both the program memory and the parity RAM.

LOOK AHEAD CARRY

The propagate and generate outputs from the 10800 chips are sent to the look-ahead carry ALU chip. This is a time-saving device to determine whether a carry will be generated in the 10800.

PARITY ERROR

A high from the read parity check circuit indicates that an error has been detected during a read from the program ROM, program RAM, or buffer memory. Because the program ROM uses addresses 20000_8 to 21777_8, +RAM or Buff Addr 2^{13} signal enables the ROM P.E. signal.

STROBE C

When low, this signal strobes the processor channel number into the channel number register at A21. This goes low when the -P.E. Strobe signal goes low and when a +RNI signal is high during a 6X or 7X instruction.

DATA ECHO

The +Data Echo signal goes high when bit 2^8 is high during a 70 instruction. +Data Echo causes the processor output channels to loop back into the respective input channel.

PROGRAM SYNC

Testpoint 50 reflects the state of bit 15 of all processor instructions. Bit 15 is not used for the instructions but can be set or cleared from the console for maintenance purposes.

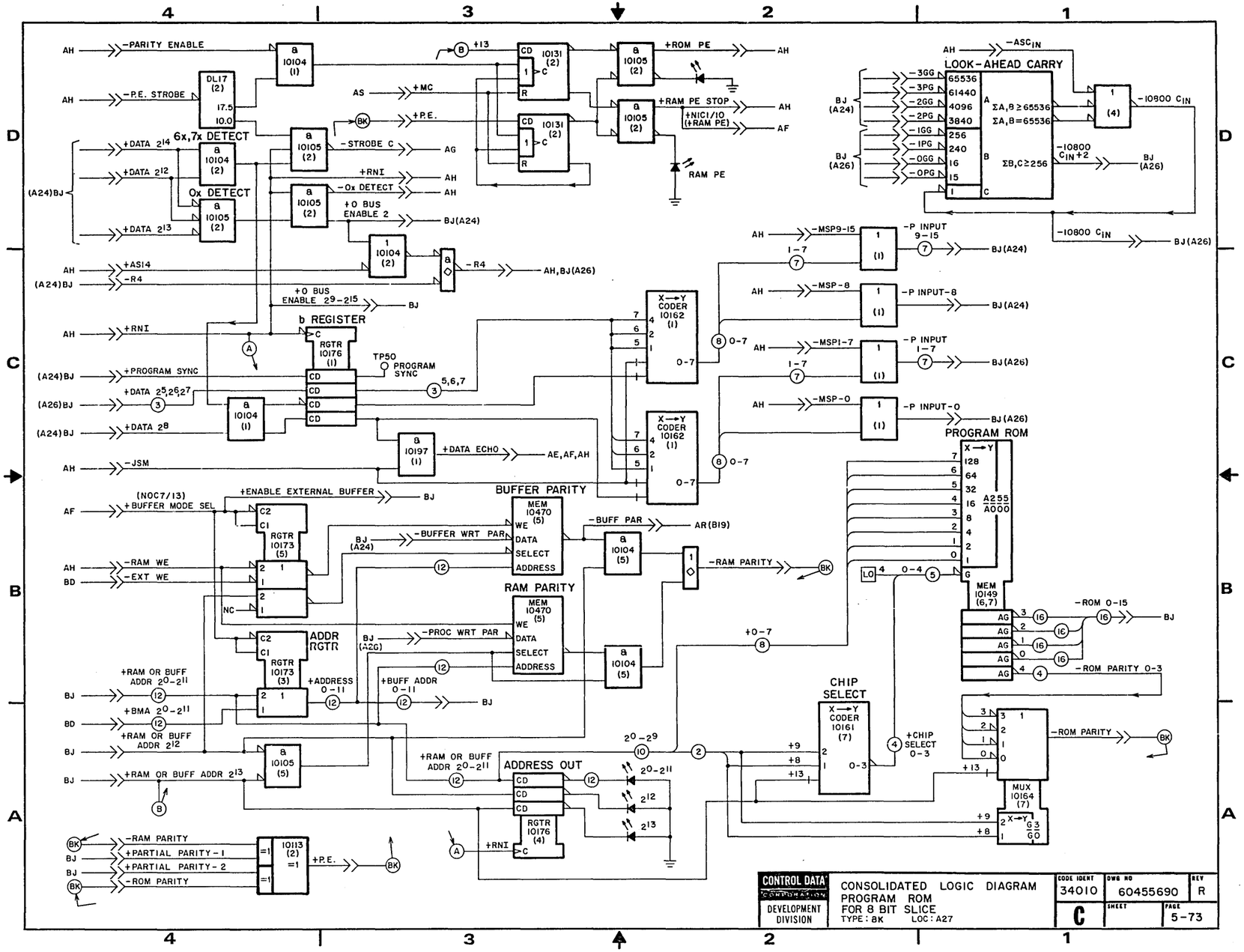
-P INPUTS 0-15

These signals set up a mask that is used by the 10803 chip. During a 76 or 77 instruction, the -JSM signal enables the coder to determine the contents of the -P Input signals. Any other time the -MSP0, -MSP1-7, -MSP8, and -MSP9-15 signals from control memory determine the -P Input signal.

-Ox DETECT

The $-O_x$ Detect signal goes low when memory sends an O_x (jump type) instruction. This signal modifies the control memory address causing a branch operation in certain conditions.

This signal also enables the -R4 signals that are used for an end-around shift in the 10800 chips. The -R4 signals also modify the control memory address.


4
3
2
1
D
C
B
A
AH
-PARITY ENABLE
8 10104 (1)
-P.E. STROBE
DL17 (2)
17.5
10.0
6x,7x DETECT
+DATA 2^14
+DATA 2^12
+DATA 2^13
(A24)BJ
8 10104 (2)
0x DETECT
8 10105 (2)
+B
+13
CD 10131 (2)
1
C
R
AS
+MC
BK
+P.E.
-STROBE C
AG
+RNI
-0x DETECT
+0 BUS ENABLE 2
BJ(A24)
8 10105 (2)
+ROM PE
+RAM PE STOP
+NICI/IO (+RAM PE)
AF
RAM PE
1 10104 (2)
-R4
AH,BJ(A26)
+AS14
+0 BUS ENABLE 29-215
BJ
b REGISTER
RGTR 10176 (1)
CD
TP50
PROGRAM SYNC
5,6,7
+PROGRAM SYNC
+DATA 25,26,27
(A26)BJ
+DATA 28
8 10104 (1)
8 10197 (1)
+DATA ECHO
AE,AF,AH
-JSM
(NOC7/13)
+BUFFER MODE SEL
+ENABLE EXTERNAL BUFFER
BUFFER PARITY
MEM 10470 (5)
WE
DATA
SELECT
ADDRESS
-BUFF PAR
AR(B19)
RGTR 10173 (5)
C2
C1
-BUFFER WRT PAR
-RAM WE
-EXT WE
BD
NC
8 10104 (5)
1
-RAM PARITY
BK
RAM PARITY
ADDR RGTR
-PROC WRT PAR
RGTR 10173 (3)
+RAM OR BUFF ADDR 20-211
+BMA 20-211
+RAM OR BUFF ADDR 212
+RAM OR BUFF ADDR 213
+ADDRESS 0-11
+BUFF ADDR 0-11
8 10105 (5)
ADDRESS OUT
RGTR 10176 (4)
+RNI
20-211
212
213
20-29
X→Y CODER 10162 (1)
0-7
8 0-7
+0-7
CHIP SELECT
X→Y CODER 10161 (7)
0-3
+CHIP SELECT 0-3
+9
+8
+13
LOOK-AHEAD CARRY
-ASC IN
-3GG
-3PG
-2GG
-2PG
-1GG
-1PG
-0GG
-0PG
65536
61440
4096
3840
256
240
16
15
ΣA,B≥65536
ΣA,B=65536
ΣB,C≥256
1 (4)
-10800 CIN
-10800 CIN+2
-10800 CIN
BJ (A24)
BJ (A26)
-MSP9-15
-P INPUT 9-15
-MSP-8
-P INPUT-8
-MSP1-7
-P INPUT 1-7
-MSP-0
-P INPUT-0
1-7
PROGRAM ROM
A255 A000
LO
0-4
MEM 10149 (6,7)
AG
-ROM 0-15
-ROM PARITY 0-3
-ROM PARITY
MUX 10164 (7)
X→Y G3 G0
-RAM PARITY
+PARTIAL PARITY-1
+PARTIAL PARITY-2
-ROM PARITY
10113 (2) =1
+P.E.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
PROGRAM ROM
FOR 8 BIT SLICE
TYPE: 8K LOC: A27
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
PAGE 5-73

CYBER MUX 2 (A07, BW)

CLOCK

The microprocessor pulse generator (A22) sends the +42 NS CLOCK pulse. The +u PROC CLC signal follows the setting and clearing of the flip-flops.

SUBSYSTEM ID SWITCHES

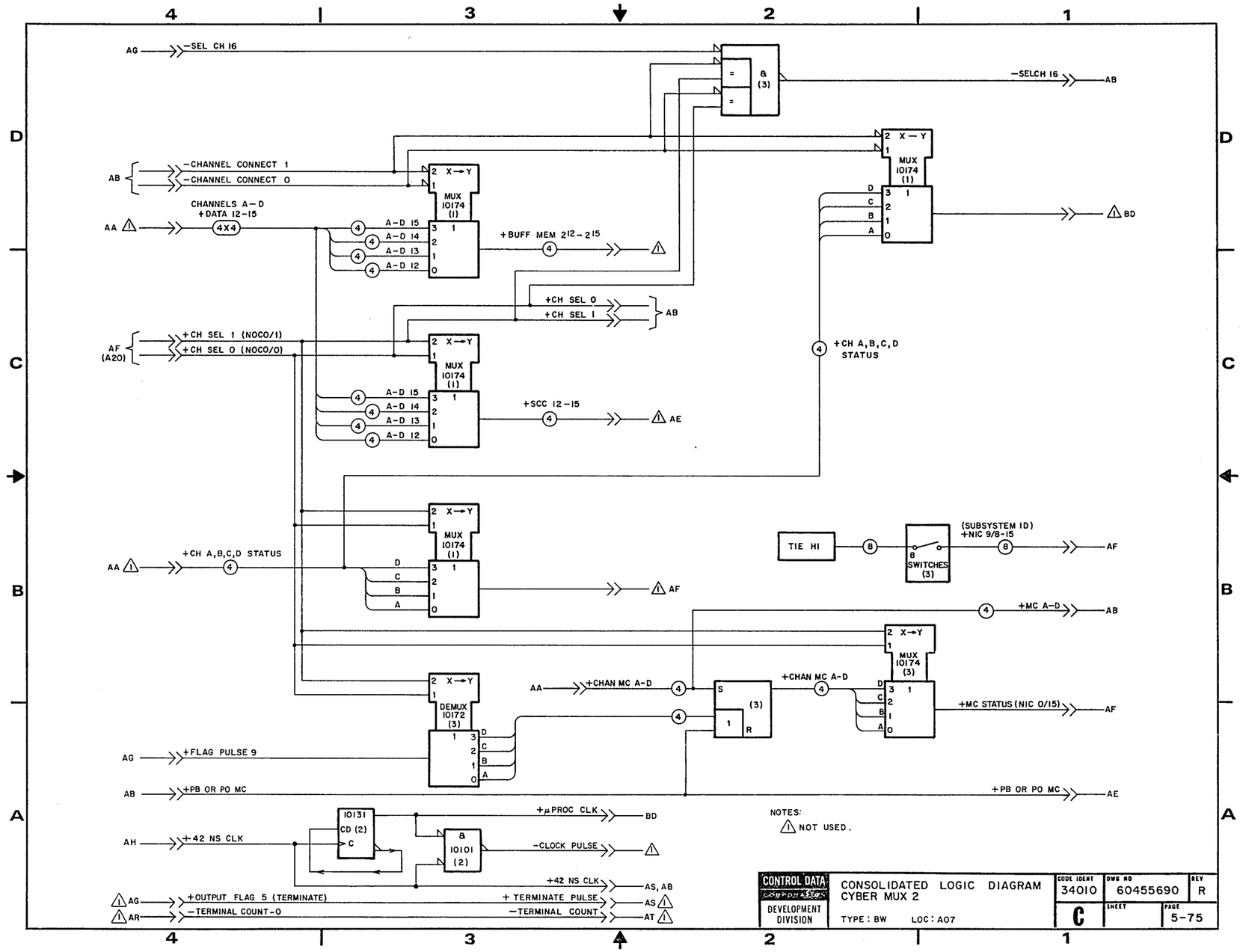
The eight ID switches provide a unique subsystem identification number. This identification number identifies the subsystem status sent to the PP.

SEL CH 16

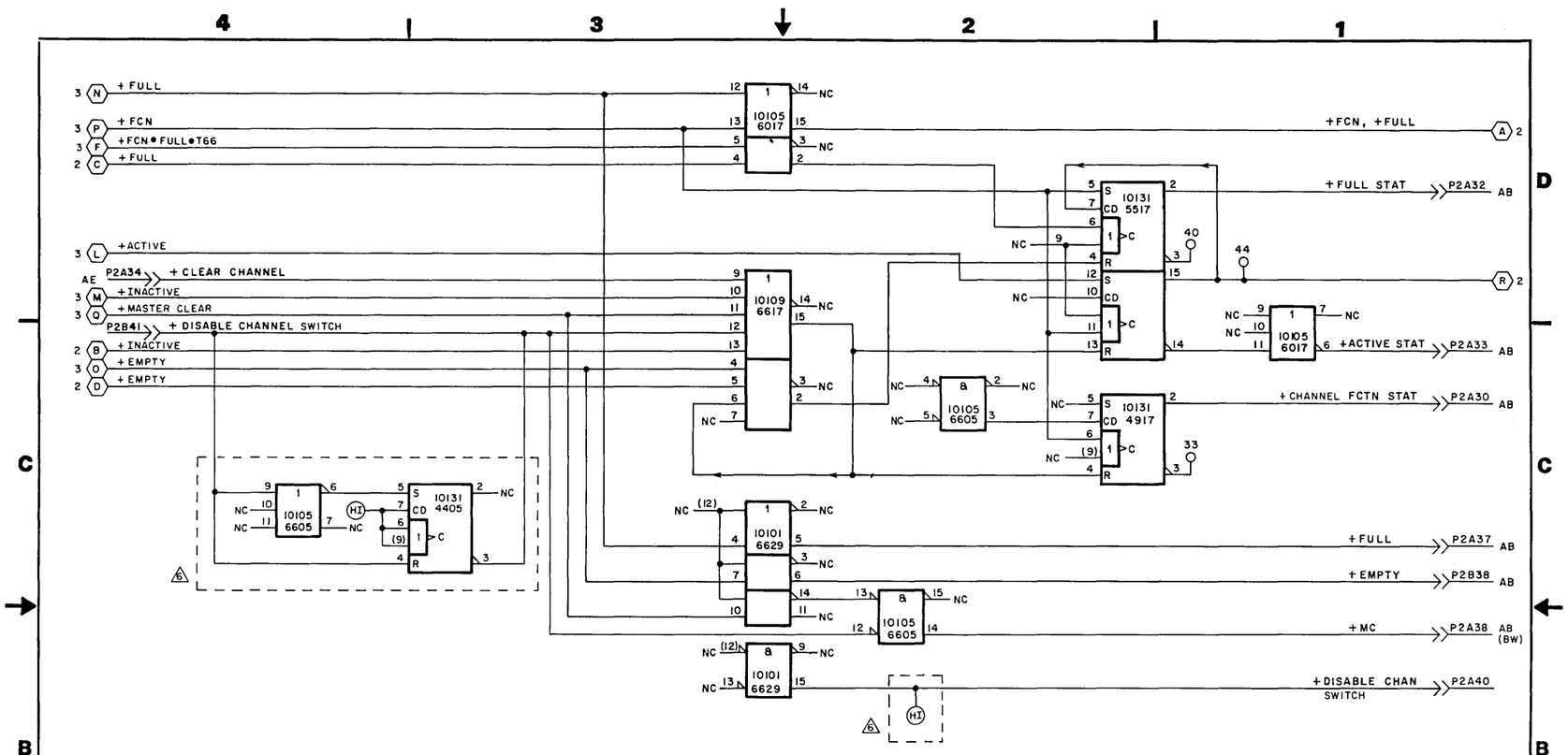
The processor selects the special channel, channel 16, to communicate directly with the PP via the I/O channel. Selection of this channel is enabled only when the PP channel connected to the controller matches the PP channel selected by the processor in NOC 0/0,1.

MC STATUS

A master clear from the PP sets a flip-flop on A07. The processor selection of the channel access code (NOC 0/0,1) and checking of the MC status (NIC 0/15) indicates whether the flip-flop set.


AG
-SEL CH 16
8 (3)
-SELCH 16
AB
MUX 10174 (1)
AB
-CHANNEL CONNECT 1
-CHANNEL CONNECT 0
CHANNELS A-D +DATA 12-15
AA
4X4
A-D 15
A-D 14
A-D 13
A-D 12
+BUFF MEM 212-215
BD
+CH SEL 0
+CH SEL 1
AB
AF (A20)
+CH SEL 1 (NOCO/1)
+CH SEL 0 (NOCO/0)
+CH A,B,C,D STATUS
+SCC 12-15
AE
AF
+CH A,B,C,D STATUS
TIE HI
8 SWITCHES (3)
(SUBSYSTEM ID) +NIC 9/8-15
+MC A-D
DEMUX 10172 (3)
+CHAN MC A-D
S
R
+MC STATUS (NIC 0/15)
+FLAG PULSE 9
+PB OR PO MC
10131 CD (2)
+μPROC CLK
+42 NS CLK
-CLOCK PULSE
+OUTPUT FLAG 5 (TERMINATE)
-TERMINAL COUNT-0
+TERMINATE PULSE
-TERMINAL COUNT
AS, AB
AS
AT
NOTES:
NOT USED.
CONTROL DATA
DEVELOPMENT DIVISION
CONSOLIDATED LOGIC DIAGRAM
CYBER MUX 2
TYPE: BW
LOC: A07
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
PAGE 5-75

LOGIC DIAGRAMS



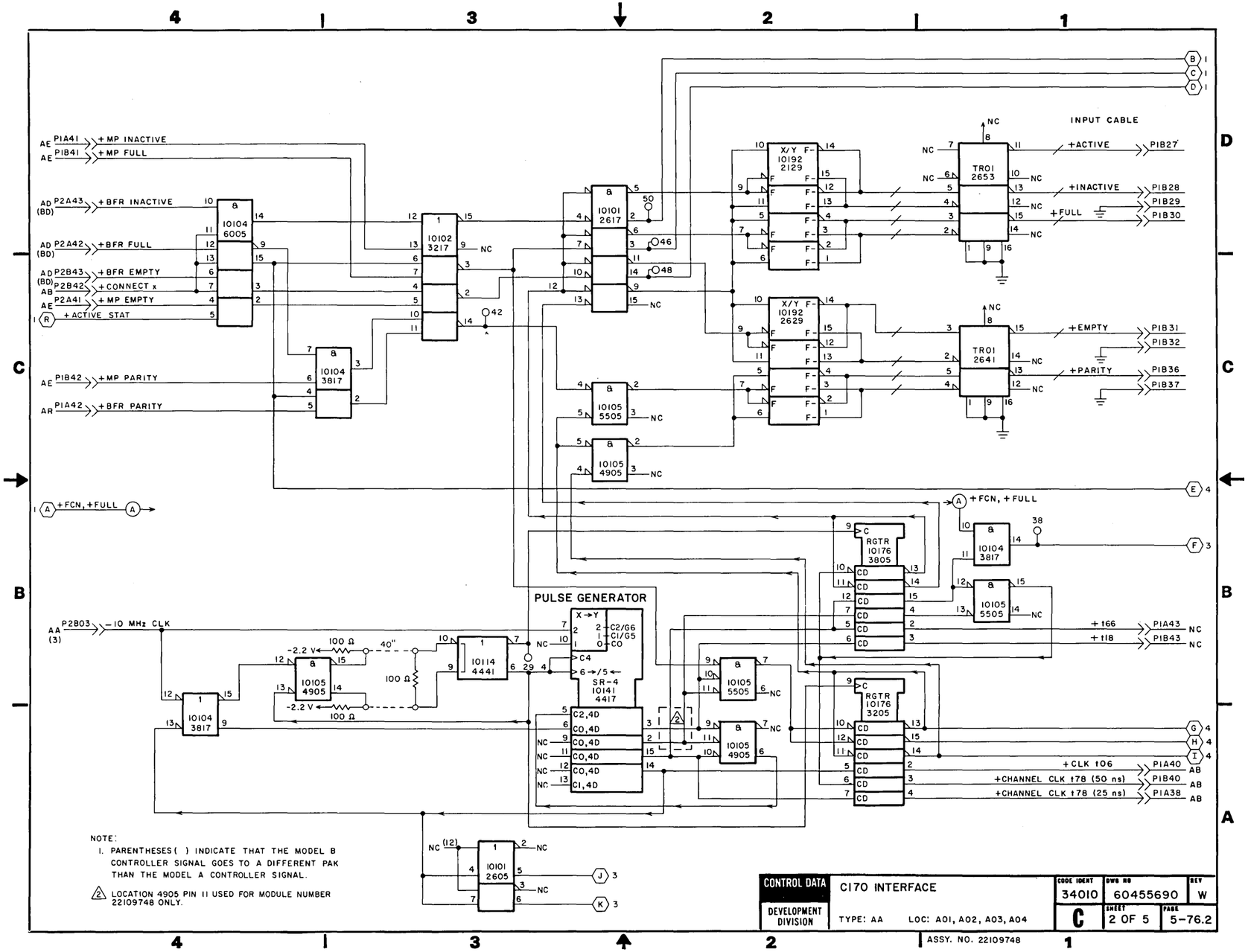
NOTES:

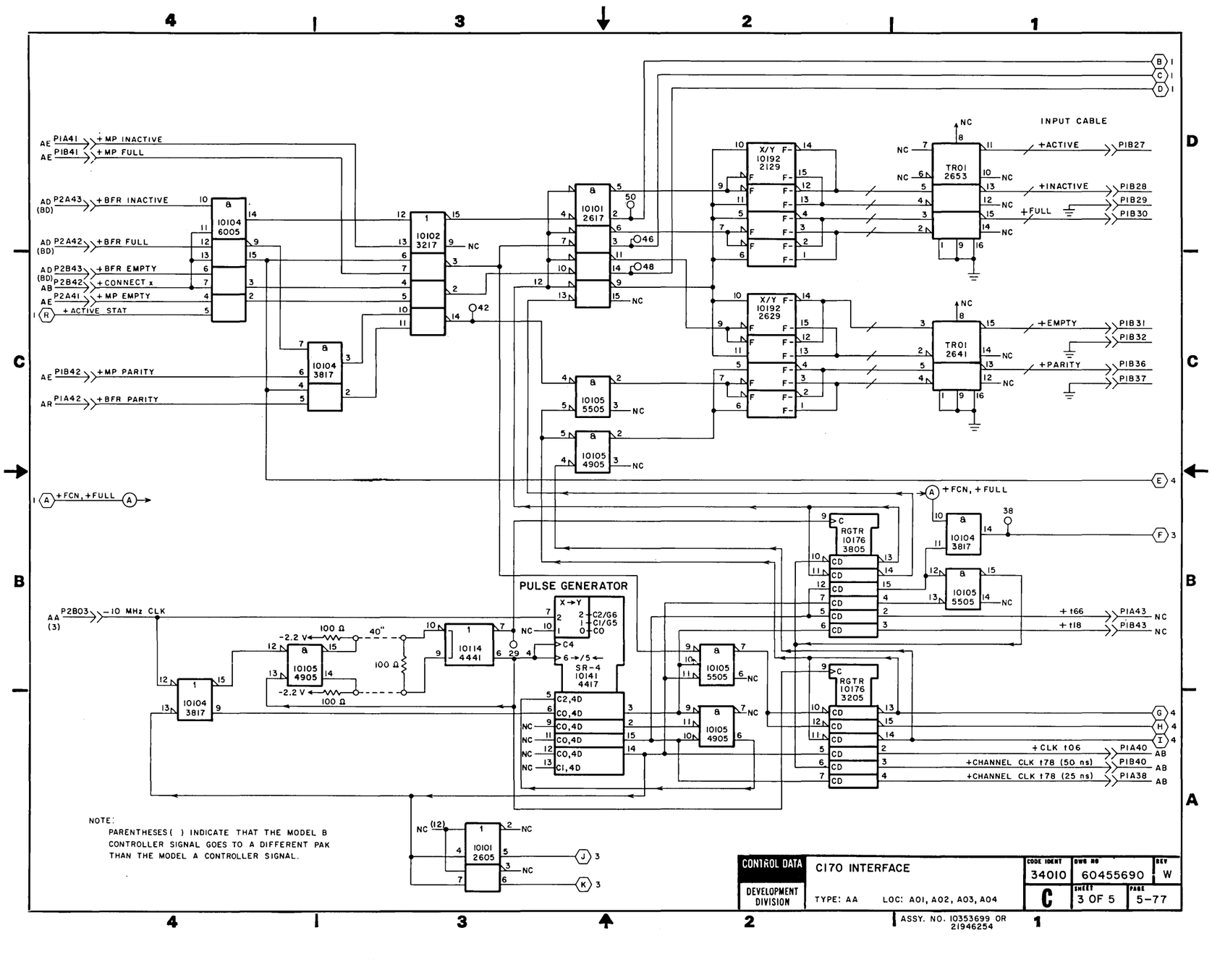
1. ON ALL TRO2, PIN 1 IS OPEN PIN 8 IS TIED TO -5.2V, AND PINS 3,5,7,16 ARE TIED TO GROUND. INPUT LINES ARE NOT TERMINATED.
2. ON ALL TRO1, PINS 1,9,16 ARE TIED TO GROUND, PIN 8 IS OPEN, AND INPUT LINES ARE NOT TERMINATED.
3. A01 = CHANNEL A
   A02 = CHANNEL B
   A03 = CHANNEL C
   A04 = CHANNEL D
4. LOCATION A01 MUST BE OCCUPIED AT ALL TIMES IN THE MODEL A CONTROLLER BECAUSE TERMINATORS (ON SHEET 4) ARE USED AT A01 ONLY. THESE INPUTS ARE NOT USED IN THE MODEL B CONTROLLER, WHICH IS TERMINATED AT A07.
5. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

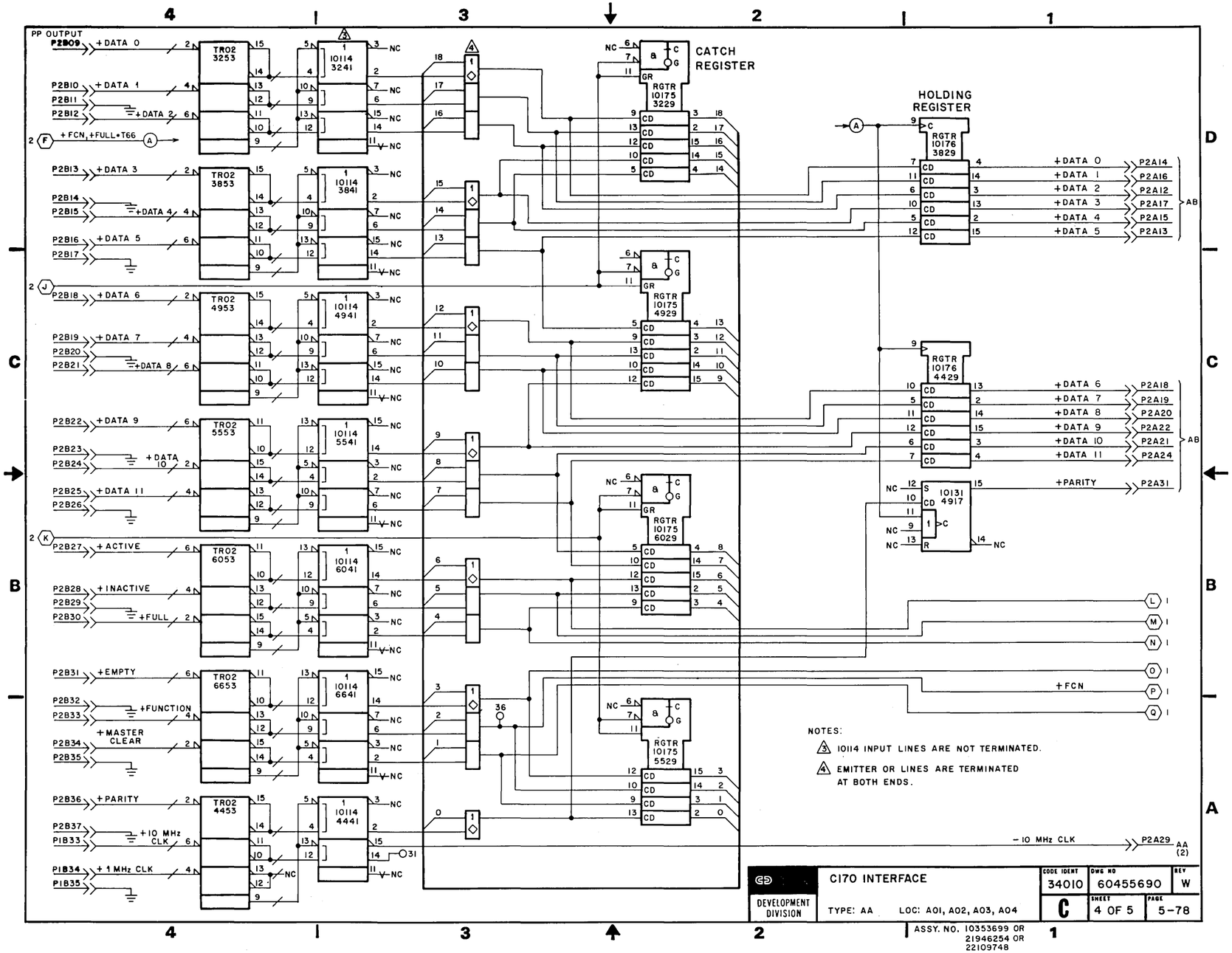
6 LOCATIONS 6605 AND 4405 USED FOR MODULE NUMBER 21946254 ONLY.

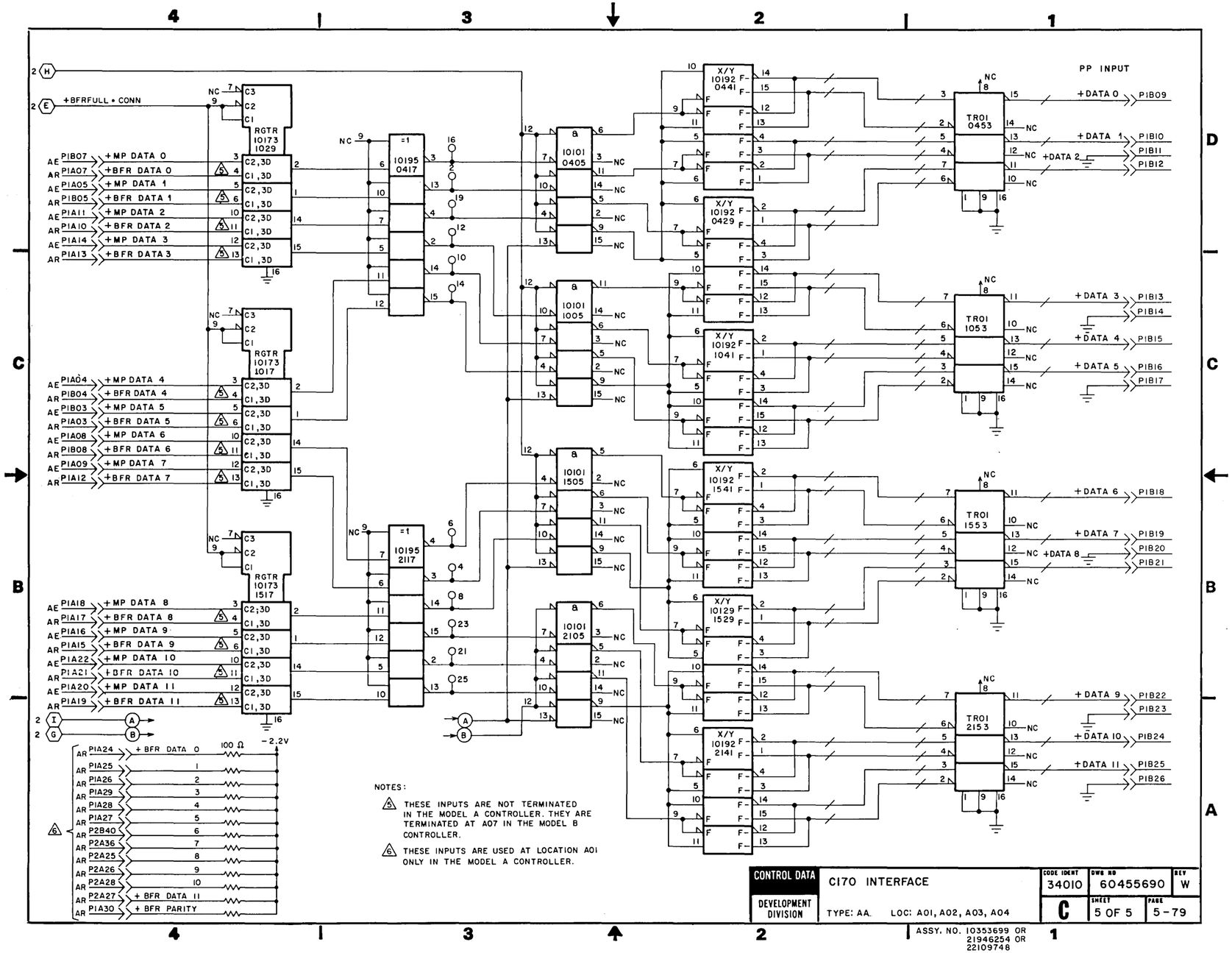
CONTROL DATA	C170 INTERFACE	CODE IDENT 34010	DWG NO 60455690	REV W
DEVELOPMENT DIVISION	TYPE: AA LOC: A01, A02, A03, A04	C	SHEET 1 OF 5	PAGE 5-76.1

ASSY. NO. 10353699 OR 21946254 OR 22109748


INPUT CABLE
AE P1A41 +MP INACTIVE
AE P1B41 +MP FULL
AD (BD) P2A43 +BFR INACTIVE
AD (BD) P2A42 +BFR FULL
AD (BD) P2B43 +BFR EMPTY
AB P2B42 +CONNECT x
AE P2A41 +MP EMPTY
+ACTIVE STAT
AE P1B42 +MP PARITY
AR P1A42 +BFR PARITY
+FCN, +FULL
10104 6005
10102 3217
10104 3817
10101 2617
10105 5505
10105 4905
X/Y F- 10192 2129
X/Y F- 10192 2629
TRO1 2653
TRO1 2641
+ACTIVE PIB27
+INACTIVE PIB28
PIB29
+FULL PIB30
+EMPTY PIB31
PIB32
+PARITY PIB36
PIB37
PULSE GENERATOR
P2B03 10 MHz CLK
100 Ω
40"
-2.2 V
10114 4441
SR-4 10141 4417
C2,4D
CO,4D
C1,4D
RGTR 10176 3805
RGTR 10176 3205
CD
10101 2605
+166 PIA43
+118 PIB43
+CLK 106 PIA40
+CHANNEL CLK 178 (50 ns) PIB40
+CHANNEL CLK 178 (25 ns) PIA38
NOTE:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
2 LOCATION 4905 PIN 11 USED FOR MODULE NUMBER 22109748 ONLY.
CONTROL DATA
DEVELOPMENT DIVISION
C170 INTERFACE
TYPE: AA LOC: A01, A02, A03, A04
ASSY. NO. 22109748
CODE IDENT 34010
DWG NO 60455690
REV W
SIZE C
SHEET 2 OF 5
PAGE 5-76.2


INPUT CABLE
AE P1A41 +MP INACTIVE
AE P1B41 +MP FULL
AD (BD) P2A43 +BFR INACTIVE
AD (BD) P2A42 +BFR FULL
AD (BD) P2B43 +BFR EMPTY
AB P2B42 +CONNECT x
AE P2A41 +MP EMPTY
+ACTIVE STAT
AE P1B42 +MP PARITY
AR P1A42 +BFR PARITY
10104 6005
10104 3817
10102 3217
10101 2617
10105 5505
10105 4905
10101 2605
X/Y 10192 2129
X/Y 10192 2629
TRO1 2653
TRO1 2641
+ACTIVE P1B27
+INACTIVE P1B28
P1B29
+FULL P1B30
+EMPTY P1B31
P1B32
+PARITY P1B36
P1B37
+FCN, +FULL
PULSE GENERATOR
P2B03 10 MHz CLK
10114 4441
SR-4 10141 4417
RGTR 10176 3805
RGTR 10176 3205
10104 3817
+t66 P1A43 NC
+t18 P1B43 NC
+CLK t06 P1A40 AB
+CHANNEL CLK t78 (50 ns) P1B40 AB
+CHANNEL CLK t78 (25 ns) P1A38 AB
100 Ω
40"
-2.2 V
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL DATA
DEVELOPMENT DIVISION
C170 INTERFACE
TYPE: AA LOC: A01, A02, A03, A04
CODE IDENT 34010
DWG NO 60455690
REV W
SHEET 3 OF 5
PAGE 5-77
ASSY. NO. 10353699 OR 21946254


PP OUTPUT
P2B09 +DATA 0
P2B10 +DATA 1
P2B11
P2B12 +DATA 2
+FCN,+FULL•T66
P2B13 +DATA 3
P2B14
P2B15 +DATA 4
P2B16 +DATA 5
P2B17
P2B18 +DATA 6
P2B19 +DATA 7
P2B20
P2B21 +DATA 8
P2B22 +DATA 9
P2B23
P2B24 +DATA 10
P2B25 +DATA 11
P2B26
P2B27 +ACTIVE
P2B28 +INACTIVE
P2B29
P2B30 +FULL
P2B31 +EMPTY
P2B32
P2B33 +FUNCTION
+MASTER CLEAR
P2B34
P2B35
P2B36 +PARITY
P2B37
P1B33 +10 MHz CLK
P1B34 +1 MHz CLK
P1B35
TRO2 3253
TRO2 3853
TRO2 4953
TRO2 5553
TRO2 6053
TRO2 6653
TRO2 4453
10114 3241
10114 3841
10114 4941
10114 5541
10114 6041
10114 6641
10114 4441
CATCH REGISTER
RGTR 10175 3229
RGTR 10175 4929
RGTR 10175 6029
RGTR 10175 5529
HOLDING REGISTER
RGTR 10176 3829
RGTR 10176 4429
10131 4917
+DATA 0 P2A14
+DATA 1 P2A16
+DATA 2 P2A12
+DATA 3 P2A17
+DATA 4 P2A15
+DATA 5 P2A13
+DATA 6 P2A18
+DATA 7 P2A19
+DATA 8 P2A20
+DATA 9 P2A22
+DATA 10 P2A21
+DATA 11 P2A24
+PARITY P2A31
+FCN
-10 MHz CLK P2A29 AA (2)
NOTES:
3 10114 INPUT LINES ARE NOT TERMINATED.
4 EMITTER OR LINES ARE TERMINATED AT BOTH ENDS.
C170 INTERFACE
DEVELOPMENT DIVISION
TYPE: AA LOC: A01, A02, A03, A04
CODE IDENT 34010
DWG NO 60455690
REV W
SIZE C
SHEET 4 OF 5
PAGE 5-78
ASSY. NO. 10353699 OR 21946254 OR 22109748

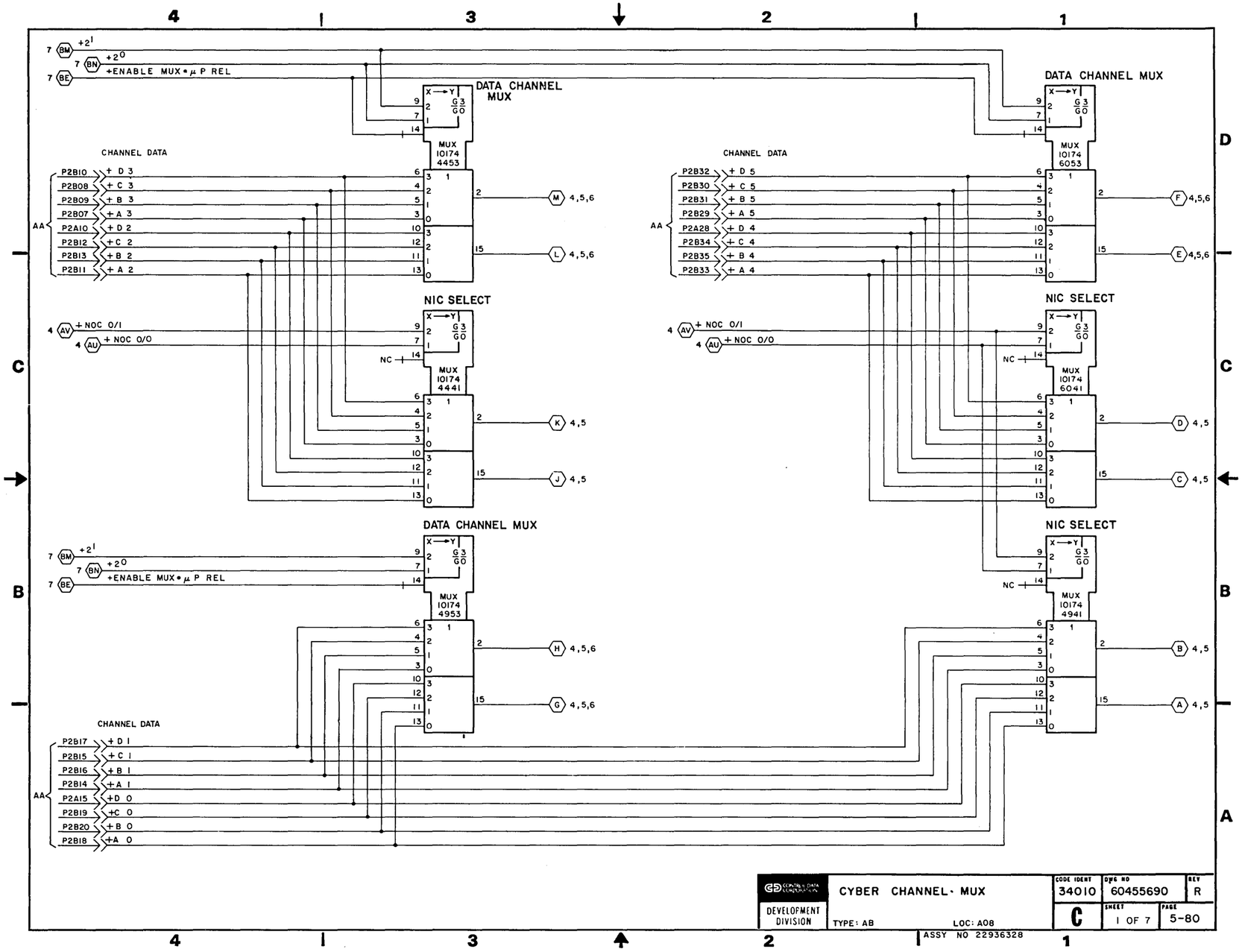


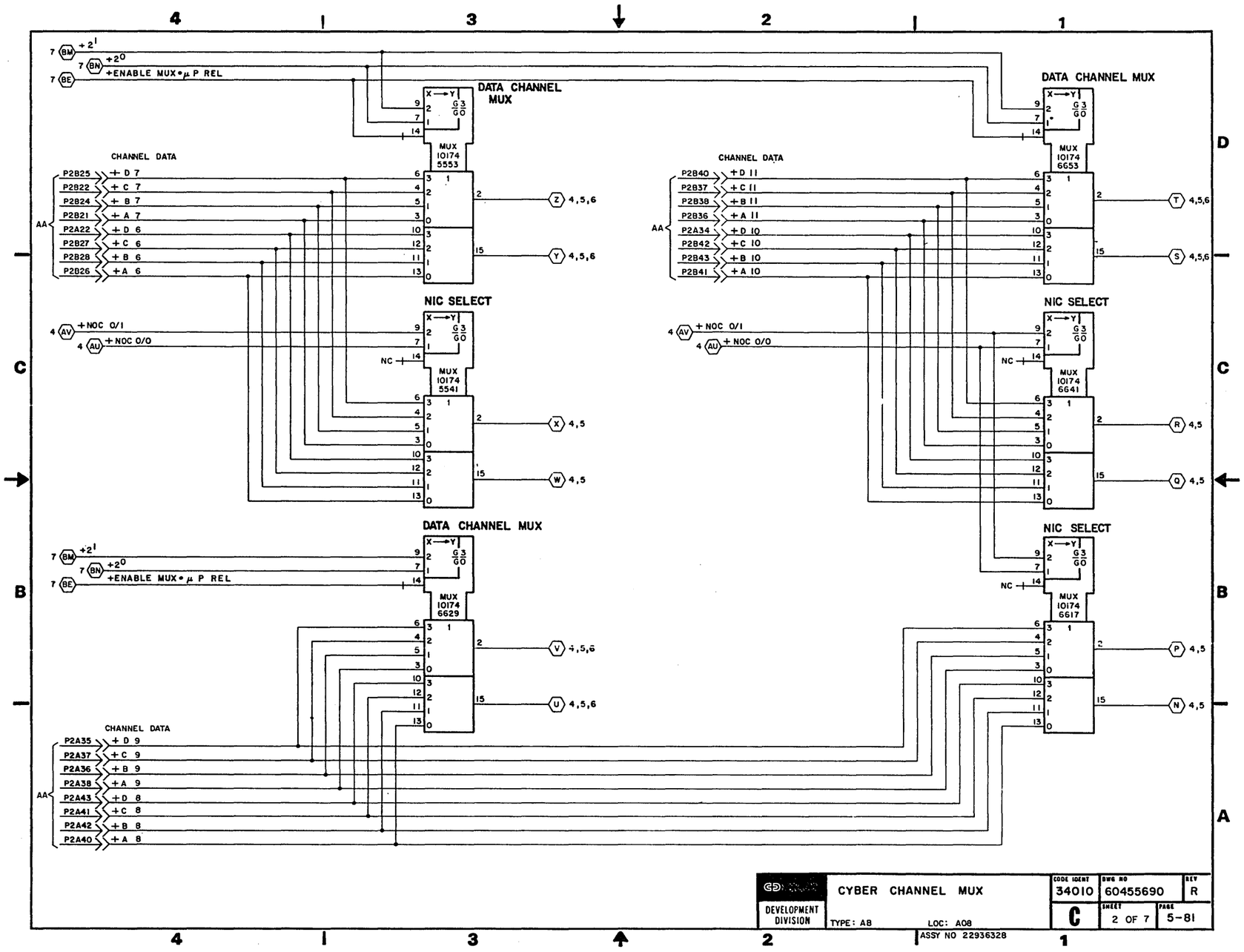
NOTES:

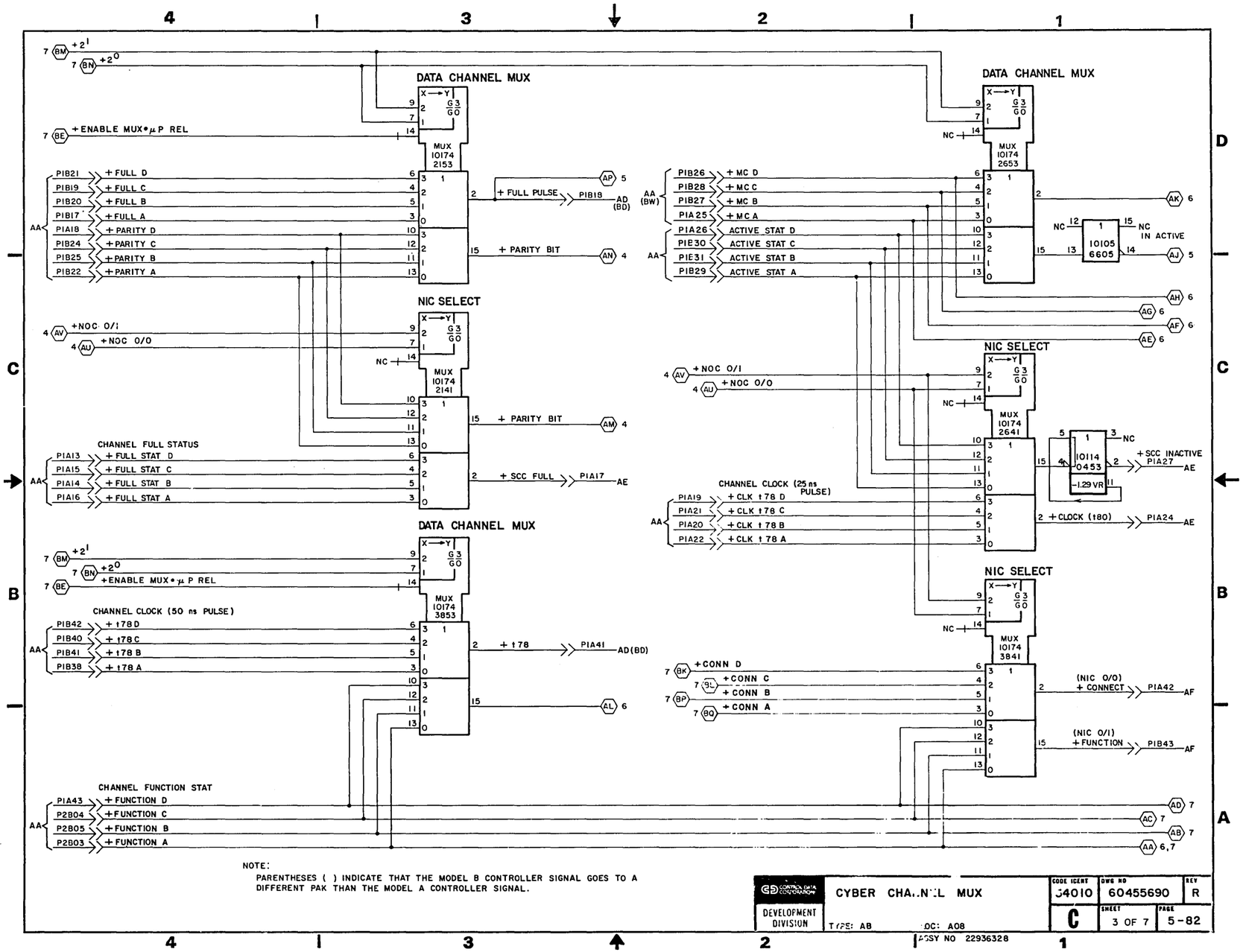
5 THESE INPUTS ARE NOT TERMINATED IN THE MODEL A CONTROLLER. THEY ARE TERMINATED AT A07 IN THE MODEL B CONTROLLER.

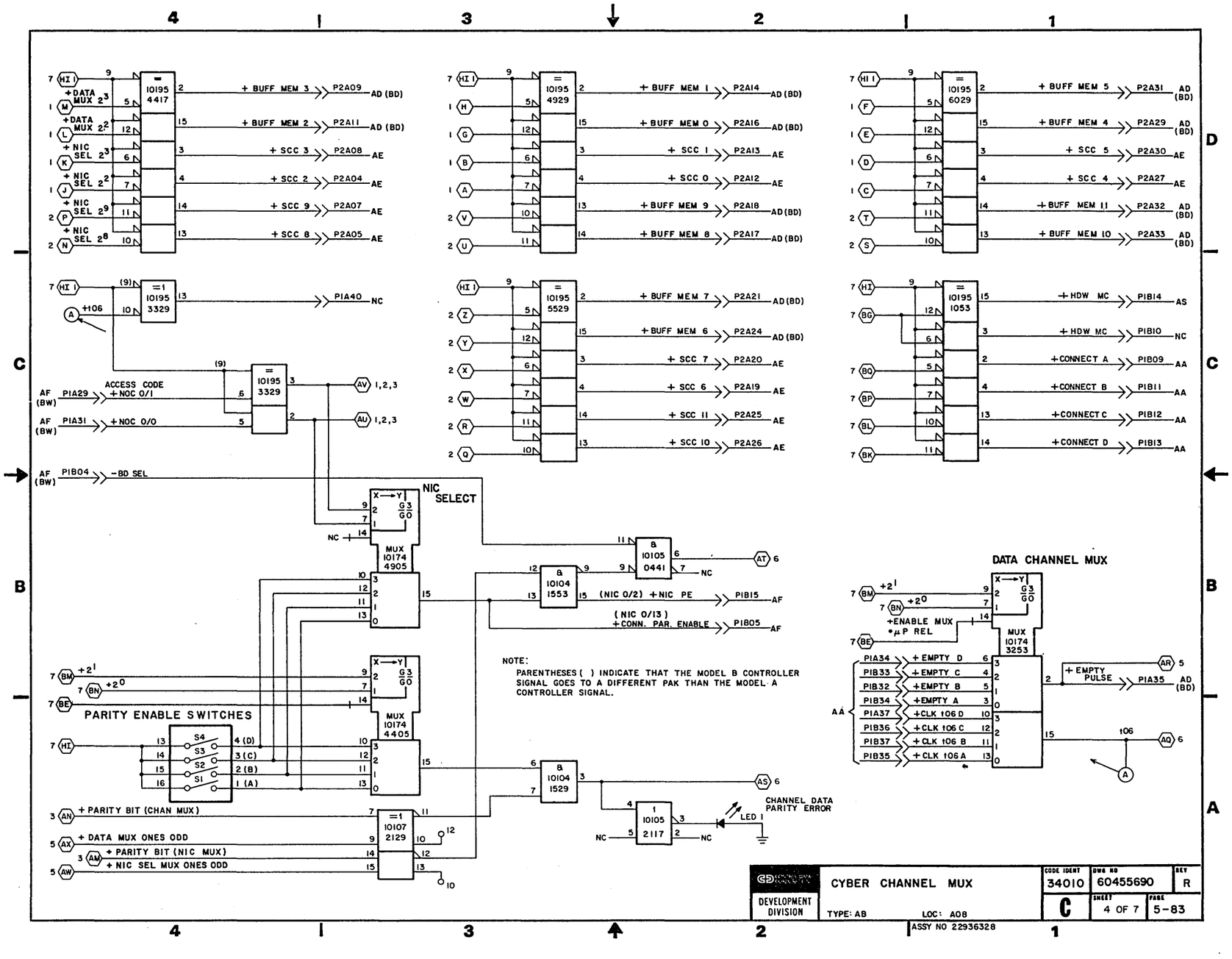
6 THESE INPUTS ARE USED AT LOCATION A01 ONLY IN THE MODEL A CONTROLLER.

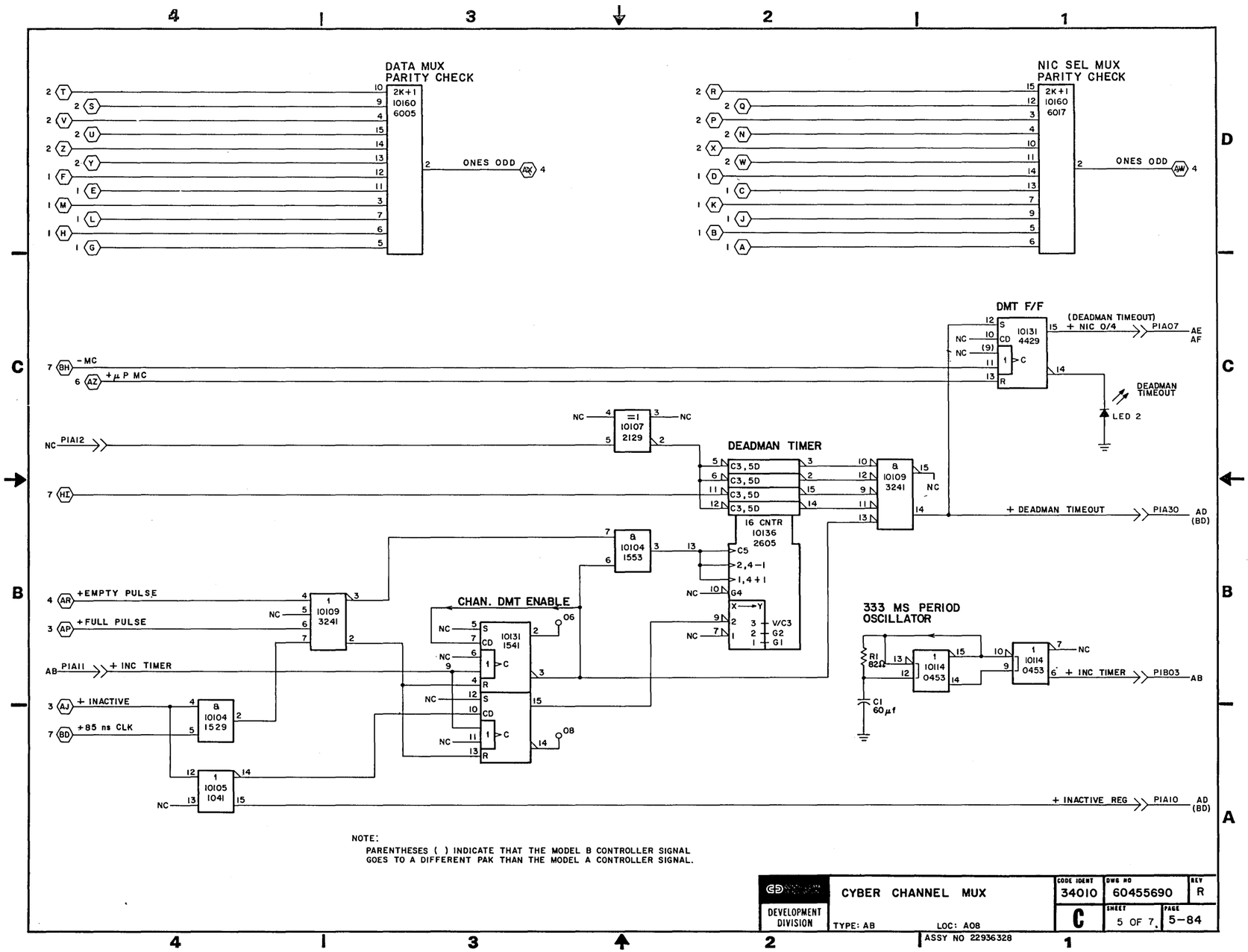
CONTROL DATA	C170 INTERFACE	CODE IDENT 34010	DWG NO 60455690	REV W
DEVELOPMENT DIVISION	TYPE: AA. LOC: A01, A02, A03, A04	C	SHEET 5 OF 5	PAGE 5-79
	ASSY. NO. 10353699 OR 21946254 OR 22109748			


4
3
2
1
DATA CHANNEL MUX
MUX 10174 4453
CHANNEL DATA
P2B10 + D 3
P2B08 + C 3
P2B09 + B 3
P2B07 + A 3
P2A10 + D 2
P2B12 + C 2
P2B13 + B 2
P2B11 + A 2
AA
+2¹
+2⁰
+ENABLE MUX • μP REL
+ NOC 0/1
+ NOC 0/O
NIC SELECT
MUX 10174 4441
DATA CHANNEL MUX
MUX 10174 4953
CHANNEL DATA
P2B17 + D 1
P2B15 + C 1
P2B16 + B 1
P2B14 + A 1
P2A15 + D 0
P2B19 + C 0
P2B20 + B 0
P2B18 + A 0
DATA CHANNEL MUX
MUX 10174 6053
CHANNEL DATA
P2B32 + D 5
P2B30 + C 5
P2B31 + B 5
P2B29 + A 5
P2A28 + D 4
P2B34 + C 4
P2B35 + B 4
P2B33 + A 4
NIC SELECT
MUX 10174 6041
NIC SELECT
MUX 10174 4941
M 4,5,6
L 4,5,6
K 4,5
J 4,5
H 4,5,6
G 4,5,6
F 4,5,6
E 4,5,6
D 4,5
C 4,5
B 4,5
A 4,5
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CYBER CHANNEL- MUX
TYPE: AB
LOC: A08
ASSY NO 22936328
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 7
PAGE 5-80


DATA CHANNEL MUX
MUX 10174 5553
CHANNEL DATA
P2B25 + D 7
P2B22 + C 7
P2B24 + B 7
P2B21 + A 7
P2A22 + D 6
P2B27 + C 6
P2B28 + B 6
P2B26 + A 6
AA
7 BM +2 1
7 BN +2 0
7 BE +ENABLE MUX • μ P REL
Z 4,5,6
Y 4,5,6
NIC SELECT
MUX 10174 5541
4 AV +NOC 0/1
4 AU +NOC 0/0
NC
X 4,5
W 4,5
DATA CHANNEL MUX
MUX 10174 6653
CHANNEL DATA
P2B40 + D 11
P2B37 + C 11
P2B38 + B 11
P2B36 + A 11
P2A34 + D 10
P2B42 + C 10
P2B43 + B 10
P2B41 + A 10
T 4,5,6
S 4,5,6
NIC SELECT
MUX 10174 6641
R 4,5
Q 4,5
DATA CHANNEL MUX
MUX 10174 6629
V 4,5,6
U 4,5,6
NIC SELECT
MUX 10174 6617
P 4,5
N 4,5
CHANNEL DATA
P2A35 + D 9
P2A37 + C 9
P2A36 + B 9
P2A38 + A 9
P2A43 + D 8
P2A41 + C 8
P2A42 + B 8
P2A40 + A 8
CYBER CHANNEL MUX
DEVELOPMENT DIVISION
TYPE: A8
LOC: A08
ASSY NO 22936328
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 2 OF 7
PAGE 5-81

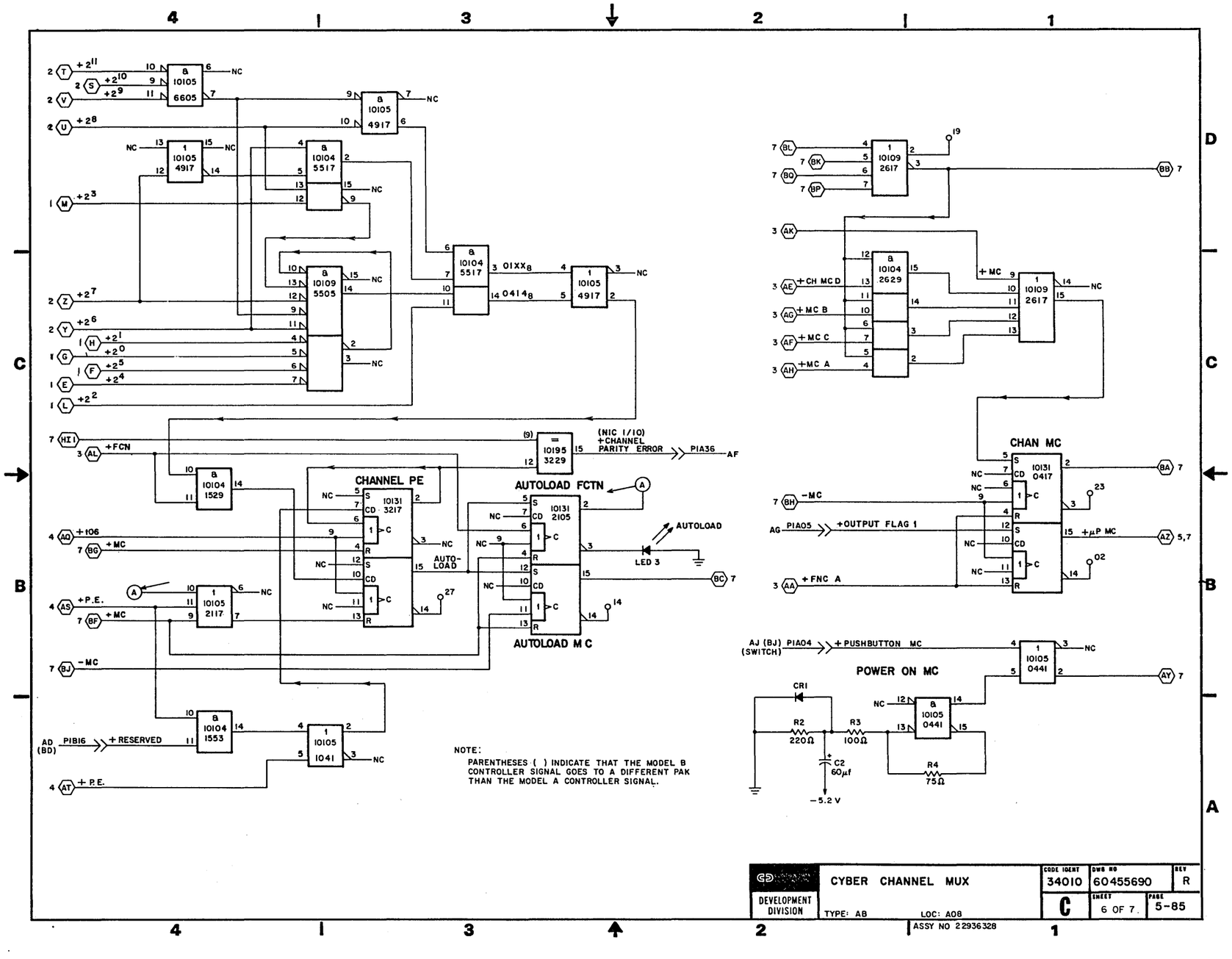

DATA CHANNEL MUX
MUX 10174 2153
+ENABLE MUX•μP REL
+FULL D
+FULL C
+FULL B
+FULL A
+PARITY D
+PARITY C
+PARITY B
+PARITY A
+FULL PULSE
+PARITY BIT
NIC SELECT
MUX 10174 2141
+NOC 0/1
+NOC 0/0
CHANNEL FULL STATUS
+FULL STAT D
+FULL STAT C
+FULL STAT B
+FULL STAT A
+SCC FULL
DATA CHANNEL MUX
MUX 10174 3853
CHANNEL CLOCK (50 ns PULSE)
+t78 D
+t78 C
+t78 B
+t78 A
+t78
CHANNEL FUNCTION STAT
+FUNCTION D
+FUNCTION C
+FUNCTION B
+FUNCTION A
DATA CHANNEL MUX
MUX 10174 2653
+MC D
+MC C
+MC B
+MC A
ACTIVE STAT D
ACTIVE STAT C
ACTIVE STAT B
ACTIVE STAT A
10105 6605
NC IN ACTIVE
NIC SELECT
MUX 10174 2641
CHANNEL CLOCK (25 ns PULSE)
+CLK t78 D
+CLK t78 C
+CLK t78 B
+CLK t78 A
10114 0453
-1.29 VR
+SCC INACTIVE PIA27
+CLOCK (180) PIA24
NIC SELECT
MUX 10174 3841
+CONN D
+CONN C
+CONN B
+CONN A
(NIC 0/0) + CONNECT PIA42
(NIC 0/1) + FUNCTION PIB43
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
CYBER CHANNEL MUX
TYPE: AB
DOC: A08
ASSY NO 22936328
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 7
PAGE 5-82

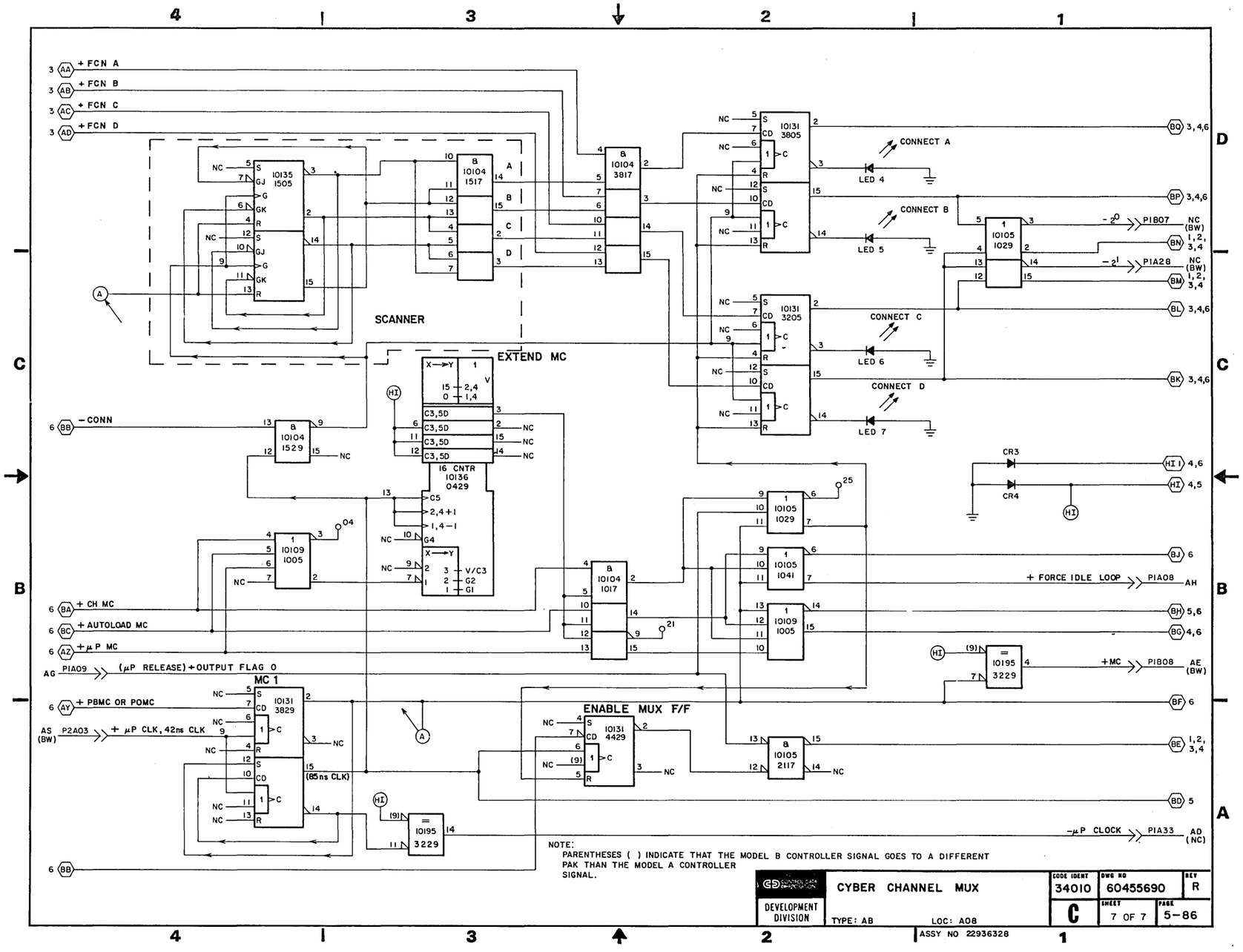

4
3
2
1
D
C
B
A
10195 4417
+ BUFF MEM 3 P2A09 AD (BD)
+ BUFF MEM 2 P2A11 AD (BD)
+ SCC 3 P2A08 AE
+ SCC 2 P2A04 AE
+ SCC 9 P2A07 AE
+ SCC 8 P2A05 AE
+DATA MUX 2^3
+DATA MUX 2^2
+NIC SEL 2^3
+NIC SEL 2^2
+NIC SEL 2^9
+NIC SEL 2^8
10195 4929
+ BUFF MEM 1 P2A14 AD (BD)
+ BUFF MEM 0 P2A16 AD (BD)
+ SCC 1 P2A13 AE
+ SCC 0 P2A12 AE
+ BUFF MEM 9 P2A18 AD (BD)
+ BUFF MEM 8 P2A17 AD (BD)
10195 6029
+ BUFF MEM 5 P2A31 AD (BD)
+ BUFF MEM 4 P2A29 AD (BD)
+ SCC 5 P2A30 AE
+ SCC 4 P2A27 AE
+ BUFF MEM 11 P2A32 AD (BD)
+ BUFF MEM 10 P2A33 AD (BD)
10195 3329
+106
P1A40 NC
ACCESS CODE
AF (BW) P1A29 +NOC 0/1
AF (BW) P1A31 +NOC 0/0
AV 1,2,3
AU 1,2,3
10195 5529
+ BUFF MEM 7 P2A21 AD (BD)
+ BUFF MEM 6 P2A24 AD (BD)
+ SCC 7 P2A20 AE
+ SCC 6 P2A19 AE
+ SCC 11 P2A25 AE
+ SCC 10 P2A26 AE
10195 1053
+HDW MC P1B14 AS
+HDW MC P1B10 NC
+CONNECT A P1B09 AA
+CONNECT B P1B11 AA
+CONNECT C P1B12 AA
+CONNECT D P1B13 AA
AF (BW) P1B04 -BD SEL
NIC SELECT
MUX 10174 4905
10105 0441
AT 6
10104 1553
(NIC 0/2) +NIC PE P1B15 AF
(NIC 0/13) +CONN. PAR. ENABLE P1B05 AF
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
PARITY ENABLE SWITCHES
S4
S3
S2
S1
4 (D)
3 (C)
2 (B)
1 (A)
MUX 10174 4405
10104 1529
AS 6
+ PARITY BIT (CHAN MUX)
+ DATA MUX ONES ODD
+ PARITY BIT (NIC MUX)
+ NIC SEL MUX ONES ODD
10107 2129
10105 2117
LED 1
CHANNEL DATA PARITY ERROR
DATA CHANNEL MUX
+2^1
+2^0
+ENABLE MUX •μP REL
MUX 10174 3253
PIA34 + EMPTY D
PIB33 + EMPTY C
PIB32 + EMPTY B
PIB34 + EMPTY A
PIA37 +CLK 106 D
PIB36 +CLK 106 C
PIB37 + CLK 106 B
PIB35 + CLK 106 A
+ EMPTY PULSE PIA35 AD (BD)
AR 5
AQ 6
106
CYBER CHANNEL MUX
TYPE: AB
LOC: A08
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 4 OF 7
PAGE 5-83
ASSY NO 22936328

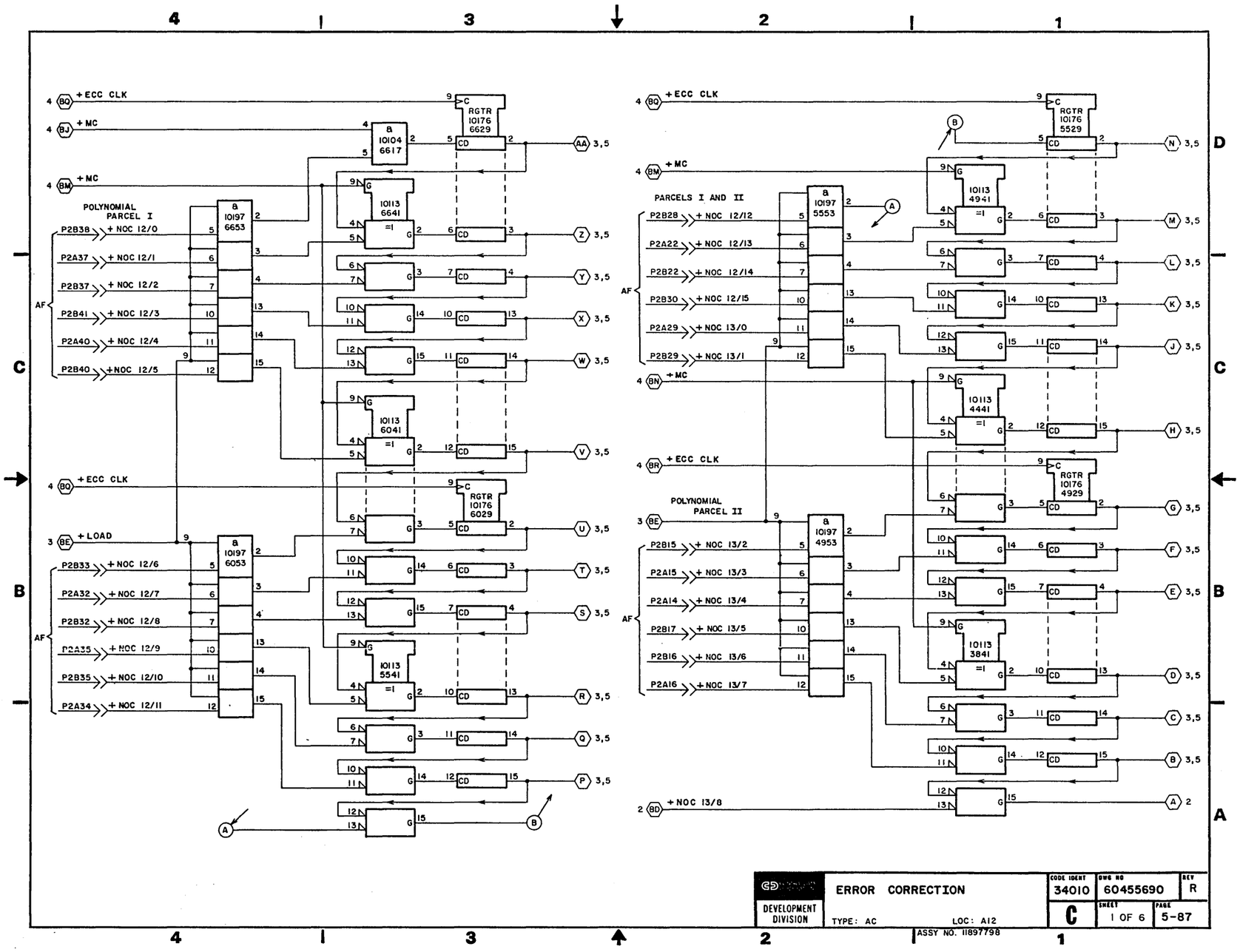


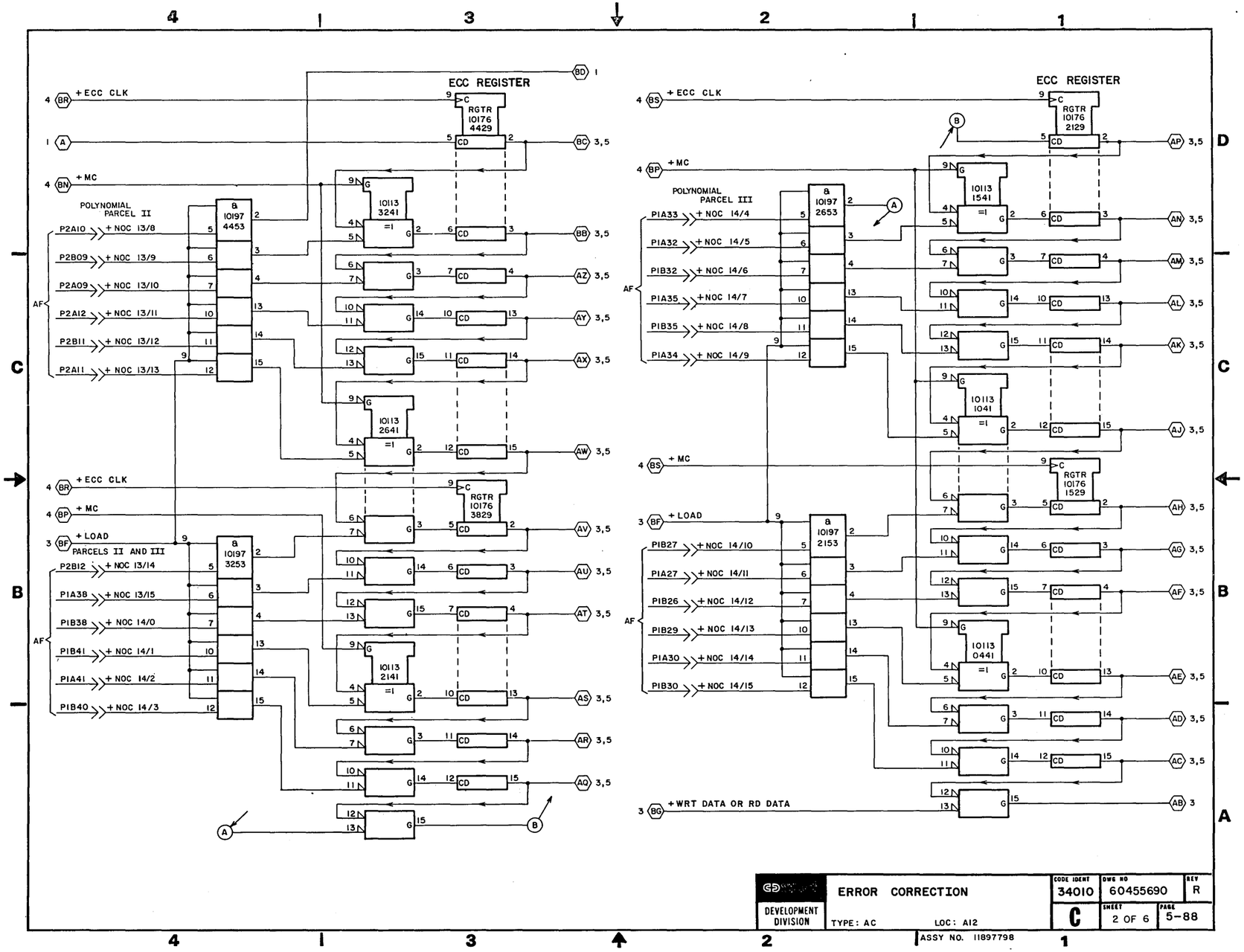
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

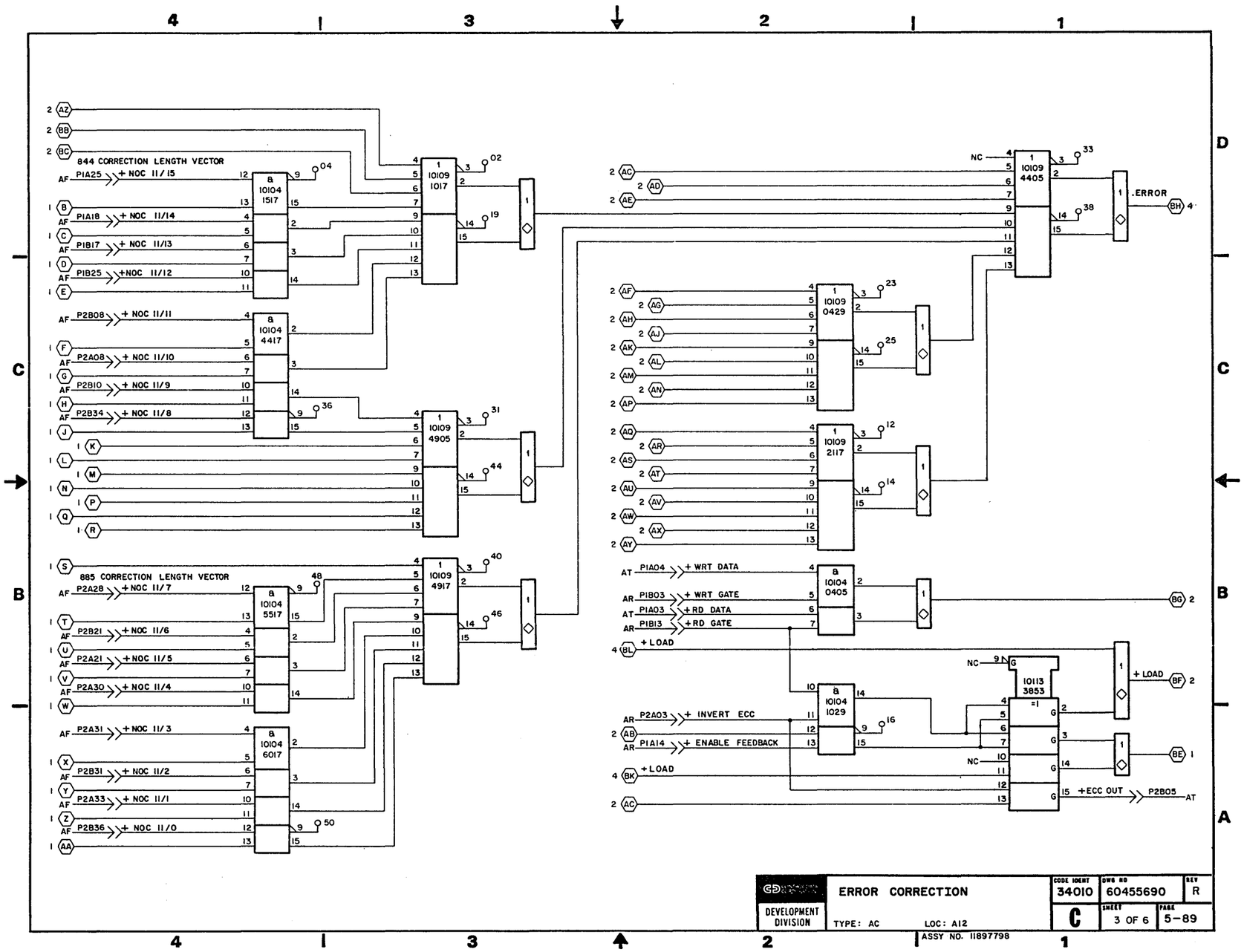
CONTROL DATA	CYBER CHANNEL MUX	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AB LOC: A08 ASSY NO 22936328	C	SHEET 5 OF 7	PAGE 5-84

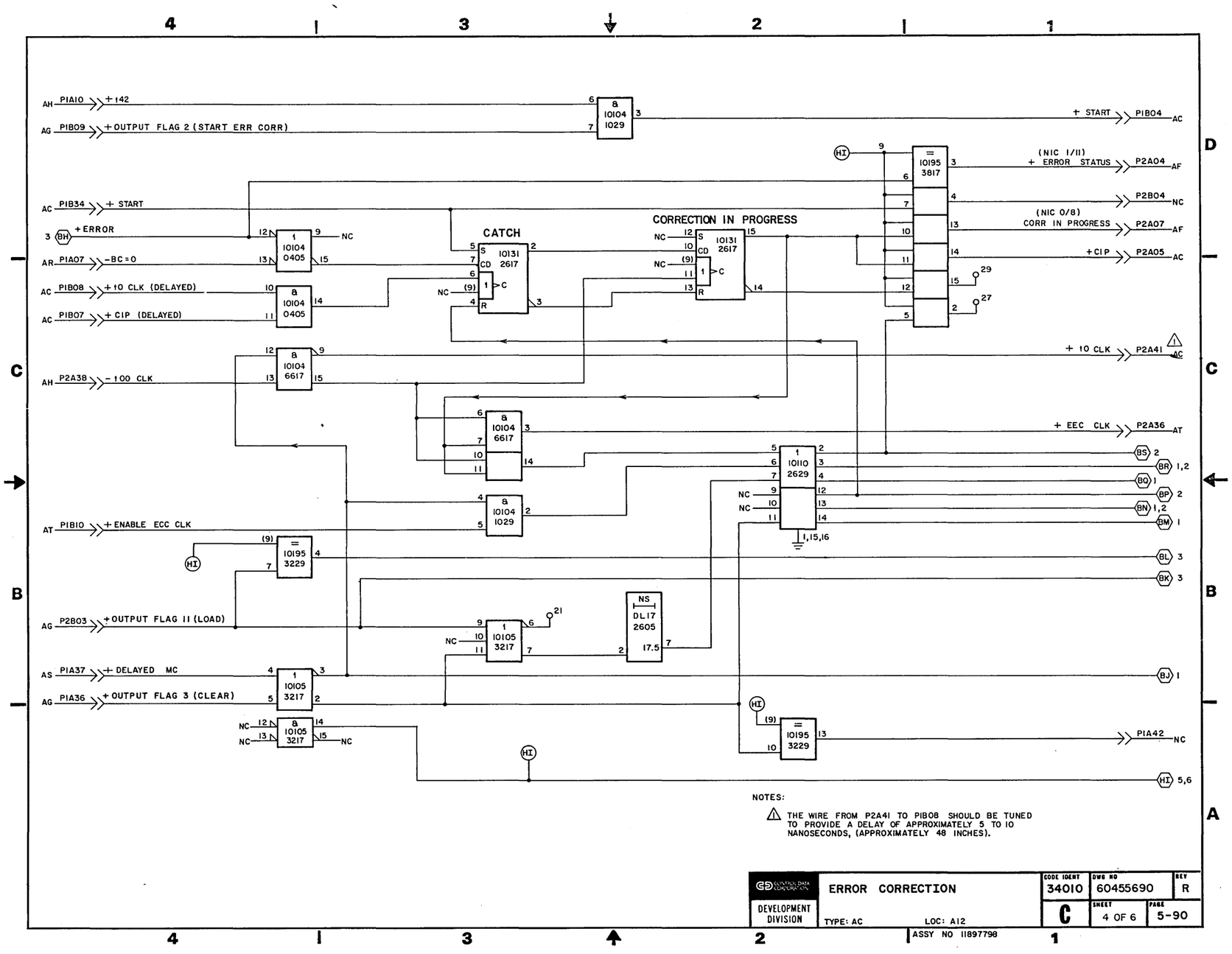

4
3
2
1
B
10105 6605
10105 4917
10105 4917
10104 5517
10104 5517
10109 5505
10105 4917
10195 3229
(NIC 1/10) +CHANNEL PARITY ERROR
PIA36
AF
CHANNEL PE
10131 3217
AUTOLOAD FCTN
10131 2105
AUTOLOAD
LED 3
AUTO-LOAD
AUTOLOAD M C
10104 1529
10105 2117
10104 1553
10105 1041
+FCN
+106
+MC
+P.E.
-MC
+RESERVED
PIB16
+ P.E.
10109 2617
10104 2629
10109 2617
+CH MC D
+MC B
+MC C
+MC A
CHAN MC
10131 0417
-MC
+OUTPUT FLAG 1
+FNC A
+µP MC
AJ (BJ) PIA04 (SWITCH)
+PUSHBUTTON MC
POWER ON MC
10105 0441
10105 0441
CR1
R2 220Ω
R3 100Ω
R4 75Ω
C2 60µf
-5.2 V
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CYBER CHANNEL MUX
DEVELOPMENT DIVISION
TYPE: AB
LOC: A08
ASSY NO 22936328
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 6 OF 7
PAGE 5-85

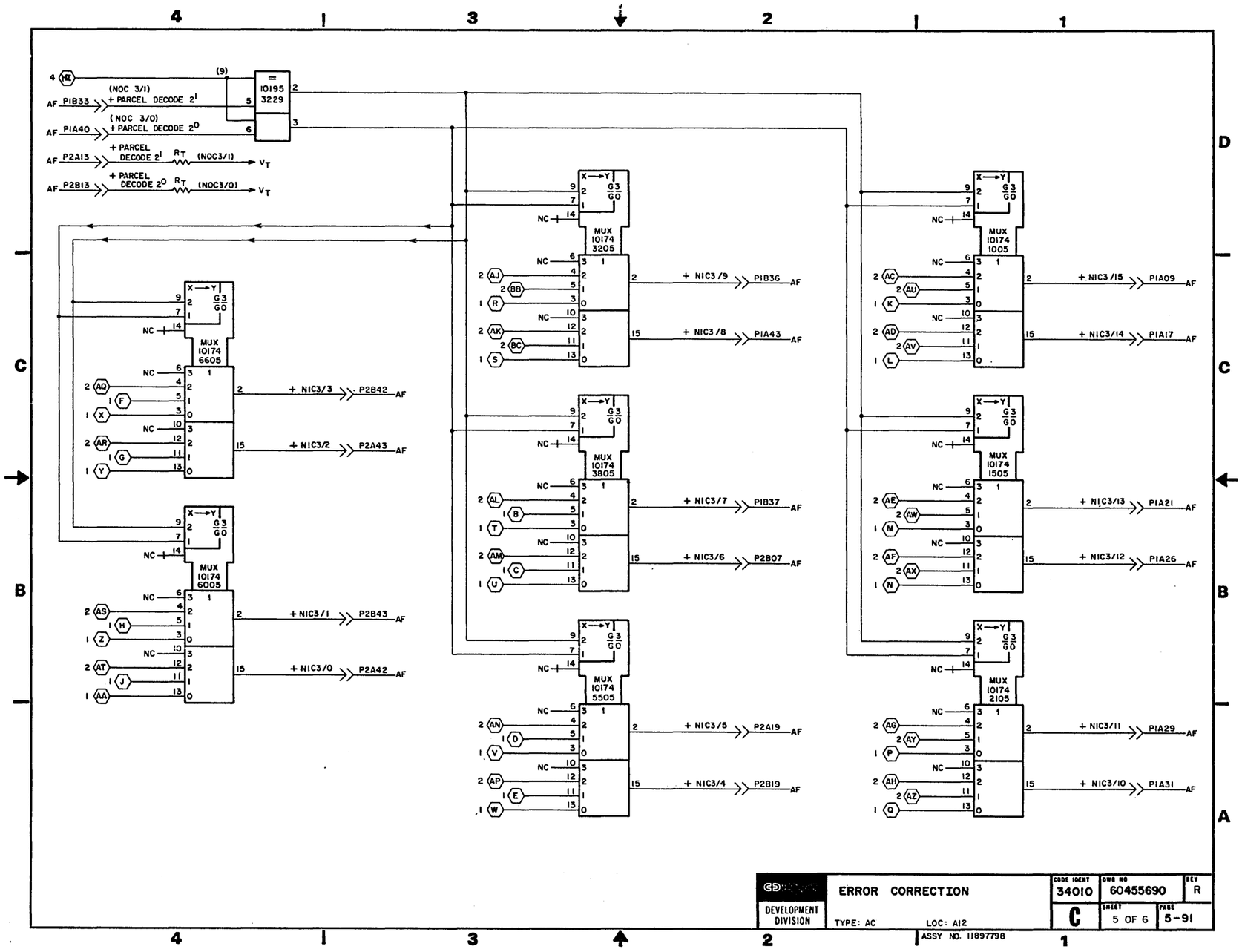

+ FCN A
+ FCN B
+ FCN C
+ FCN D
SCANNER
EXTEND MC
CONNECT A
CONNECT B
CONNECT C
CONNECT D
LED 4
LED 5
LED 6
LED 7
- CONN
+ CH MC
+ AUTOLOAD MC
+ μP MC
(μP RELEASE) + OUTPUT FLAG 0
+ PBMC OR POMC
+ μP CLK, 42ns CLK
MC 1
ENABLE MUX F/F
16 CNTR 10136 0429
+ FORCE IDLE LOOP
+MC
-μP CLOCK
CR3
CR4
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CYBER CHANNEL MUX
TYPE: AB
LOC: A08
ASSY NO 22936328
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 7 OF 7
PAGE 5-86
DEVELOPMENT DIVISION

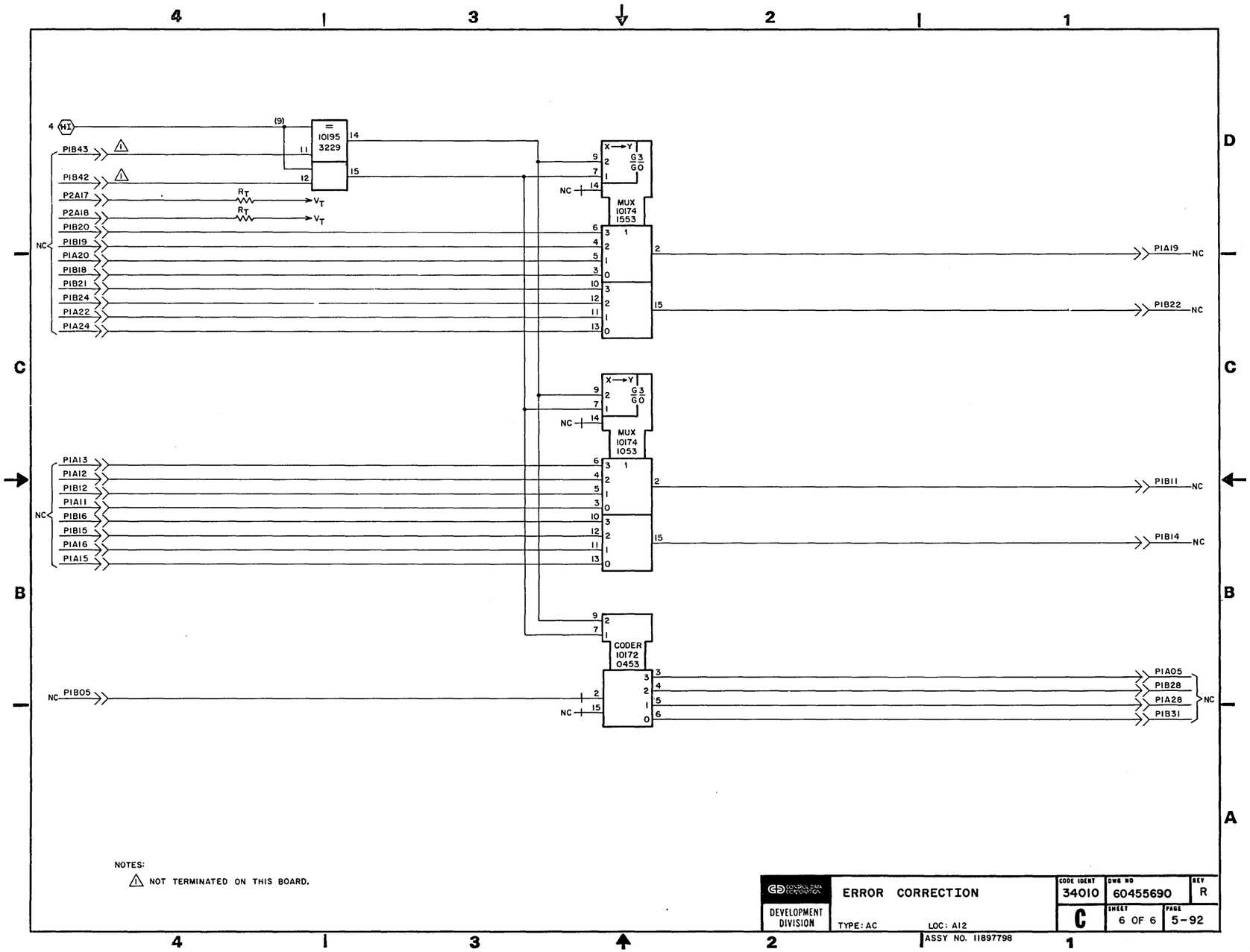

+ECC CLK
+MC
+MC
POLYNOMIAL PARCEL I
P2B38 +NOC 12/0
P2A37 +NOC 12/1
P2B37 +NOC 12/2
P2B41 +NOC 12/3
P2A40 +NOC 12/4
P2B40 +NOC 12/5
AF
8 10197 6653
8 10104 6617
10113 6641
=1
RGTR 10176 6629
CD
AA 3,5
Z 3,5
Y 3,5
X 3,5
W 3,5
10113 6041
=1
V 3,5
+ECC CLK
RGTR 10176 6029
U 3,5
+LOAD
P2B33 +NOC 12/6
P2A32 +NOC 12/7
P2B32 +NOC 12/8
P2A35 +NOC 12/9
P2B35 +NOC 12/10
P2A34 +NOC 12/11
8 10197 6053
T 3,5
S 3,5
10113 5541
=1
R 3,5
Q 3,5
P 3,5
A
B
+ECC CLK
+MC
PARCELS I AND II
P2B28 +NOC 12/12
P2A22 +NOC 12/13
P2B22 +NOC 12/14
P2B30 +NOC 12/15
P2A29 +NOC 13/0
P2B29 +NOC 13/1
+MC
8 10197 5553
RGTR 10176 5529
N 3,5
10113 4941
=1
M 3,5
L 3,5
K 3,5
J 3,5
10113 4441
=1
H 3,5
+ECC CLK
POLYNOMIAL PARCEL II
P2B15 +NOC 13/2
P2A15 +NOC 13/3
P2A14 +NOC 13/4
P2B17 +NOC 13/5
P2B16 +NOC 13/6
P2A16 +NOC 13/7
8 10197 4953
RGTR 10176 4929
G 3,5
F 3,5
E 3,5
10113 3841
=1
D 3,5
C 3,5
B 3,5
+NOC 13/8
A 2
4
1
3
2
1
D
C
B
A
DEVELOPMENT DIVISION
ERROR CORRECTION
TYPE: AC
LOC: A12
ASSY NO. 11897798
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 1 OF 6
PAGE 5-87


ECC REGISTER
+ECC CLK
+MC
+LOAD
PARCELS II AND III
POLYNOMIAL PARCEL II
POLYNOMIAL PARCEL III
RGTR 10176 4429
RGTR 10176 3829
RGTR 10176 2129
RGTR 10176 1529
8 10197 4453
8 10197 3253
8 10197 2653
8 10197 2153
10113 3241
10113 2641
10113 2141
10113 1541
10113 1041
10113 0441
=1
P2A10 +NOC 13/8
P2B09 +NOC 13/9
P2A09 +NOC 13/10
P2A12 +NOC 13/11
P2B11 +NOC 13/12
P2A11 +NOC 13/13
P2B12 +NOC 13/14
P1A38 +NOC 13/15
P1B38 +NOC 14/0
P1B41 +NOC 14/1
P1A41 +NOC 14/2
P1B40 +NOC 14/3
P1A33 +NOC 14/4
P1A32 +NOC 14/5
P1B32 +NOC 14/6
P1A35 +NOC 14/7
P1B35 +NOC 14/8
P1A34 +NOC 14/9
P1B27 +NOC 14/10
P1A27 +NOC 14/11
P1B26 +NOC 14/12
P1B29 +NOC 14/13
P1A30 +NOC 14/14
P1B30 +NOC 14/15
+WRT DATA OR RD DATA
BC 3,5
BB 3,5
AZ 3,5
AY 3,5
AX 3,5
AW 3,5
AV 3,5
AU 3,5
AT 3,5
AS 3,5
AR 3,5
AQ 3,5
AP 3,5
AN 3,5
AM 3,5
AL 3,5
AK 3,5
AJ 3,5
AH 3,5
AG 3,5
AF 3,5
AE 3,5
AD 3,5
AC 3,5
AB 3
DEVELOPMENT DIVISION
ERROR CORRECTION
TYPE: AC
LOC: A12
ASSY NO. 11897798
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 2 OF 6
PAGE 5-88


844 CORRECTION LENGTH VECTOR
885 CORRECTION LENGTH VECTOR
+ NOC 11/15
+ NOC 11/14
+ NOC 11/13
+NOC 11/12
+ NOC 11/11
+ NOC 11/10
+ NOC 11/9
+ NOC 11/8
+ NOC 11/7
+ NOC 11/6
+ NOC 11/5
+ NOC 11/4
+ NOC 11/3
+ NOC 11/2
+ NOC 11/1
+ NOC 11/0
+ WRT DATA
+ WRT GATE
+RD DATA
+RD GATE
+ LOAD
+ INVERT ECC
+ ENABLE FEEDBACK
+ECC OUT
.ERROR
NC
P2B05
ERROR CORRECTION
TYPE: AC
LOC: A12
ASSY NO. 11897798
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 6
PAGE 5-89
DEVELOPMENT DIVISION


AH PIA10 + 142
AG PIB09 + OUTPUT FLAG 2 (START ERR CORR)
8 10104 1029
+ START P1B04 AC
HI
= 10195 3817
(NIC 1/11) + ERROR STATUS P2A04 AF
P2B04 NC
(NIC 0/8) CORR IN PROGRESS P2A07 AF
+ CIP P2A05 AC
29
27
AC PIB34 + START
3 BH + ERROR
AR PIA07 - BC = 0
AC PIB08 + 10 CLK (DELAYED)
AC PIB07 + CIP (DELAYED)
1 10104 0405
8 10104 0405
NC
CATCH
S 10131 2617 CD
1 C
R
CORRECTION IN PROGRESS
NC
(9)
+ 10 CLK P2A41 AC
AH P2A38 - 100 CLK
8 10104 6617
+ EEC CLK P2A36 AT
8 10104 1029
1 10110 2629
BS 2
BR 1,2
BQ 1
BP 2
BN 1,2
BM 1
1,15,16
AT PIB10 + ENABLE ECC CLK
= 10195 3229
BL 3
BK 3
NS DL17 2605 17.5
AG P2B03 + OUTPUT FLAG 11 (LOAD)
1 10105 3217
21
AS PIA37 + DELAYED MC
AG PIA36 + OUTPUT FLAG 3 (CLEAR)
BJ 1
8 10105 3217
PIA42 NC
HI 5,6
NOTES:
1. THE WIRE FROM P2A41 TO PIB08 SHOULD BE TUNED TO PROVIDE A DELAY OF APPROXIMATELY 5 TO 10 NANOSECONDS, (APPROXIMATELY 48 INCHES).
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
ERROR CORRECTION
TYPE: AC
LOC: A12
ASSY NO 11897798
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 4 OF 6
PAGE 5-90

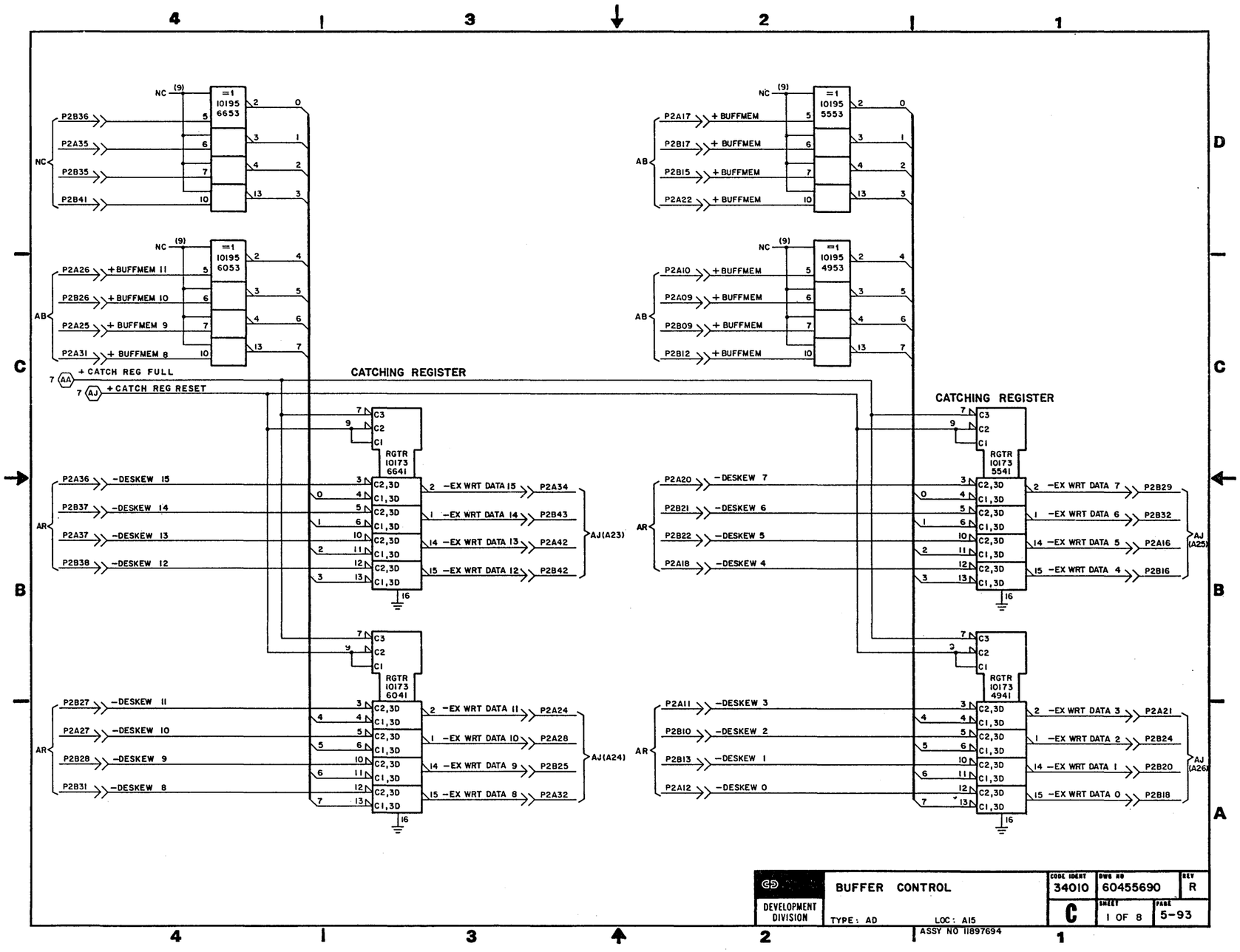

4
3
2
1
D
C
B
A
(9)
=
10195
3229
(NOC 3/1)
+ PARCEL DECODE 2^1
(NOC 3/0)
+ PARCEL DECODE 2^0
AF P1B33
AF P1A40
AF P2A13
AF P2B13
+ PARCEL DECODE 2^1 RT (NOC3/1) VT
+ PARCEL DECODE 2^0 RT (NOC3/0) VT
MUX 10174 6605
MUX 10174 6005
MUX 10174 3205
MUX 10174 3805
MUX 10174 5505
MUX 10174 1005
MUX 10174 1505
MUX 10174 2105
+ NIC3/3 P2B42 AF
+ NIC3/2 P2A43 AF
+ NIC3/1 P2B43 AF
+ NIC3/0 P2A42 AF
+ NIC3/9 P1B36 AF
+ NIC3/8 P1A43 AF
+ NIC3/7 P1B37 AF
+ NIC3/6 P2B07 AF
+ NIC3/5 P2A19 AF
+ NIC3/4 P2B19 AF
+ NIC3/15 P1A09 AF
+ NIC3/14 P1A17 AF
+ NIC3/13 P1A21 AF
+ NIC3/12 P1A26 AF
+ NIC3/11 P1A29 AF
+ NIC3/10 P1A31 AF
ERROR CORRECTION
DEVELOPMENT DIVISION
TYPE: AC
LOC: A12
ASSY NO. 11897798
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 5 OF 6
PAGE 5-91

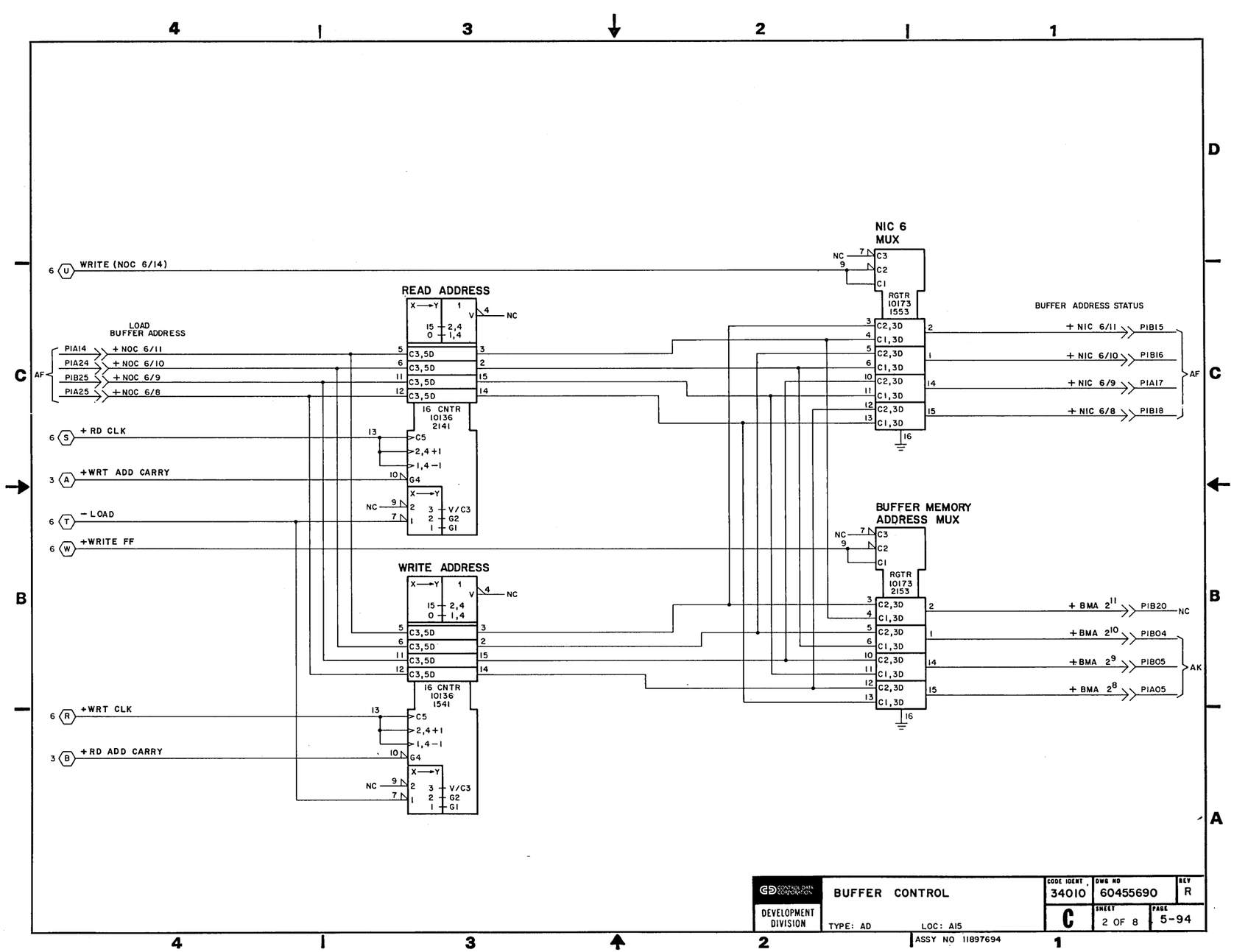


NOTES:

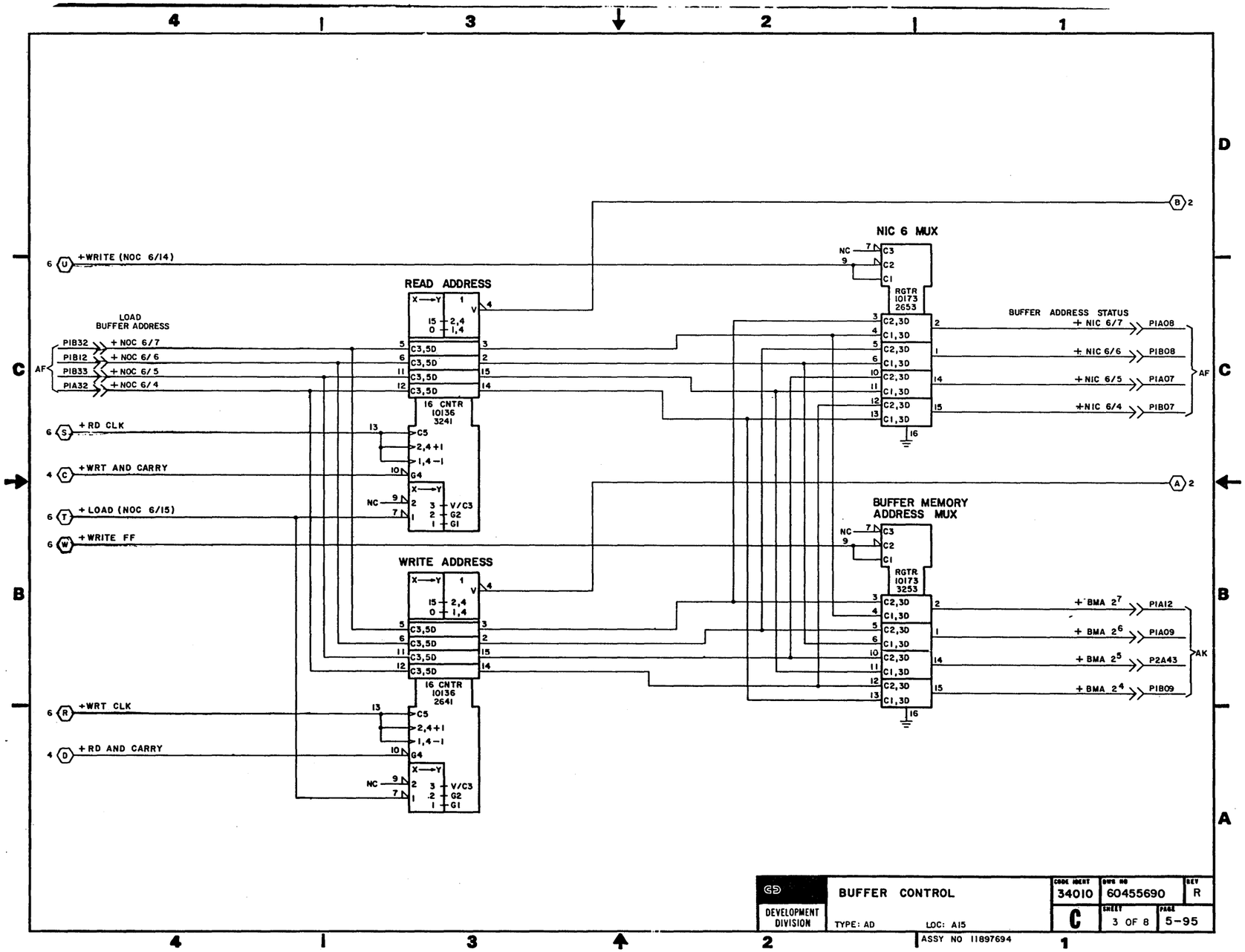
⚠ NOT TERMINATED ON THIS BOARD.

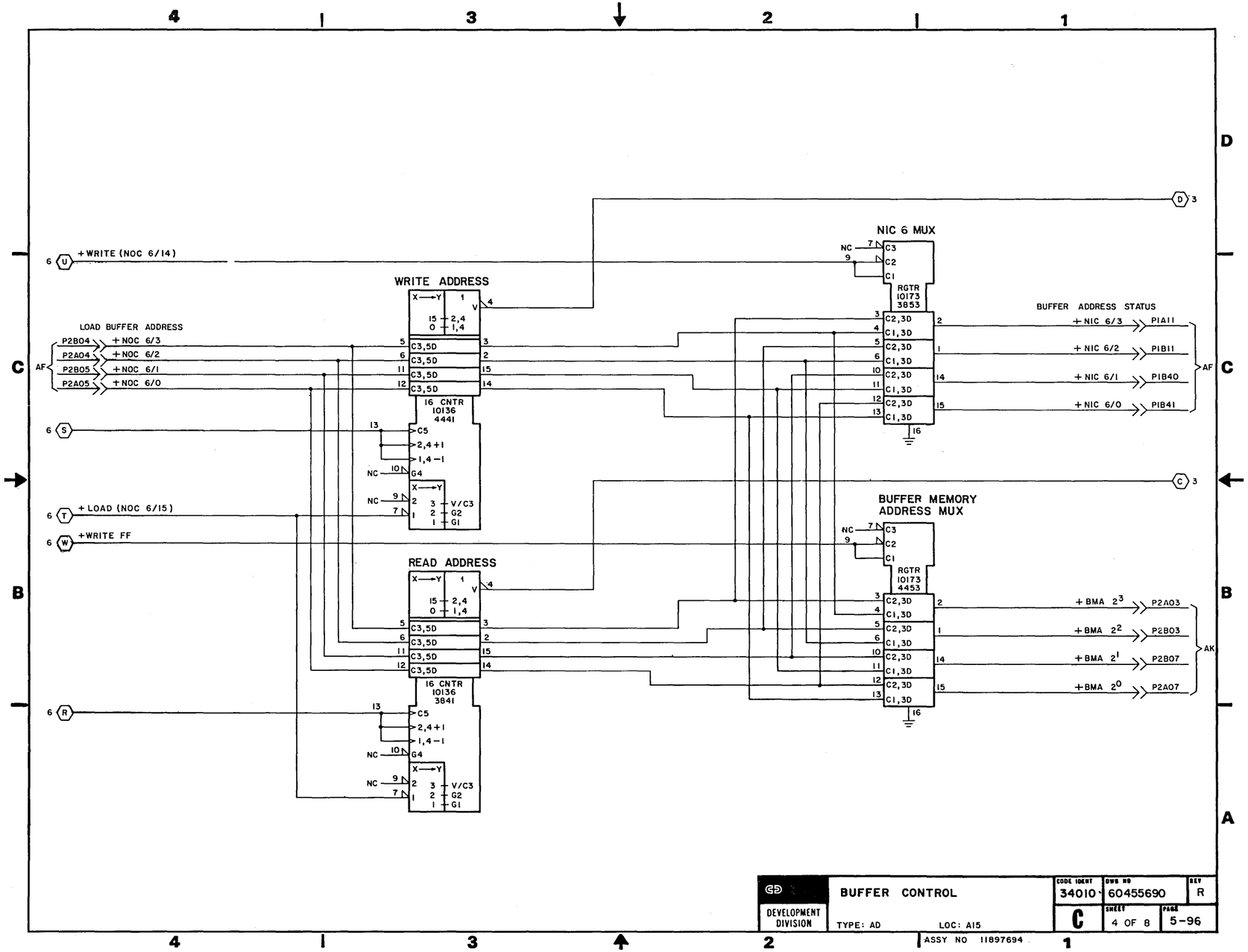
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	ERROR CORRECTION	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AC LOC: AI2 ASSY NO. 11897798		C	SHEET 6 OF 6	PAGE 5-92

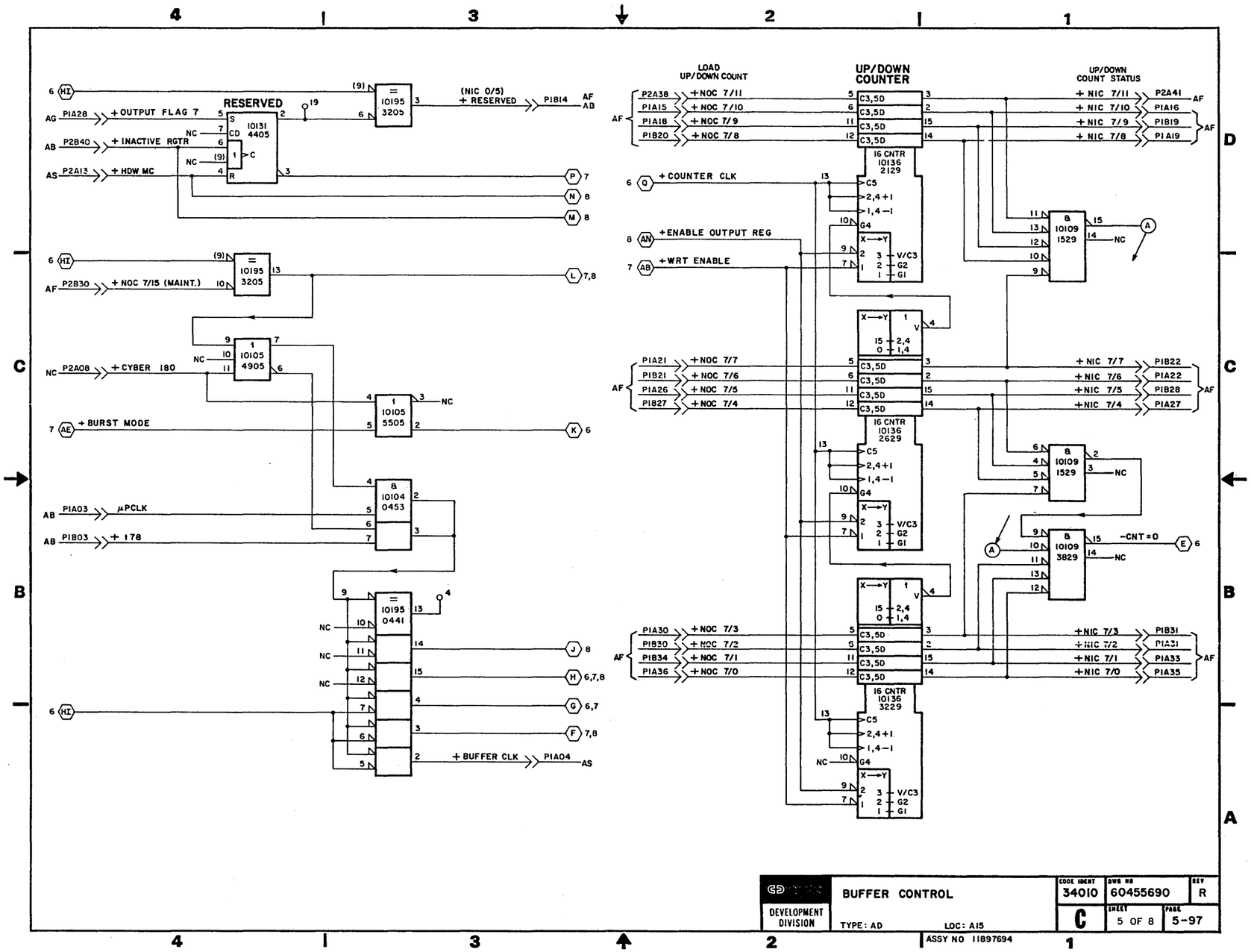

4
3
2
1
D
C
B
A
NC
(9)
=1
10195
6653
P2B36
P2A35
P2B35
P2B41
2
0
3
1
4
2
13
3
10195
6053
P2A26
+BUFFMEM 11
P2B26
+BUFFMEM 10
P2A25
+BUFFMEM 9
P2A31
+BUFFMEM 8
AB
5
4
6
5
7
6
10
7
+CATCH REG FULL
+CATCH REG RESET
AA
AJ
CATCHING REGISTER
RGTR
10173
6641
C3
C2
C1
C2,3D
C1,3D
16
P2A36
-DESKEW 15
P2B37
-DESKEW 14
P2A37
-DESKEW 13
P2B38
-DESKEW 12
AR
-EX WRT DATA 15
P2A34
-EX WRT DATA 14
P2B43
-EX WRT DATA 13
P2A42
-EX WRT DATA 12
P2B42
AJ(A23)
RGTR
10173
6041
P2B27
-DESKEW 11
P2A27
-DESKEW 10
P2B28
-DESKEW 9
P2B31
-DESKEW 8
-EX WRT DATA 11
P2A24
-EX WRT DATA 10
P2A28
-EX WRT DATA 9
P2B25
-EX WRT DATA 8
P2A32
AJ(A24)
10195
5553
P2A17
P2B17
P2B15
P2A22
10195
4953
P2A10
P2A09
P2B09
P2B12
RGTR
10173
5541
P2A20
-DESKEW 7
P2B21
-DESKEW 6
P2B22
-DESKEW 5
P2A18
-DESKEW 4
-EX WRT DATA 7
P2B29
-EX WRT DATA 6
P2B32
-EX WRT DATA 5
P2A16
-EX WRT DATA 4
P2B16
AJ
(A25)
RGTR
10173
4941
P2A11
-DESKEW 3
P2B10
-DESKEW 2
P2B13
-DESKEW 1
P2A12
-DESKEW 0
-EX WRT DATA 3
P2A21
-EX WRT DATA 2
P2B24
-EX WRT DATA 1
P2B20
-EX WRT DATA 0
P2B18
AJ
(A26)
DEVELOPMENT DIVISION
BUFFER CONTROL
TYPE: AD
LOC: A15
ASSY NO 11897694
CODE IDENT
34010
DWG NO
60455690
REV
R
C
SHEET
1 OF 8
PAGE
5-93

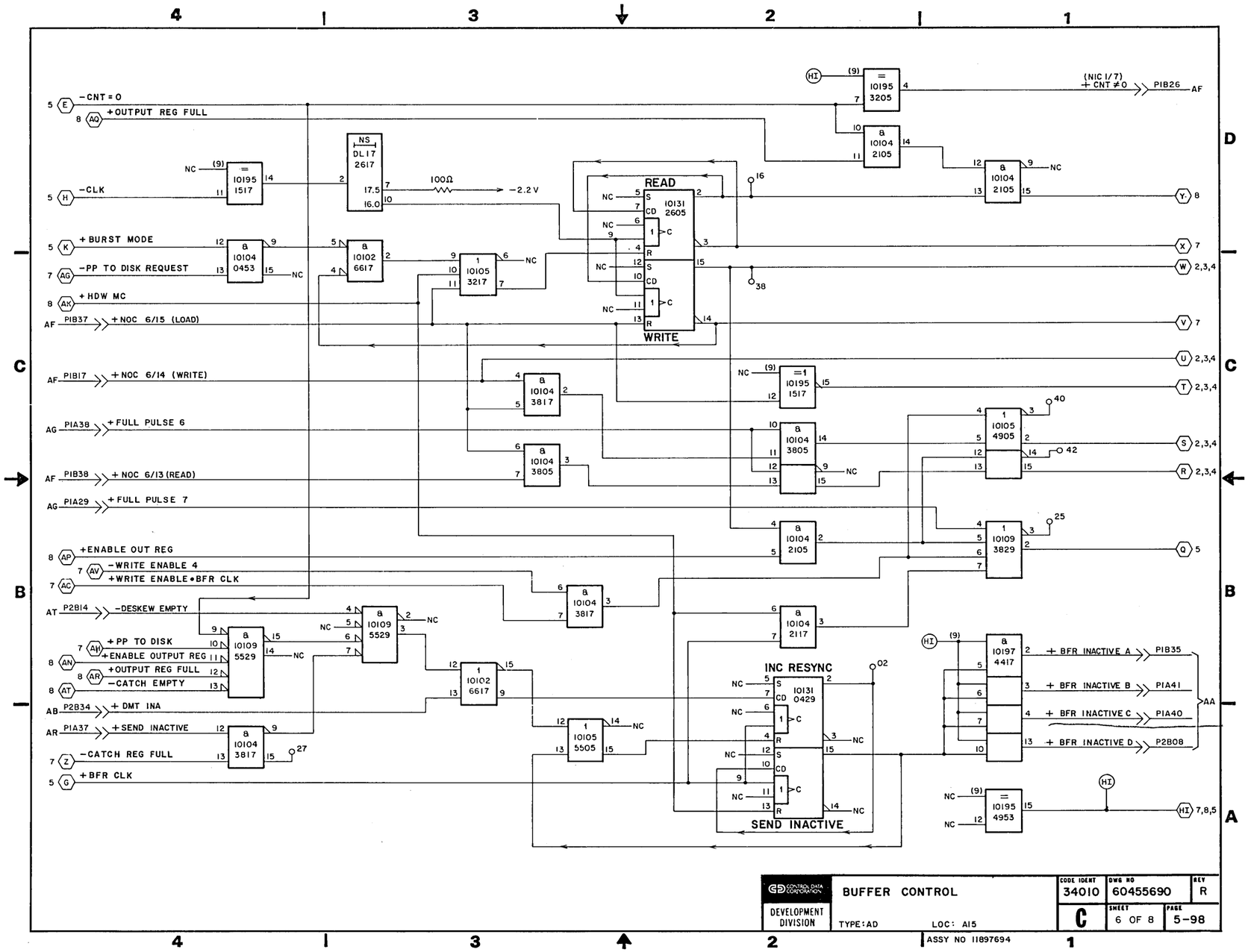


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	BUFFER CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AD LOC: A15 ASSY NO 11897694	C	SHEET 2 OF 8	PAGE 5-94

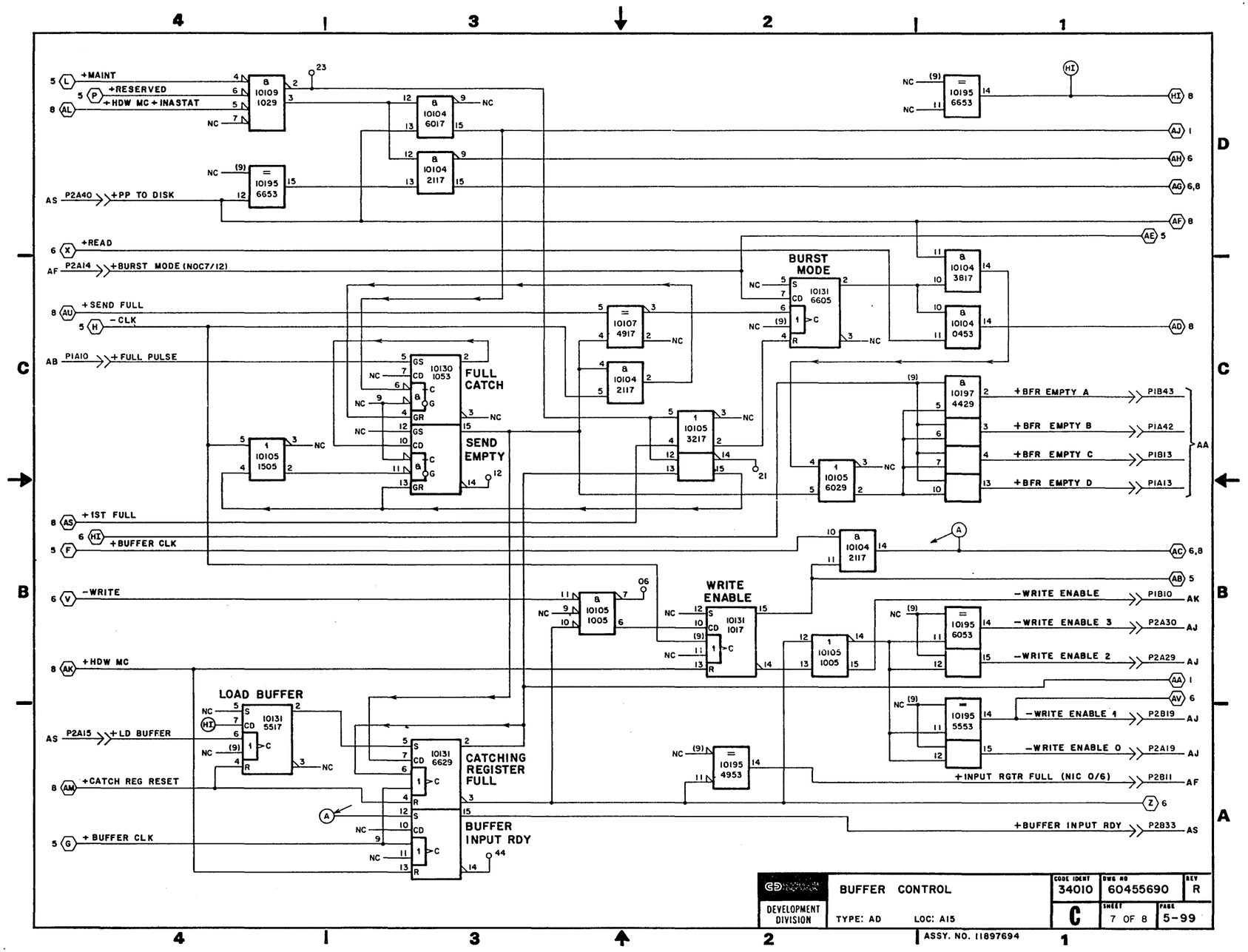

4
3
2
1
D
C
B
A
NIC 6 MUX
BUFFER MEMORY ADDRESS MUX
READ ADDRESS
WRITE ADDRESS
LOAD BUFFER ADDRESS
+WRITE (NOC 6/14)
+RD CLK
+WRT AND CARRY
+LOAD (NOC 6/15)
+WRITE FF
+WRT CLK
+RD AND CARRY
PIB32 + NOC 6/7
PIB12 + NOC 6/6
PIB33 + NOC 6/5
PIA32 + NOC 6/4
16 CNTR 10136 3241
16 CNTR 10136 2641
RGTR 10173 2653
RGTR 10173 3253
BUFFER ADDRESS STATUS
+ NIC 6/7 PIA08
+ NIC 6/6 PIB08
+ NIC 6/5 PIA07
+NIC 6/4 PIB07
+ BMA 2^7 PIA12
+ BMA 2^6 PIA09
+ BMA 2^5 P2A43
+ BMA 2^4 P1B09
DEVELOPMENT DIVISION
BUFFER CONTROL
TYPE: AD
LOC: A15
ASSY NO 11897694
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 8
PAGE 5-95


+WRITE (NOC 6/14)
WRITE ADDRESS
LOAD BUFFER ADDRESS
P2B04 +NOC 6/3
P2A04 +NOC 6/2
P2B05 +NOC 6/1
P2A05 +NOC 6/0
AF
16 CNTR 10136 4441
+LOAD (NOC 6/15)
+WRITE FF
READ ADDRESS
16 CNTR 10136 3841
NIC 6 MUX
RGTR 10173 3853
BUFFER ADDRESS STATUS
+NIC 6/3 P1A11
+NIC 6/2 P1B11
+NIC 6/1 P1B40
+NIC 6/0 P1B41
BUFFER MEMORY ADDRESS MUX
RGTR 10173 4453
+BMA 2^3 P2A03
+BMA 2^2 P2B03
+BMA 2^1 P2B07
+BMA 2^0 P2A07
AK
BUFFER CONTROL
DEVELOPMENT DIVISION
TYPE: AD
LOC: A15
ASSY NO 11897694
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 4 OF 8
PAGE 5-96

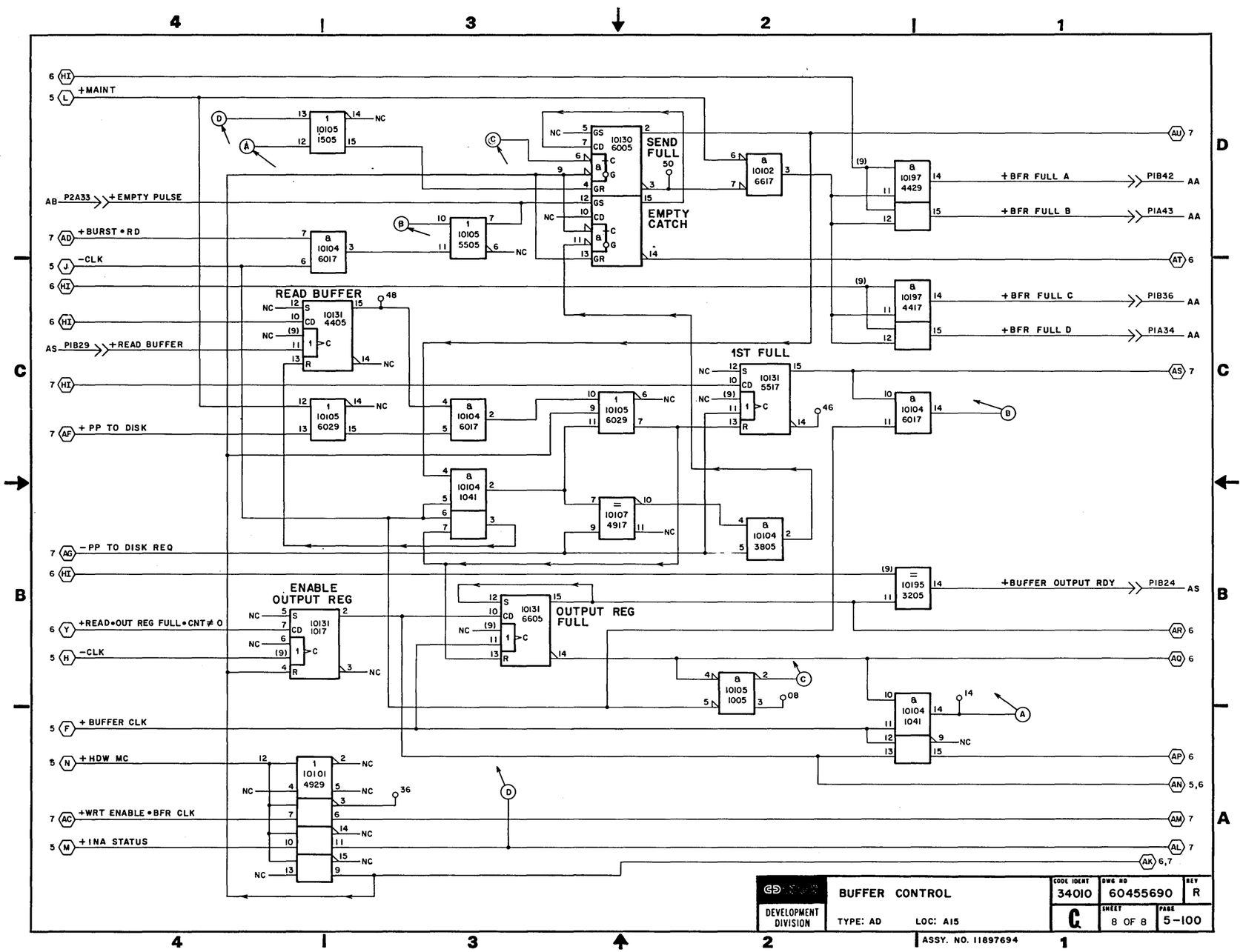

RESERVED
LOAD UP/DOWN COUNT
UP/DOWN COUNTER
UP/DOWN COUNT STATUS
+OUTPUT FLAG 7
+INACTIVE RGTR
+HDW MC
(NIC 0/5) + RESERVED
+NOC 7/15 (MAINT.)
+CYBER 180
+BURST MODE
μPCLK
+178
+BUFFER CLK
+COUNTER CLK
+ENABLE OUTPUT REG
+WRT ENABLE
+NOC 7/11
+NOC 7/10
+NOC 7/9
+NOC 7/8
+NOC 7/7
+NOC 7/6
+NOC 7/5
+NOC 7/4
+NOC 7/3
+NOC 7/2
+NOC 7/1
+NOC 7/0
+NIC 7/11
+NIC 7/10
+NIC 7/9
+NIC 7/8
+NIC 7/7
+NIC 7/6
+NIC 7/5
+NIC 7/4
+NIC 7/3
+NIC 7/2
+NIC 7/1
+NIC 7/0
-CNT=0
BUFFER CONTROL
TYPE: AD
LOC: A15
ASSY NO 11897694
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 5 OF 8
PAGE 5-97

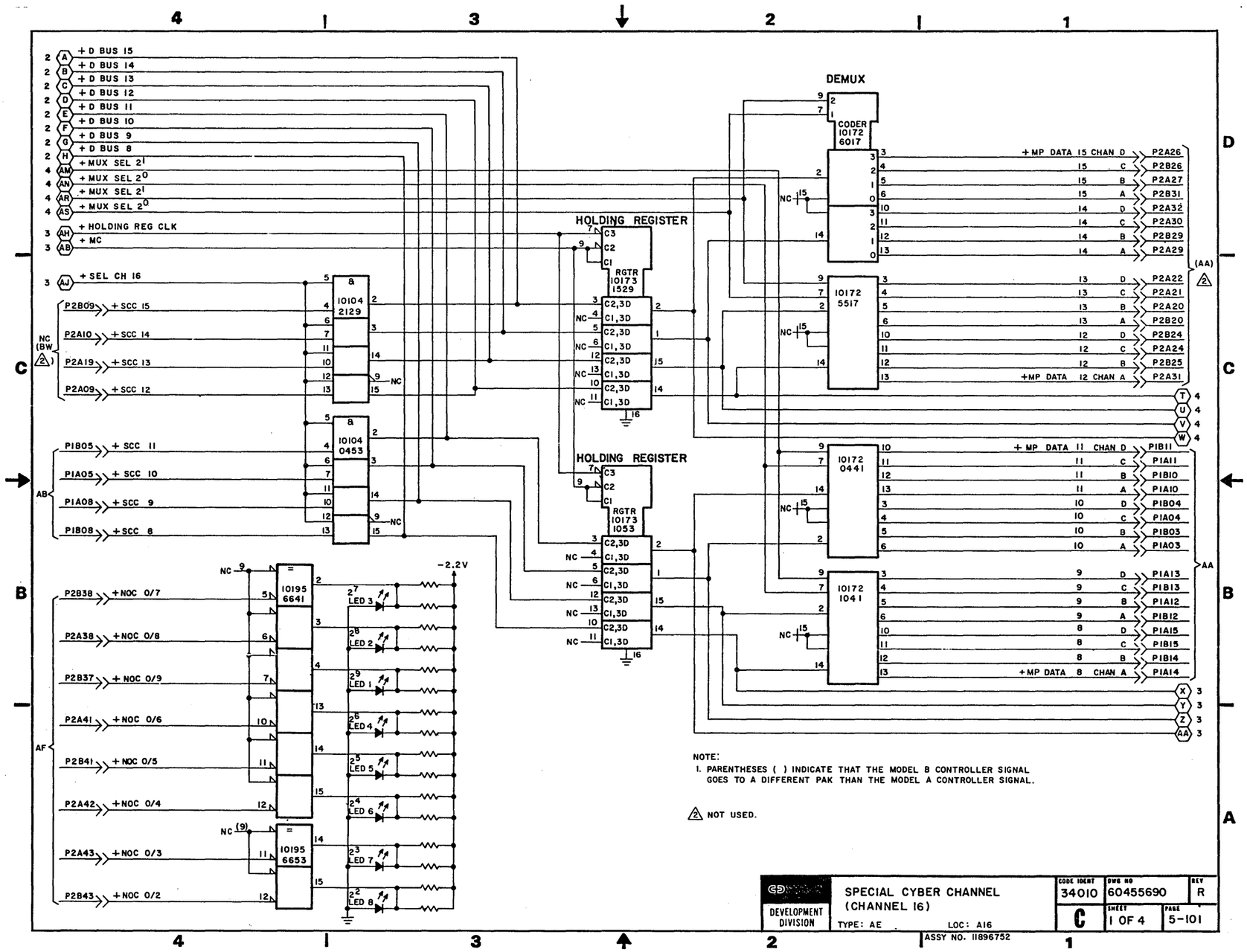


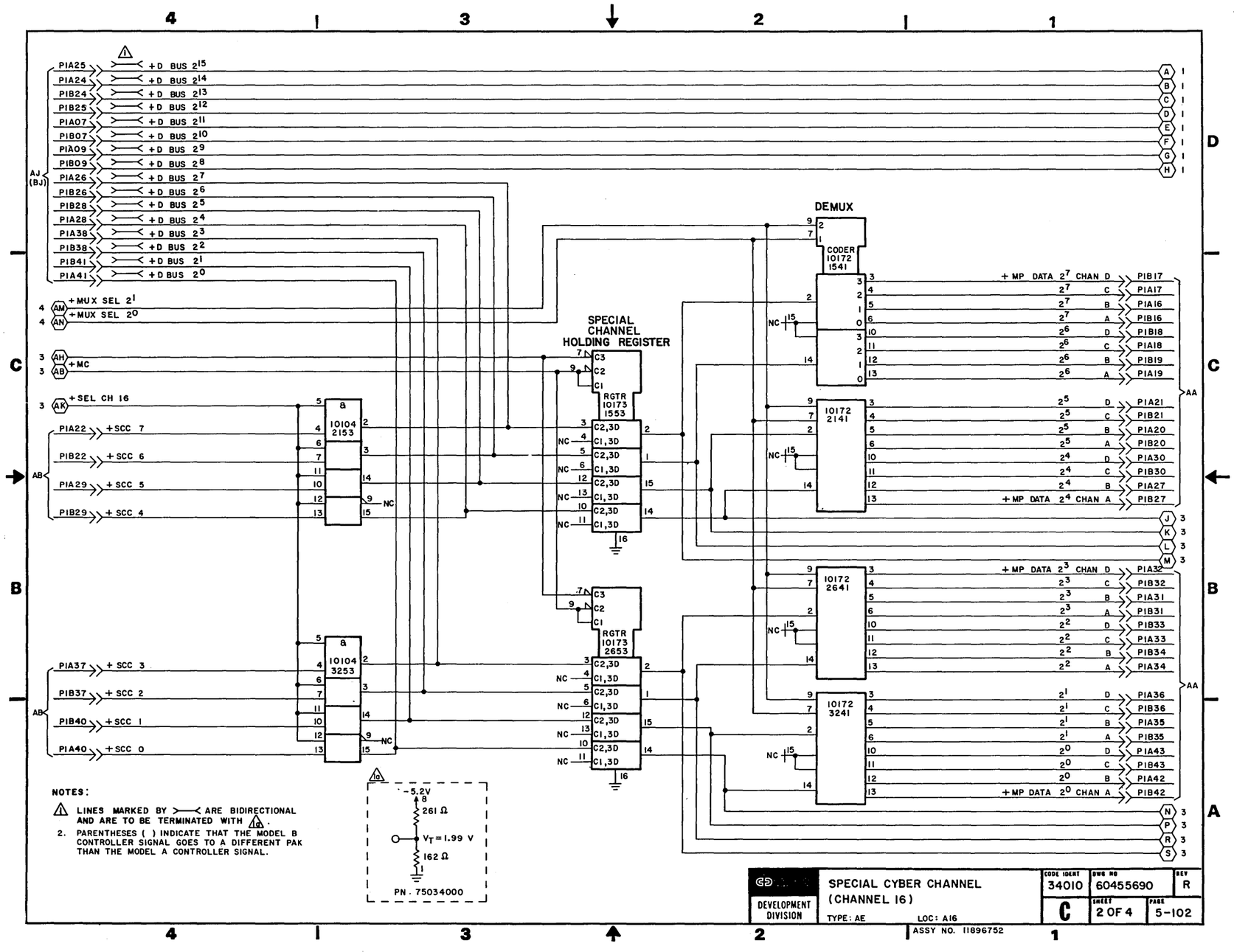
CONTROL DATA CORPORATION	BUFFER CONTROL		CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AD	LOC: AI5	C	SHEET 6 OF 8	PAGE 5-98
	ASSY NO 11897694				



DEVELOPMENT DIVISION	BUFFER CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AD LOC: A15	C	SHEET 7 OF 8	PAGE 5-99
	ASSY. NO. 11897694			


4
3
2
1
D
C
B
A
6 HI
5 L +MAINT
AB P2A33 +EMPTY PULSE
7 AD +BURST • RD
5 J -CLK
6 HI
6 HI
AS P1B29 +READ BUFFER
7 HI
7 AF + PP TO DISK
7 AG -PP TO DISK REQ
6 HI
6 Y +READ • OUT REG FULL • CNT ≠ 0
5 H -CLK
5 F + BUFFER CLK
5 N + HDW MC
7 AC +WRT ENABLE • BFR CLK
5 M + INA STATUS
SEND FULL 50
EMPTY CATCH
READ BUFFER
1ST FULL
ENABLE OUTPUT REG
OUTPUT REG FULL
+BFR FULL A
+BFR FULL B
+BFR FULL C
+BFR FULL D
+BUFFER OUTPUT RDY
AU 7
AT 6
AS 7
AR 6
AQ 6
AP 6
AN 5,6
AM 7
AL 7
AK 6,7
PIB42 AA
PIA43 AA
PIB36 AA
PIA34 AA
PIB24 AS
GD DEVELOPMENT DIVISION
BUFFER CONTROL
TYPE: AD LOC: A15
ASSY. NO. 11897694
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 8 OF 8
PAGE 5-100

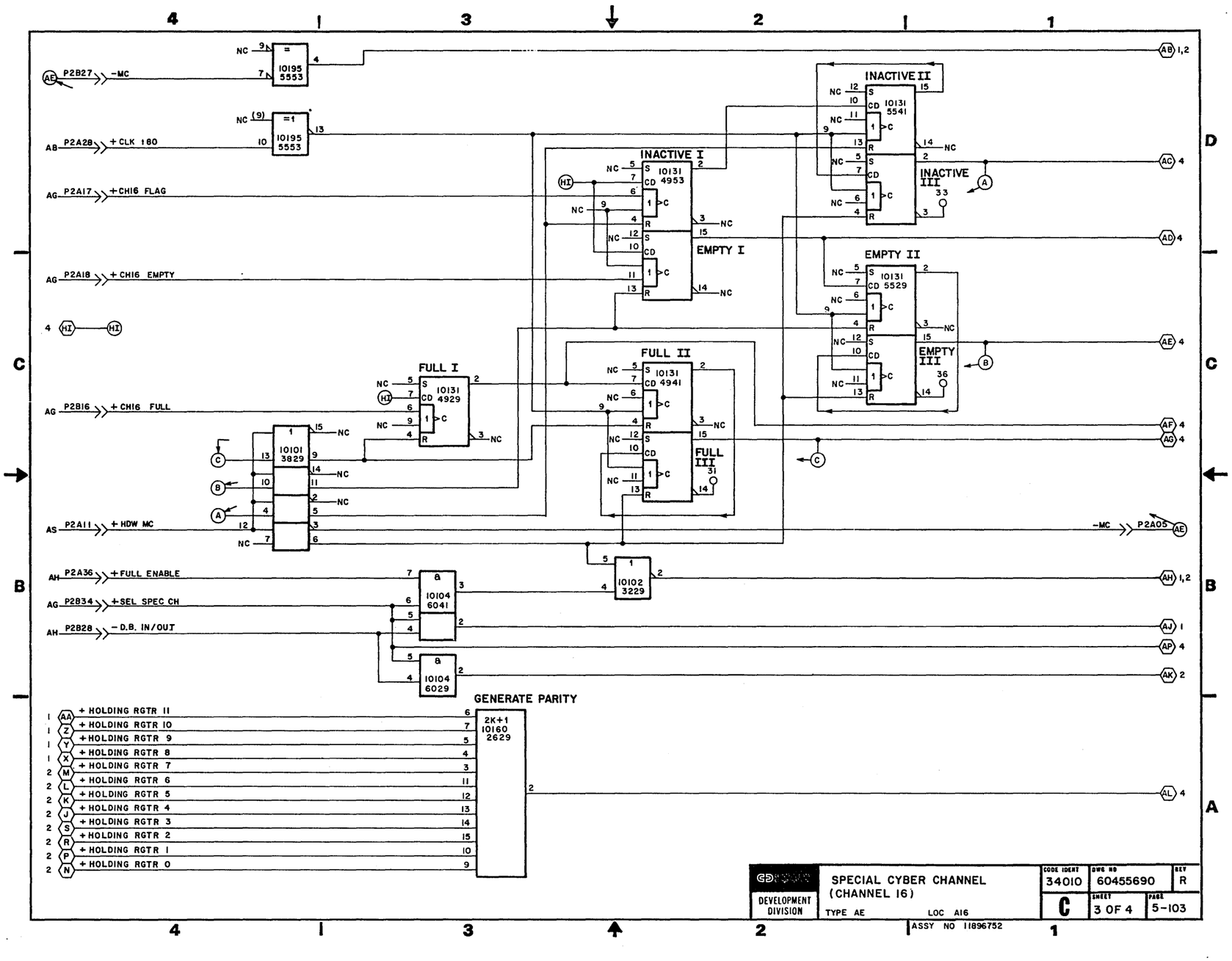

+ D BUS 15
+ D BUS 14
+ D BUS 13
+ D BUS 12
+ D BUS 11
+ D BUS 10
+ D BUS 9
+ D BUS 8
+ MUX SEL 2^1
+ MUX SEL 2^0
+ MUX SEL 2^1
+ MUX SEL 2^0
+ HOLDING REG CLK
+ MC
+ SEL CH 16
P2B09 + SCC 15
P2A10 + SCC 14
P2A19 + SCC 13
P2A09 + SCC 12
NC (BW 2)
P1B05 + SCC 11
P1A05 + SCC 10
P1A08 + SCC 9
P1B08 + SCC 8
AB
10104 2129
10104 0453
P2B38 + NOC 0/7
P2A38 + NOC 0/8
P2B37 + NOC 0/9
P2A41 + NOC 0/6
P2B41 + NOC 0/5
P2A42 + NOC 0/4
P2A43 + NOC 0/3
P2B43 + NOC 0/2
AF
10195 6641
10195 6653
-2.2V
LED 3
LED 2
LED 1
LED 4
LED 5
LED 6
LED 7
LED 8
HOLDING REGISTER
RGTR 10173 1529
RGTR 10173 1053
C3
C2
C1
C2,3D
C1,3D
DEMUX
CODER 10172 6017
10172 5517
10172 0441
10172 1041
+MP DATA 15 CHAN D
+MP DATA 12 CHAN A
+MP DATA 11 CHAN D
+MP DATA 8 CHAN A
P2A26
P2B26
P2A27
P2B31
P2A32
P2A30
P2B29
P2A29
P2A22
P2A21
P2A20
P2B20
P2B24
P2A24
P2B25
P2A31
P1B11
P1A11
P1B10
P1A10
P1B04
P1A04
P1B03
P1A03
P1A13
P1B13
P1A12
P1B12
P1A15
P1B15
P1B14
P1A14
(AA)
AA
NOTE:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
2 NOT USED.
DEVELOPMENT DIVISION
SPECIAL CYBER CHANNEL (CHANNEL 16)
TYPE: AE
LOC: A16
ASSY NO. 11896752
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 4
PAGE 5-101

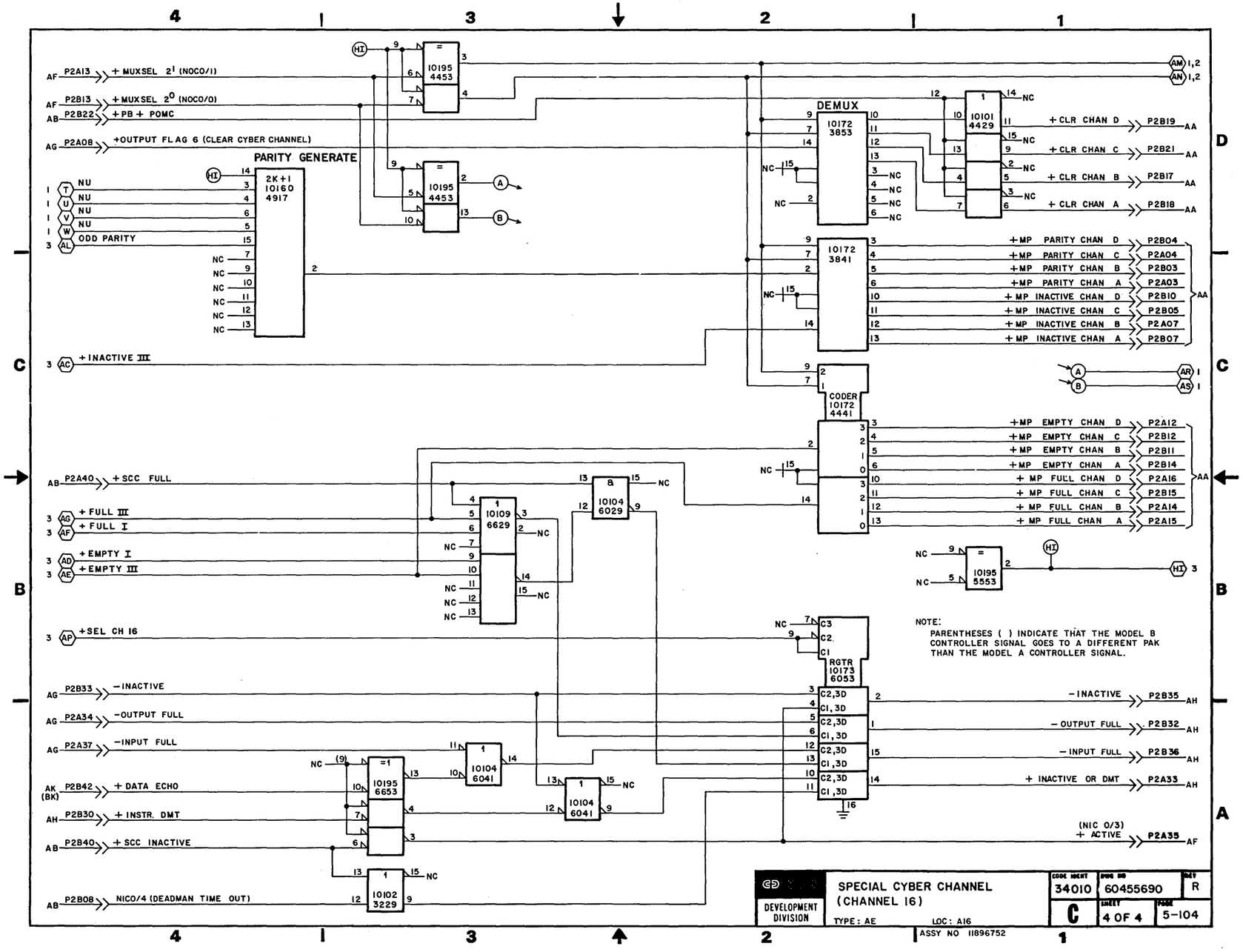


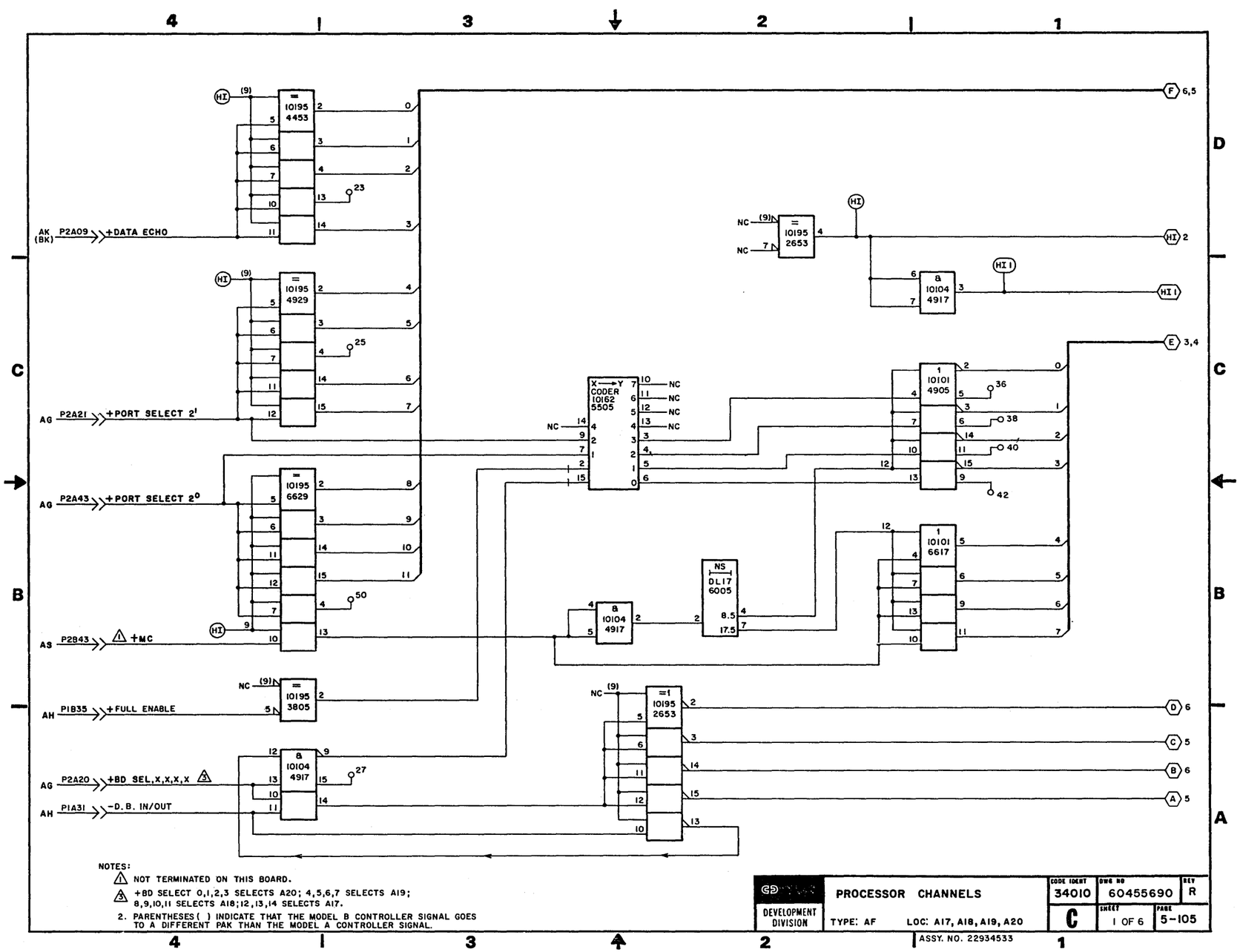
NOTES:

1. LINES MARKED BY >—< ARE BIDIRECTIONAL AND ARE TO BE TERMINATED WITH 1Ω.
2. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

DEVELOPMENT DIVISION	SPECIAL CYBER CHANNEL (CHANNEL 16)	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AE LOC: A16 ASSY NO. 11896752		C	SHEET 2 OF 4	PAGE 5-102


4
3
2
1
D
C
B
A
P2B27 -MC
P2A28 +CLK 180
P2A17 +CHI6 FLAG
P2A18 +CHI6 EMPTY
P2B16 +CHI6 FULL
P2A11 +HDW MC
P2A36 +FULL ENABLE
P2B34 +SEL SPEC CH
P2B28 -D.B. IN/OUT
10195 5553
10101 3829
10131 4953
10131 4929
10131 5541
10131 5529
10131 4941
10102 3229
10104 6041
10104 6029
INACTIVE I
INACTIVE II
INACTIVE III
EMPTY I
EMPTY II
EMPTY III
FULL I
FULL II
FULL III
GENERATE PARITY
2K+1 10160 2629
+HOLDING RGTR 11
+HOLDING RGTR 10
+HOLDING RGTR 9
+HOLDING RGTR 8
+HOLDING RGTR 7
+HOLDING RGTR 6
+HOLDING RGTR 5
+HOLDING RGTR 4
+HOLDING RGTR 3
+HOLDING RGTR 2
+HOLDING RGTR 1
+HOLDING RGTR 0
-MC P2A05
SPECIAL CYBER CHANNEL
(CHANNEL 16)
TYPE AE
LOC A16
ASSY NO 11896752
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 4
PAGE 5-103

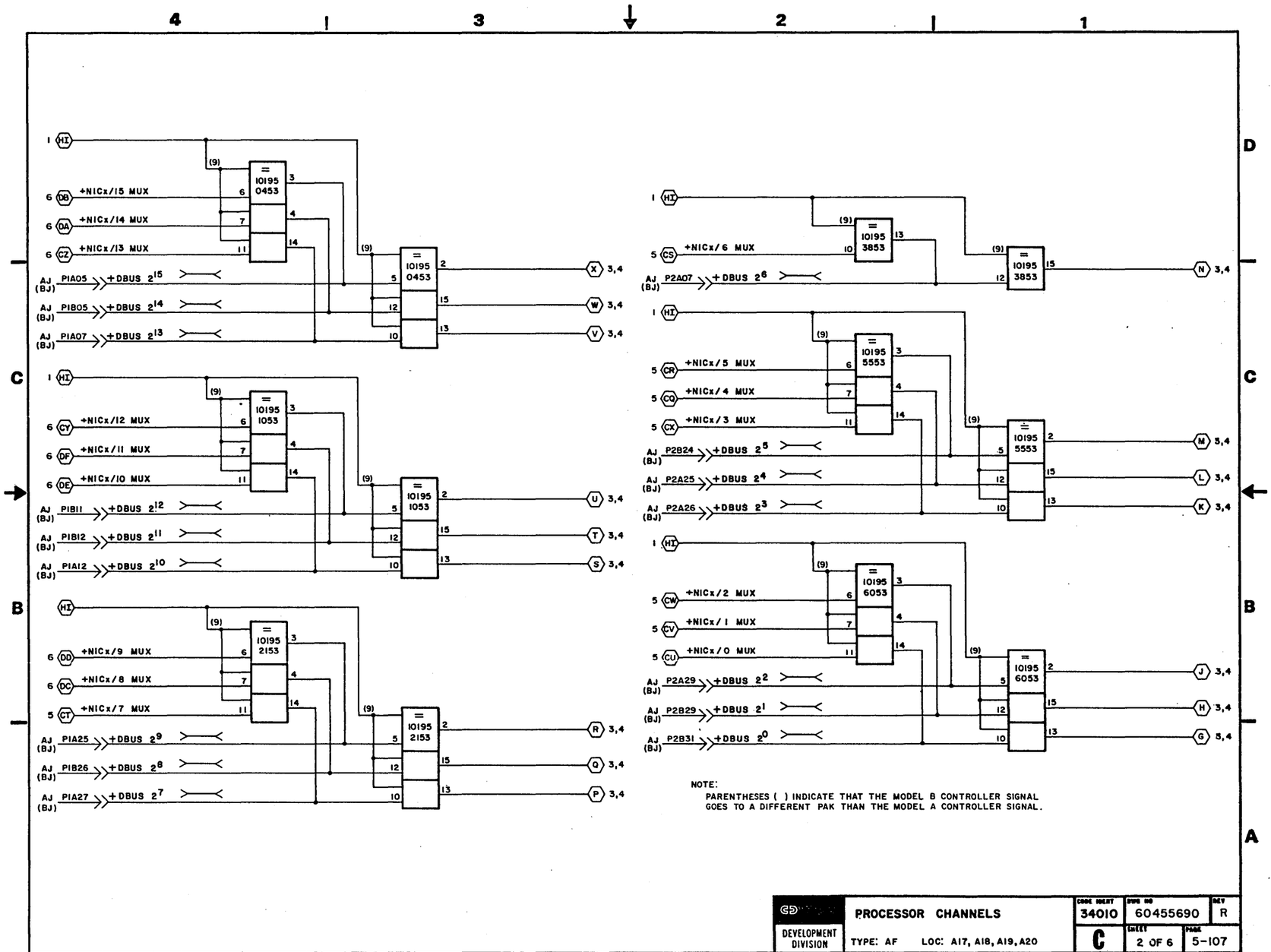

PARITY GENERATE
DEMUX
10172 3853
10172 3841
CODER 10172 4441
RGTR 10173 6053
2K+1 10160 4917
10195 4453
10101 4429
10195 5553
10195 6653
10109 6629
10104 6029
10104 6041
10102 3229
AF P2A13 + MUXSEL 2¹ (NOCO/1)
AF P2B13 + MUXSEL 2⁰ (NOCO/0)
AB P2B22 + PB + POMC
AG P2A08 +OUTPUT FLAG 6 (CLEAR CYBER CHANNEL)
NU
ODD PARITY
+INACTIVE III
AB P2A40 + SCC FULL
+ FULL III
+ FULL I
+ EMPTY I
+ EMPTY III
+SEL CH 16
AG P2B33 −INACTIVE
AG P2A34 −OUTPUT FULL
AG P2A37 −INPUT FULL
AK (BK) P2B42 + DATA ECHO
AH P2B30 + INSTR. DMT
AB P2B40 + SCC INACTIVE
AB P2B08 NICO/4 (DEADMAN TIME OUT)
+ CLR CHAN D P2B19 AA
+ CLR CHAN C P2B21 AA
+ CLR CHAN B P2B17 AA
+ CLR CHAN A P2B18 AA
+MP PARITY CHAN D P2B04
+MP PARITY CHAN C P2A04
+MP PARITY CHAN B P2B03
+MP PARITY CHAN A P2A03
+MP INACTIVE CHAN D P2B10
+MP INACTIVE CHAN C P2B05
+MP INACTIVE CHAN B P2A07
+MP INACTIVE CHAN A P2B07
+MP EMPTY CHAN D P2A12
+MP EMPTY CHAN C P2B12
+MP EMPTY CHAN B P2B11
+MP EMPTY CHAN A P2B14
+MP FULL CHAN D P2A16
+MP FULL CHAN C P2B15
+MP FULL CHAN B P2A14
+MP FULL CHAN A P2A15
−INACTIVE P2B35 AH
−OUTPUT FULL P2B32 AH
−INPUT FULL P2B36 AH
+ INACTIVE OR DMT P2A33 AH
(NIC 0/3) + ACTIVE P2A35 AF
AM 1,2
AN 1,2
AR 1
AS 1
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
SPECIAL CYBER CHANNEL (CHANNEL 16)
DEVELOPMENT DIVISION
TYPE: AE
LOC: A16
ASSY NO 11896752
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 4 OF 4
PAGE 5-104



NOTES:

1. NOT TERMINATED ON THIS BOARD.
2. +BD SELECT 0,1,2,3 SELECTS A20; 4,5,6,7 SELECTS A19; 8,9,10,11 SELECTS A18; 12,13,14 SELECTS A17.
2. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

DEVELOPMENT DIVISION	PROCESSOR CHANNELS		CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AF	LOC: A17, A18, A19, A20	C	SHEET 1 OF 6	PAGE 5-105
		ASSY. NO. 22934533			

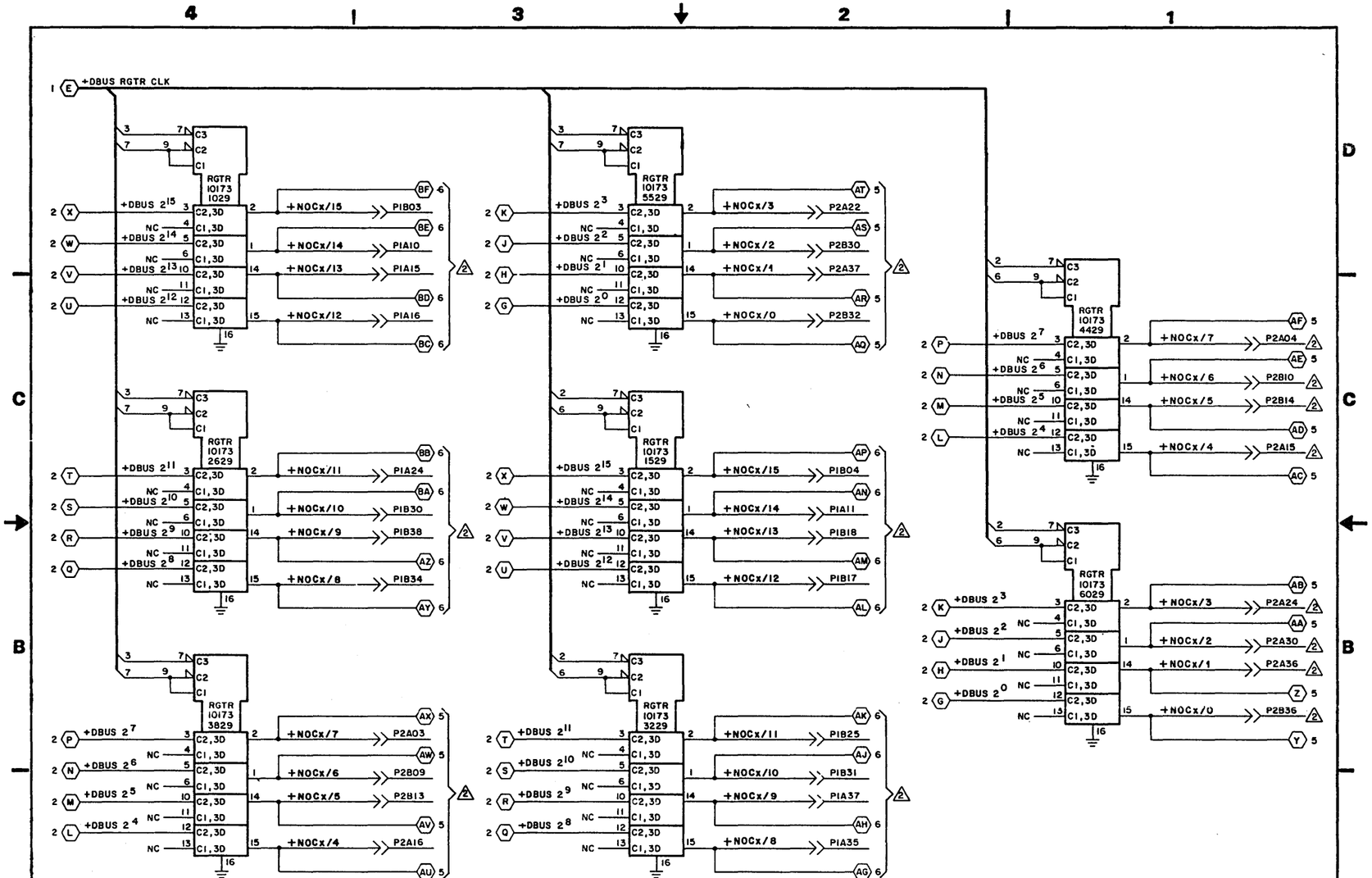


NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CD DEVELOPMENT DIVISION	PROCESSOR CHANNELS TYPE: AF LOC: A17, A18, A19, A20	CODE IDENT 34010	DWG NO 60455690	REV R
	ASSY. NO. 22934533	SIZE C	SHEET 2 OF 6	PAGE 5-107

Connector Pin	LOC A17		LOC A18		LOC A19		LOC A20	
	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination
P1B03	NOC12/15	AC,AF	NOC8/15	AM	NOC4/15	AR	NC	
P1A10	NOC12/14		NOC8/14	AM	NOC4/14	AR	NC	
P1A15	NOC12/13		NOC8/13	AM	NOC4/13	AR	NC	
P1A16	NOC12/12		NOC8/12	AM	NOC4/12	AR	NC	
P1A24	NOC12/11		NOC8/11	AM	NOC4/11	AR	NC	
P1B30	NOC12/10		NOC8/10	AM	NOC4/10	AR	NC	
P1B38	NOC12/9		NOC8/9	AM	NOC4/9	AR	NOC0/9	AE
P1B34	NOC12/8		NOC8/8	AM	NOC4/8	AR	NOC0/8	AE
P2A03	NOC12/7		NOC8/7	AM	NOC4/7	AR	NOC0/7	AE
P2B09	NOC12/6		NOC8/6	AM	NOC4/6	AR	NOC0/6	AE
P2B13	NOC12/5		NOC8/5	AM	NOC4/5	AR	NOC0/5	AE
P2A16	NOC12/4		NOC8/4	AM	NOC4/4	AR	NOC0/4	AE
P2A22	NOC12/3		NOC8/3	AM	NOC4/3	AR	NOC0/3	AE
P2B30	NOC12/2		NOC8/2	AM	NOC4/2	AR	NOC0/2	AE
P2A37	NOC12/1		NOC8/1	AM	NOC4/1	AR	NOC0/1	AB,AE
P2B32	NOC12/0		NOC8/0	AM	NOC4/0	AR	NOC0/0	AB,AE
P1B04	NOC13/15		NC		NOC5/15	AR	NOC1/15	AM
P1A11	NOC13/14		NC		NOC5/14	AR	NOC1/14	AM
P1B18	NOC13/13		NC		NOC5/13	AR	NOC1/13	AJ (BJ)
P1B17	NOC13/12		NC		NOC5/12	AR	NOC1/12	AJ (BJ)
P1B25	NOC13/11		NC		NOC5/11	AR	NOC1/11	AM
P1B31	NOC13/10		NC		NOC5/10	AR	NOC1/10	AM
P1A37	NOC13/9		NC		NOC5/9	AR	NOC1/9	AH
P1A35	NOC13/8		NC		NOC5/8	AR	NC	
P2A04	NOC13/7		NOC9/7	AP	NOC5/7	AR	NOC1/7	AM
P2B10	NOC13/6		NOC9/6	AN	NOC5/6	AR	NOC1/6	AM
P2B14	NOC13/5		NOC9/5	AN	NOC5/5	AR	NOC1/5	AS
P2A15	NOC13/4		NOC9/4	AN	NOC5/4	AR	NC	
P2A24	NOC13/3		NOC9/3	AP	NOC5/3	AR	NOC1/3	AP
P2A30	NOC13/2		NOC9/2	AP	NOC5/2	AR	NOC1/2	AP
P2A36	NOC13/1		NOC9/1	AP	NOC5/1	AR	NOC1/1	AP
P2B36	NOC13/0	AC,AF	NOC9/0	AP	NOC5/0	AR	NOC1/0	AP

NOTE: ALL SIGNALS POSITIVE (+) POLARITY.



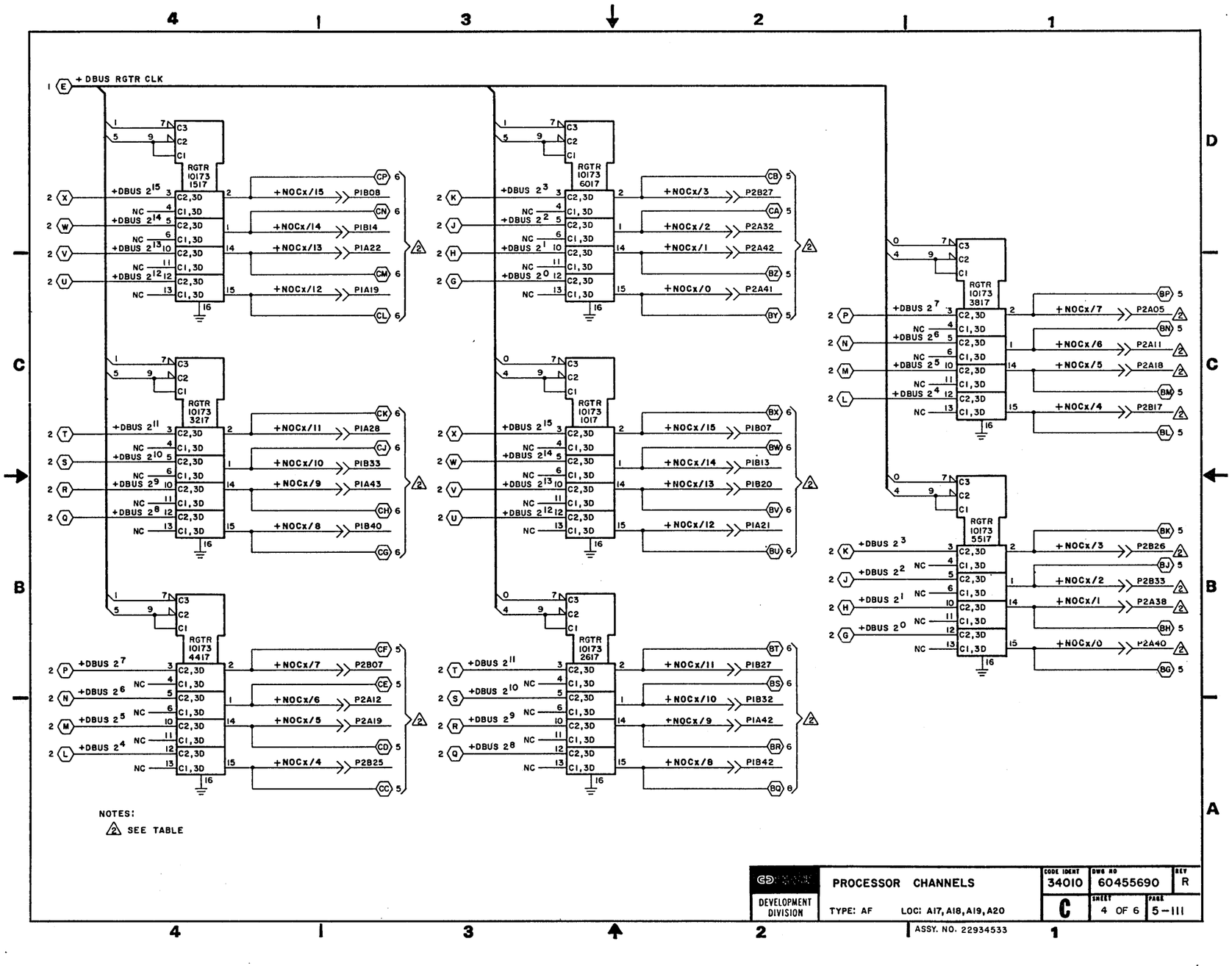
NOTES:

2 SEE TABLE

GD DEVELOPMENT DIVISION	PROCESSOR CHANNELS	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AF LOC: A17, A18, A19, A20 ASSY. NO. 22934533	C	SHEET 3 OF 6	PAGE 5-109

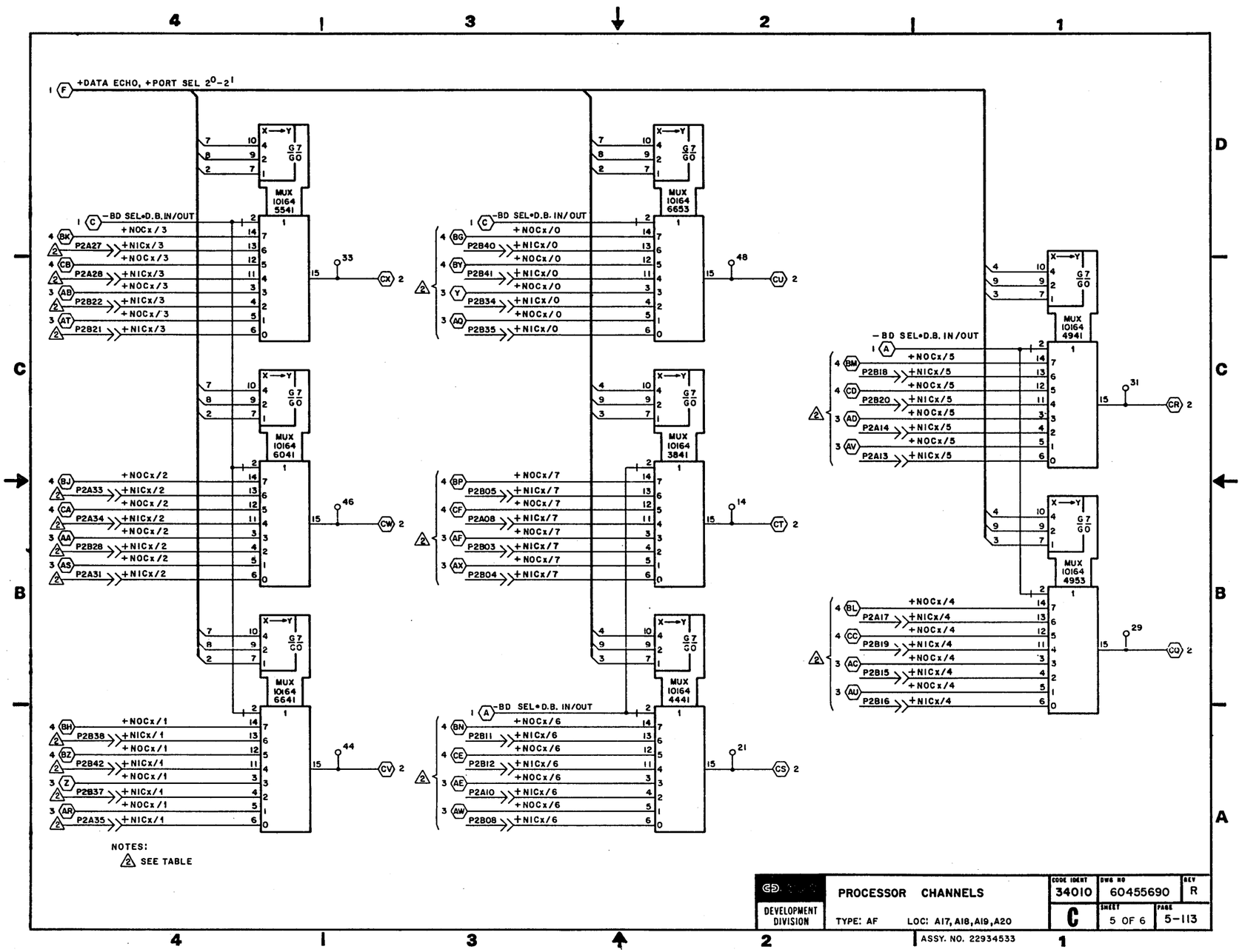
Connector Pin	LOC A17		LOC A18		LOC A19		LOC A20	
	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination
P1B08	NOC14/15	AC,AF	NOC10/15	AN	NOC6/15	AD (BD)		NC
P1B14	NOC14/14		NOC10/14	AN	NOC6/14	AD (BD)		NC
P1A22	NOC14/13		NOC10/13	AN	NOC6/13	AD (BD)		NC
P1A19	NOC14/12		NOC10/12	AN		NC		NC
P1A28	NOC14/11		NOC10/11	AP	NOC6/11	AD (BD)		NC
P1B33	NOC14/10		NOC10/10	AN	NOC6/10	AD (BD)		NC
P1A43	NOC14/9		NOC10/9	AN	NOC6/9	AD (BD)		NC
P1B40	NOC14/8		NOC10/8	AN	NOC6/8	AD (BD)		NC
P2B07	NOC14/7		NOC10/7	AN	NOC6/7	AD (BD)	NOC2/7	AS
P2A12	NOC14/6		NOC10/6	AN	NOC6/6	AD (BD)	NOC2/6	AS
P2A19	NOC14/5		NOC10/5	AN	NOC6/5	AD (BD)	NOC2/5	AR
P2B25	NOC14/4		NOC10/4	AN	NOC6/4	AD (BD)	NOC2/4	AR
P2B27	NOC14/3		NOC10/3	AN	NOC6/3	AD (BD)	NOC2/3	AR
P2A32	NOC14/2		NOC10/2	AN	NOC6/2	AD (BD)	NOC2/2	AB,AE
P2A42	NOC14/1		NOC10/1	AP	NOC6/1	AD (BD)	NOC2/1	AR
P2A41	NOC14/0	AC,AF	NOC10/0	AP	NOC6/0	AD (BD)	NOC2/0	AR
P1B07		NC	NOC11/15	AC,AF	NOC7/15	AD (BD),AS,AT		NC
P1B13		NC	NOC11/14		NOC7/14	AS		NC
P1B20		NC	NOC11/13		NOC7/13	AK (BK)		NC
P1A21		NC	NOC11/12		NOC7/12	AD (BD)		NC
P1B27		NC	NOC11/11		NOC7/11	AD (BD)		NC
P1B32		NC	NOC11/10		NOC7/10	AD (BD)		NC
P1A42		NC	NOC11/9		NOC7/9	AD (BD)		NC
P1B42		NC	NOC11/8		NOC7/8	AD (BD)		NC
P2A05		NC	NOC11/7		NOC7/7	AD (BD)		NC
P2A11		NC	NOC11/6		NOC7/6	AD (BD)		NC
P2A18		NC	NOC11/5		NOC7/5	AD (BD)		NC
P2B17		NC	NOC11/4		NOC7/4	AD (BD)		NC
P2B26		NC	NOC11/3		NOC7/3	AD (BD)		NC
P2B33		NC	NOC11/2		NOC7/2	AD (BD)		NC
P2A38		NC	NOC11/1		NOC7/1	AD (BD)	NOC3/1	AC
P2A40		NC	NOC11/0	AC,AF	NOC7/0	AD (BD)	NOC3/0	AC

NOTE: ALL SIGNALS POSITIVE (+) POLARITY.


+ DBUS RGTR CLK
RGTR 10173 1517
+DBUS 2^15
+DBUS 2^14
+DBUS 2^13
+DBUS 2^12
+NOCx/15
+NOCx/14
+NOCx/13
+NOCx/12
PIB08
PIB14
PIA22
PIA19
RGTR 10173 6017
+DBUS 2^3
+DBUS 2^2
+DBUS 2^1
+DBUS 2^0
+NOCx/3
+NOCx/2
+NOCx/1
+NOCx/0
P2B27
P2A32
P2A42
P2A41
RGTR 10173 3817
+DBUS 2^7
+DBUS 2^6
+DBUS 2^5
+DBUS 2^4
+NOCx/7
+NOCx/6
+NOCx/5
+NOCx/4
P2A05
P2A11
P2A18
P2B17
RGTR 10173 3217
+DBUS 2^11
+DBUS 2^10
+DBUS 2^9
+DBUS 2^8
+NOCx/11
+NOCx/10
+NOCx/9
+NOCx/8
PIA28
PIB33
PIA43
PIB40
RGTR 10173 1017
+DBUS 2^15
+DBUS 2^14
+DBUS 2^13
+DBUS 2^12
+NOCx/15
+NOCx/14
+NOCx/13
+NOCx/12
PIB07
PIB13
PIB20
PIA21
RGTR 10173 5517
+DBUS 2^3
+DBUS 2^2
+DBUS 2^1
+DBUS 2^0
+NOCx/3
+NOCx/2
+NOCx/1
+NOCx/0
P2B26
P2B33
P2A38
P2A40
RGTR 10173 4417
+DBUS 2^7
+DBUS 2^6
+DBUS 2^5
+DBUS 2^4
+NOCx/7
+NOCx/6
+NOCx/5
+NOCx/4
P2B07
P2A12
P2A19
P2B25
RGTR 10173 2617
+DBUS 2^11
+DBUS 2^10
+DBUS 2^9
+DBUS 2^8
+NOCx/11
+NOCx/10
+NOCx/9
+NOCx/8
PIB27
PIB32
PIA42
PIB42
NOTES:
2 SEE TABLE
PROCESSOR CHANNELS
TYPE: AF
LOC: A17, A18, A19, A20
ASSY. NO. 22934533
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 4 OF 6
PAGE 5-111

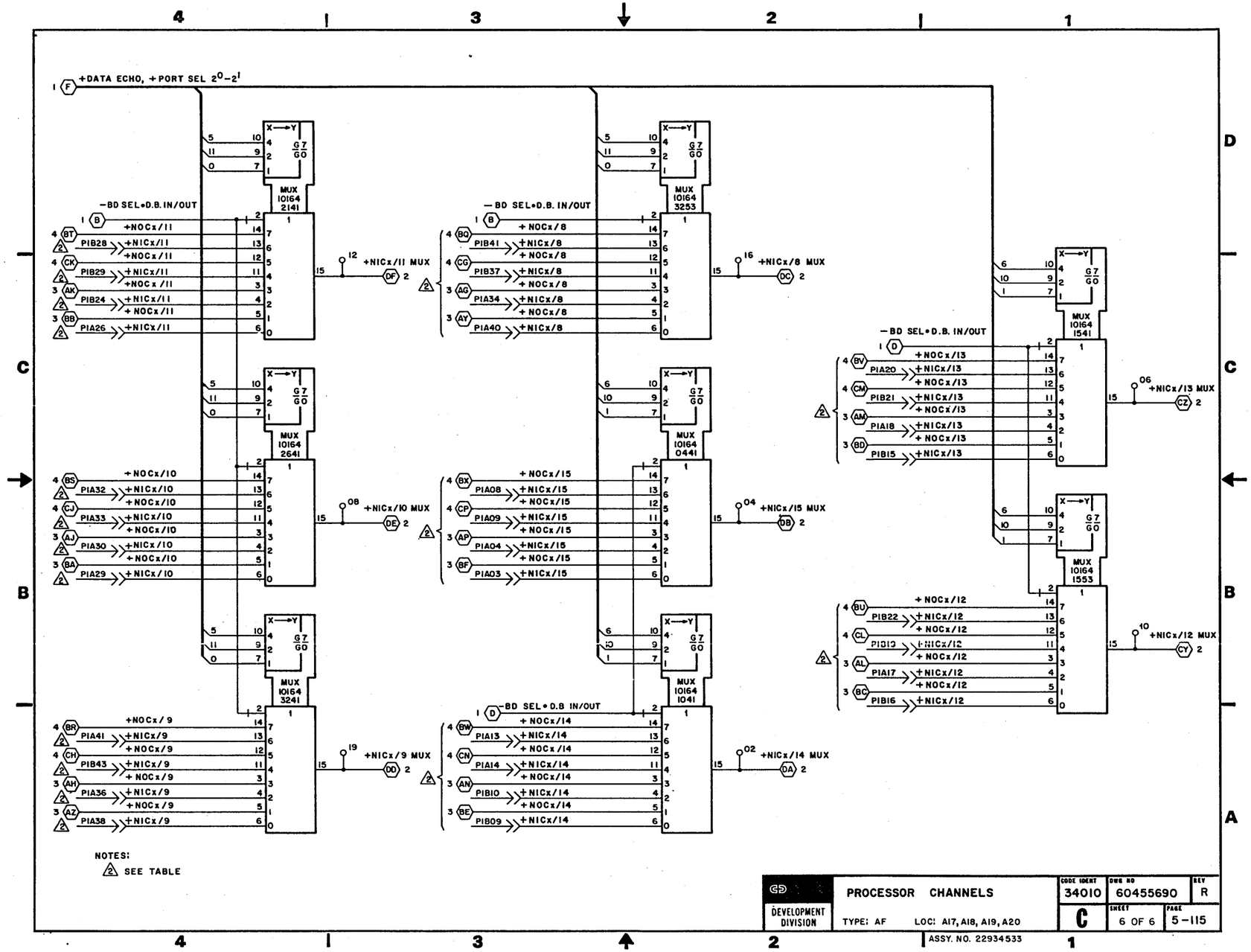
Connector Pin	LOC A17		LOC A18		LOC A19		LOC A20	
	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination
P2A27	NC		NIC11/3	AF	NIC7/3	AD (BD)	NIC3/3	AC
P2A28	NIC14/3	AF	NIC10/3	AN	NIC6/3	AD (BD)	NIC2/3	AR
P2B22	NIC13/3		NC		NIC5/3	AR	NIC1/3	AT
P2B21	NIC12/3		NIC8/3	AM	NIC4/3	AR	NIC0/3	AE
P2A33	NC		NIC11/2	AF	NIC7/2	AD (BD)	NIC3/2	AC
P2A34	NIC14/2		NIC10/2	AN	NIC6/2	AD (BD)	NIC2/2	AR
P2B28	NIC13/2		NIC9/2	AL	NIC5/2	AR	NIC1/2	AS
P2A31	NIC12/2		NIC8/2	AM	NIC4/2	AR	NIC0/2	AB
P2B38	NC		NIC11/1	AF	NIC7/1	AD (BD)	NIC3/1	AC
P2B42	NIC14/1		NIC10/1	AP	NIC6/1	AD (BD)	NIC2/1	AR
P2B37	NIC13/1		NIC9/1	AL	NIC5/1	AR	NIC1/1	AT
P2A35	NIC12/1		NIC8/1	AM	NIC4/1	AR	NIC0/1	AB
P2B40	NC		NIC11/0	AF	NIC7/0	AD (BD)	NIC3/0	AC
P2B41	NIC14/0		NIC10/0	AP	NIC6/0	AD (BD)	NIC2/0	AR
P2B34	NIC13/0		NIC9/0	AL	NIC5/0	AR	NIC1/0	AT
P2B35	NIC12/0		NIC8/0	AM	NIC4/0	AR	NIC0/0	AB
P2B05	NC		NIC11/7	AF	NIC7/7	AD (BD)	NIC3/7	AC
P2A08	NIC14/7		NIC10/7	AN	NIC6/7	AD (BD)	NIC2/7	AR
P2B03	NIC13/7		NC		NIC5/7	AR	NIC1/7	AD (BD)
P2B04	NIC12/7		NIC8/7	AM	NIC4/7	AR	NIC0/7	AS
P2B11	NC		NIC11/6	AF	NIC7/6	AD (BD)	NIC3/6	AC
P2B12	NIC14/6		NIC10/6	AN	NIC6/6	AD (BD)	NIC2/6	AR
P2A10	NIC13/6		NC		NIC5/6	AR	NIC1/6	AS
P2B08	NIC12/6		NIC8/6	AM	NIC4/6	AR	NIC0/6	AD (BD)
P2B18	NC		NIC11/5	AF	NIC7/5	AD (BD)	NIC3/5	AC
P2B20	NIC14/5		NIC10/5	AN	NIC6/5	AD (BD)	NIC2/5	AR
P2A14	NIC13/5		NC		NIC5/5	AR	NIC1/5	AS
P2A13	NIC12/5		NIC8/5	AM	NIC4/5	AR	NIC0/5	AD (BD)
P2A17	NC		NIC11/4	AF	NIC7/4	AD (BD)	NIC3/4	AC
P2B19	NIC14/4		NIC10/4	AP	NIC6/4	AD (BD)	NIC2/4	AR
P2B15	NIC13/4		NIC9/4	NC (AL)	NIC5/4	AR	NIC1/4	AS
P2B16	NIC12/4	AF	NIC8/4	AM	NIC4/4	AR	NIC0/4	AB

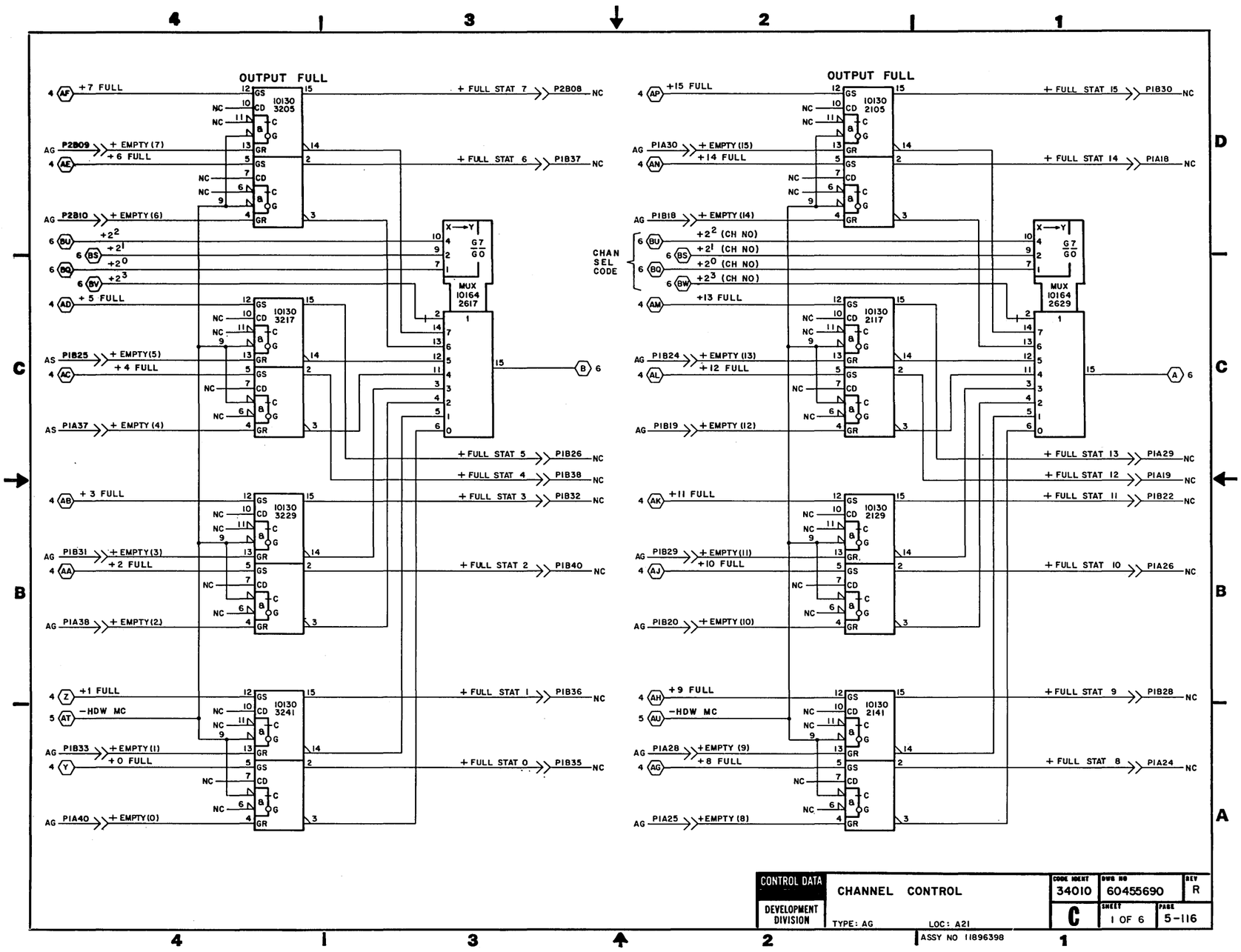
NOTE: ALL SIGNALS POSITIVE (+) POLARITY.


+DATA ECHO, +PORT SEL 2⁰-2¹
MUX 10164 5541
-BD SEL•D.B. IN/OUT
+NOCx/3
P2A27 +NICx/3
+NOCx/3
P2A28 +NICx/3
+NOCx/3
P2B22 +NICx/3
+NOCx/3
P2B21 +NICx/3
33
CX
MUX 10164 6653
-BD SEL•D.B. IN/OUT
+NOCx/0
P2B40 +NICx/0
+NOCx/0
P2B41 +NICx/0
+NOCx/0
P2B34 +NICx/0
+NOCx/0
P2B35 +NICx/0
48
CU
MUX 10164 4941
-BD SEL•D.B. IN/OUT
+NOCx/5
P2B18 +NICx/5
+NOCx/5
P2B20 +NICx/5
+NOCx/5
P2A14 +NICx/5
+NOCx/5
P2A13 +NICx/5
31
CR
MUX 10164 6041
+NOCx/2
P2A33 +NICx/2
+NOCx/2
P2A34 +NICx/2
+NOCx/2
P2B28 +NICx/2
+NOCx/2
P2A31 +NICx/2
46
CW
MUX 10164 3841
+NOCx/7
P2B05 +NICx/7
+NOCx/7
P2A08 +NICx/7
+NOCx/7
P2B03 +NICx/7
+NOCx/7
P2B04 +NICx/7
14
CT
MUX 10164 4953
+NOCx/4
P2A17 +NICx/4
+NOCx/4
P2B19 +NICx/4
+NOCx/4
P2B15 +NICx/4
+NOCx/4
P2B16 +NICx/4
29
CQ
MUX 10164 6641
+NOCx/1
P2B38 +NICx/1
+NOCx/1
P2B42 +NICx/1
+NOCx/1
P2B37 +NICx/1
+NOCx/1
P2A35 +NICx/1
44
CV
MUX 10164 4441
-BD SEL•D.B. IN/OUT
+NOCx/6
P2B11 +NICx/6
+NOCx/6
P2B12 +NICx/6
+NOCx/6
P2A10 +NICx/6
+NOCx/6
P2B08 +NICx/6
21
CS
NOTES:
2 SEE TABLE
GD
DEVELOPMENT DIVISION
PROCESSOR CHANNELS
TYPE: AF LOC: A17, A18, A19, A20
ASSY. NO. 22934533
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 5 OF 6
PAGE 5-113

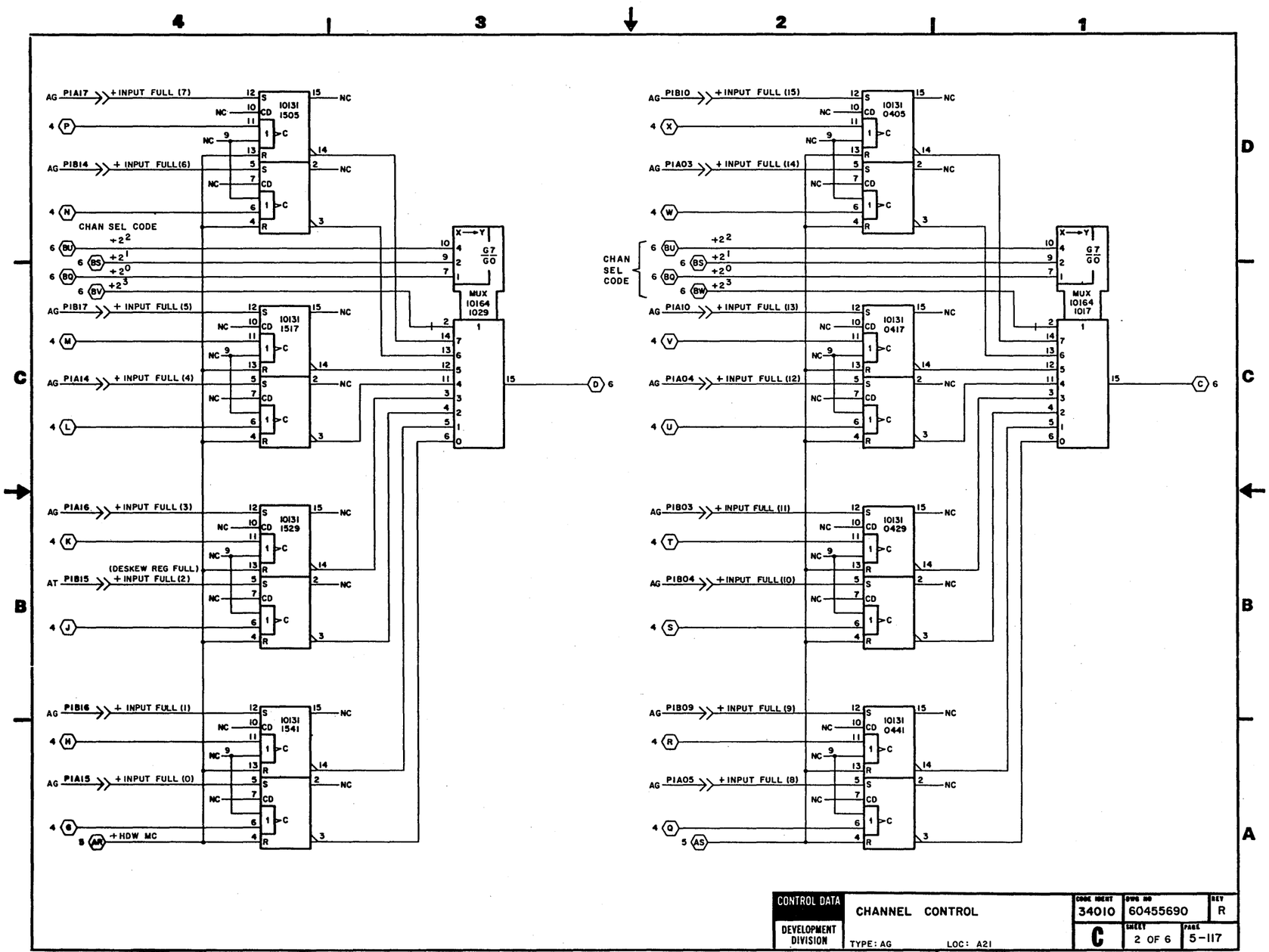
Connector Pin	LOC A17		LOC A18		LOC A19		LOC A20	
	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination	Signal Name	Destination
P1B28	NC		NIC11/11	AF	NIC7/11	AD (BD)	NIC3/11	AC
P1B29	NIC14/11		NIC10/11	AN	NIC6/11	AD (BD)	NIC2/11	AR
P1B24	NIC13/11		NIC9/11	NC (BW)	NIC5/11	AR	NIC1/11	AC
P1A26	NIC12/11		NIC8/11	AL	NIC4/11	AR	NC	
P1A32	NC		NIC11/10	AF	NIC7/10	AD (BD)	NIC3/10	AC
P1A33	NIC14/10		NIC10/10	AN	NIC6/10	AD (BD)	NIC2/10	AR
P1A30	NIC13/10		NIC9/10	NC (BW)	NIC5/10	AR	NIC1/10	AB
P1A29	NIC12/10		NIC8/10	AS	NIC4/10	AR	NC	
P1A41	NC		NIC11/9	AF	NIC7/9	AD (BD)	NIC3/9	AC
P1B43	NIC14/9		NIC10/9	AN	NIC6/9	AD (BD)	NIC2/9	AR
P1A36	NIC13/9		NIC9/9	NC (BW)	NIC5/9	AR	NIC1/9	AH
P1A38	NIC12/9		NIC8/9	AM	NIC4/9	AR	NC	
P1B41	NC		NIC11/8	AF	NIC7/8	AD (BD)	NIC3/8	AC
P1B37	NIC14/8		NIC10/8	AN	NIC6/8	AD (BD)	NIC2/8	AR
P1A34	NIC13/8		NIC9/8	NC (BW)	NIC5/8	AR	NIC1/8	AT
P1A40	NIC12/8		NIC8/8	AM	NIC4/8	AR	NIC0/8	AC
P1A08	NC		NIC11/15	AF	NC		NIC3/15	AC
P1A09	NIC14/15		NIC10/15	AP	NC		NIC2/15	AR
P1A04	NIC13/15		NIC9/15	NC (BW)	NIC5/15	AR	NIC1/15	AT
P1A03	NIC12/15		NIC8/15	AL	NIC4/15	AR	NIC0/15	NC (BW)
P1A13	NC		NIC11/14	AF	NC		NIC3/14	AC
P1A14	NIC14/14		NIC10/14	AN	NC		NIC2/14	AR
P1B10	NIC13/14		NIC9/14	NC (BW)	NIC5/14	AR	NC	
P1B09	NIC12/14		NIC8/14	AL	NIC4/14	AR	NC	
P1A20	NC		NIC11/13	AF	NC		NIC3/13	AC
P1B21	NIC14/13		NIC10/13	AN	NC		NIC2/13	AR
P1A18	NIC13/13		NIC9/13	NC (BW)	NIC5/13	AR	NC	
P1B15	NIC12/13		NIC8/13	AL	NIC4/13	AR	NIC0/13	AB
P1B22	NC		NIC11/12	AF	NC		NIC3/12	AC
P1B19	NIC14/12		NIC10/12	AN	NIC6/12	AG	NIC2/12	AR
P1A17	NIC13/12		NIC9/12	NC (BW)	NIC5/12	AR	NC	
P1B16	NIC12/12	AF	NIC8/12	AL	NIC4/12	AR	NIC0/12	AK (BK)

NOTE: ALL SIGNALS POSITIVE (+) POLARITY.

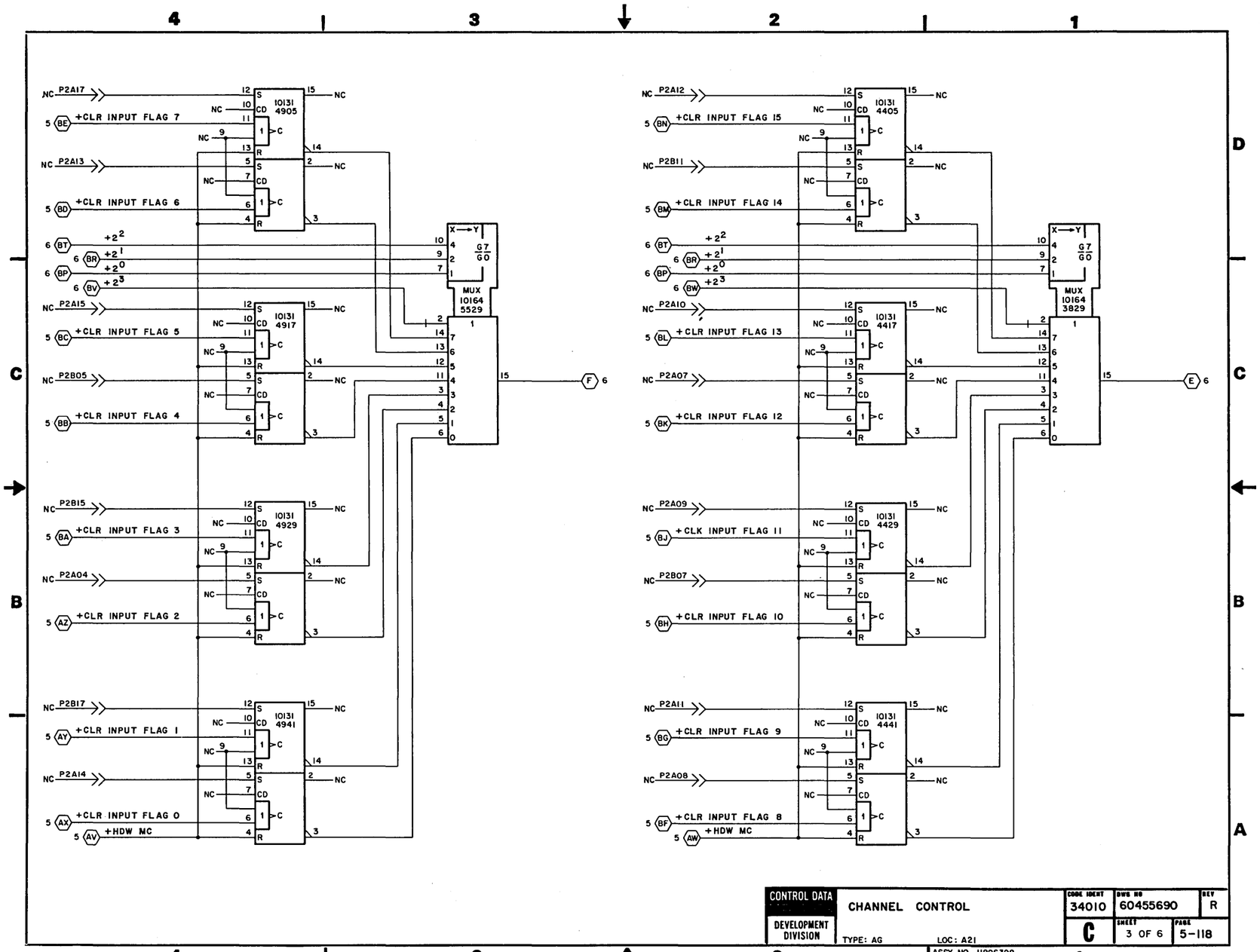

+DATA ECHO, + PORT SEL 2⁰-2¹
MUX 10164 2141
MUX 10164 3253
MUX 10164 1541
MUX 10164 2641
MUX 10164 0441
MUX 10164 1553
MUX 10164 3241
MUX 10164 1041
— BD SEL • D.B. IN/OUT
+NOCx/11
+NICx/11
+NICx/11 MUX
+NOCx/8
+NICx/8
+NICx/8 MUX
+NOCx/13
+NICx/13
+NICx/13 MUX
+NOCx/10
+NICx/10
+NICx/10 MUX
+NOCx/15
+NICx/15
+NICx/15 MUX
+NOCx/12
+NICx/12
+NICx/12 MUX
+NOCx/9
+NICx/9
+NICx/9 MUX
+NOCx/14
+NICx/14
+NICx/14 MUX
PIB28
PIB29
PIB24
PIA26
PIB41
PIB37
PIA34
PIA40
PIA20
PIB21
PIA18
PIB15
PIA32
PIA33
PIA30
PIA29
PIA08
PIA09
PIA04
PIA03
PIB22
PIB13
PIA17
PIB16
PIA41
PIB43
PIA36
PIA38
PIA13
PIA14
PIB10
PIB09
NOTES:
2 SEE TABLE
PROCESSOR CHANNELS
TYPE: AF
LOC: A17, A18, A19, A20
DEVELOPMENT DIVISION
ASSY. NO. 22934533
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
6 OF 6
PAGE 5-115



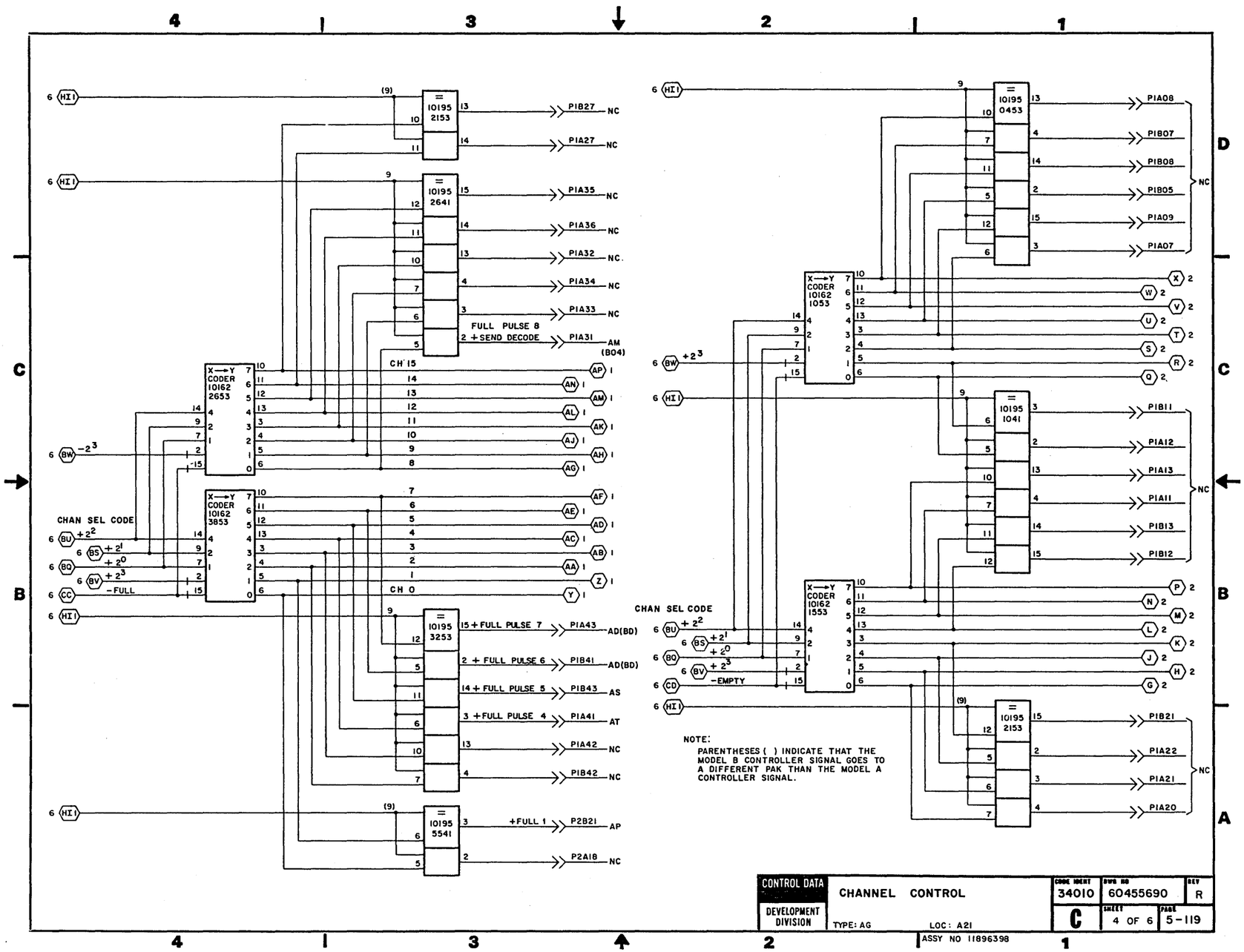
CONTROL DATA DEVELOPMENT DIVISION	CHANNEL CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AG LOC: A21 ASSY NO 11896398		C	SHEET 1 OF 6	PAGE 5-116



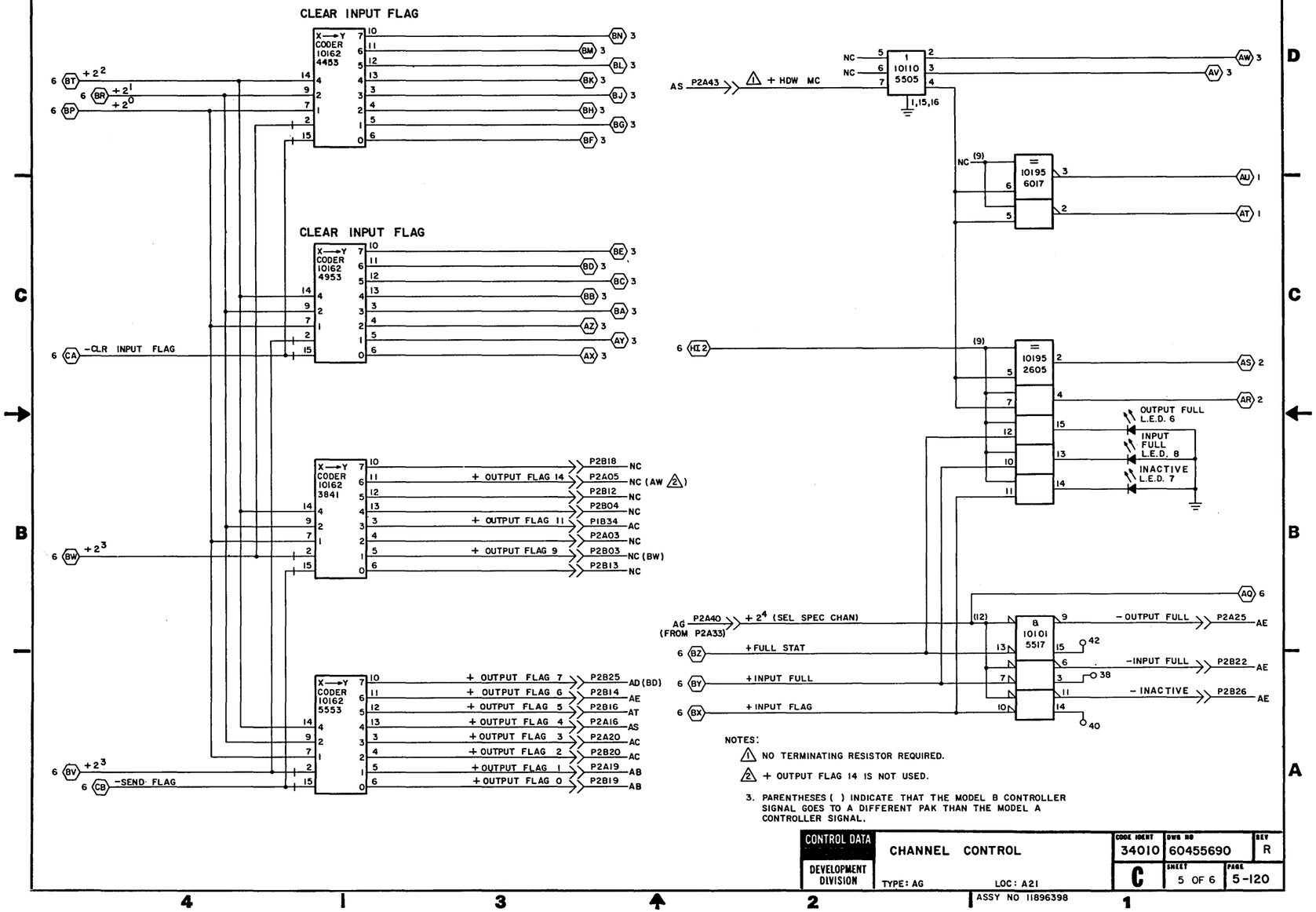
CONTROL DATA	CHANNEL CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AG LOC: A21 ASSY NO 11896398	SIZE C	SHEET 2 OF 6	PAGE 5-117



CONTROL DATA	CHANNEL CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AG LOC: A21 ASSY NO 11896398	C	SHEET 3 OF 6	PAGE 5-118



CONTROL DATA	CHANNEL CONTROL	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	TYPE: AG LOC: A21	34010	60455690	R
	ASSY NO 11896398	C	SHEET 4 OF 6	PAGE 5-119



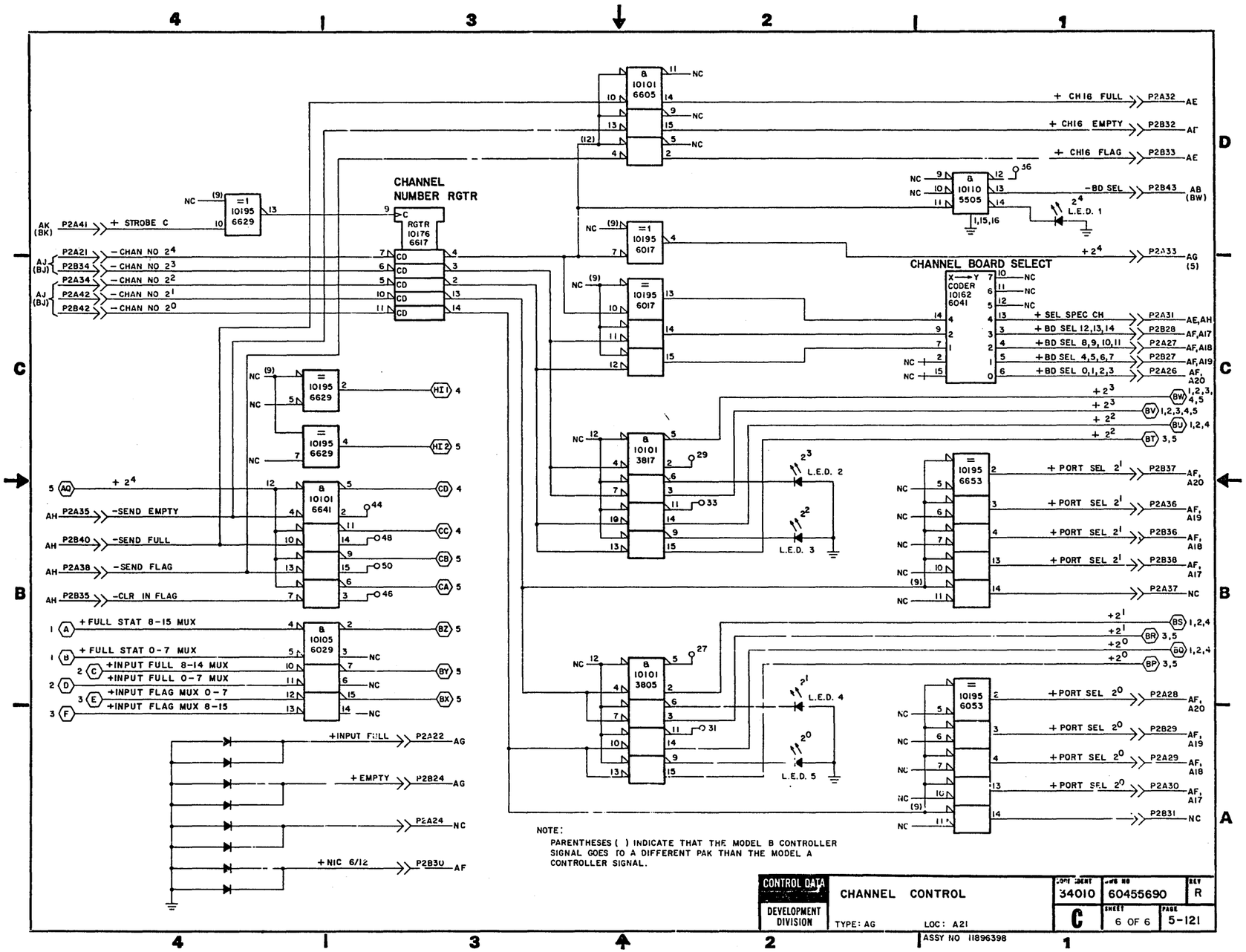
NOTES:

△1 NO TERMINATING RESISTOR REQUIRED.

△2 + OUTPUT FLAG 14 IS NOT USED.

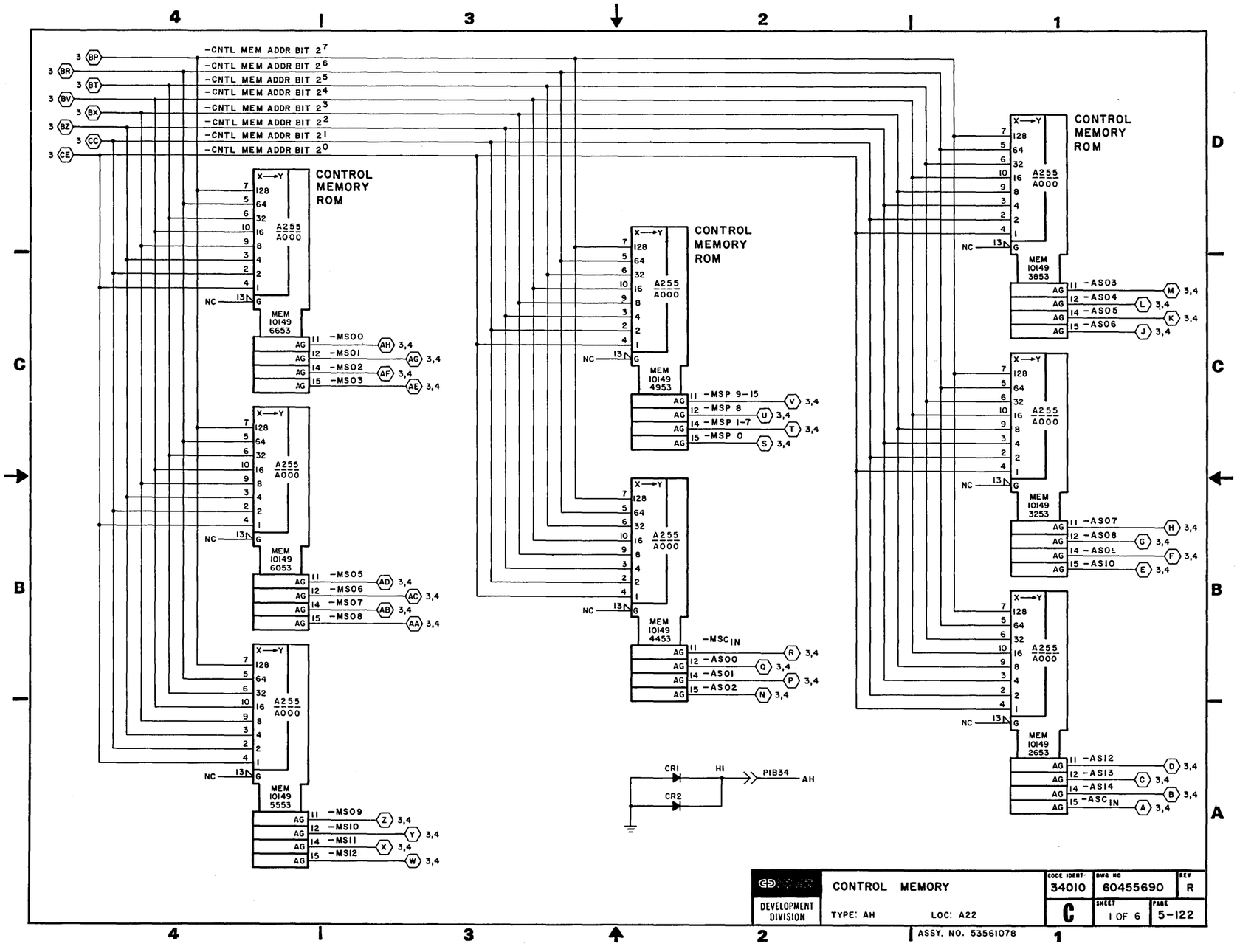
3. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

CONTROL DATA	CHANNEL CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AG LOC: A21 ASSY NO 11896398	C	SHEET 5 OF 6	PAGE 5-120

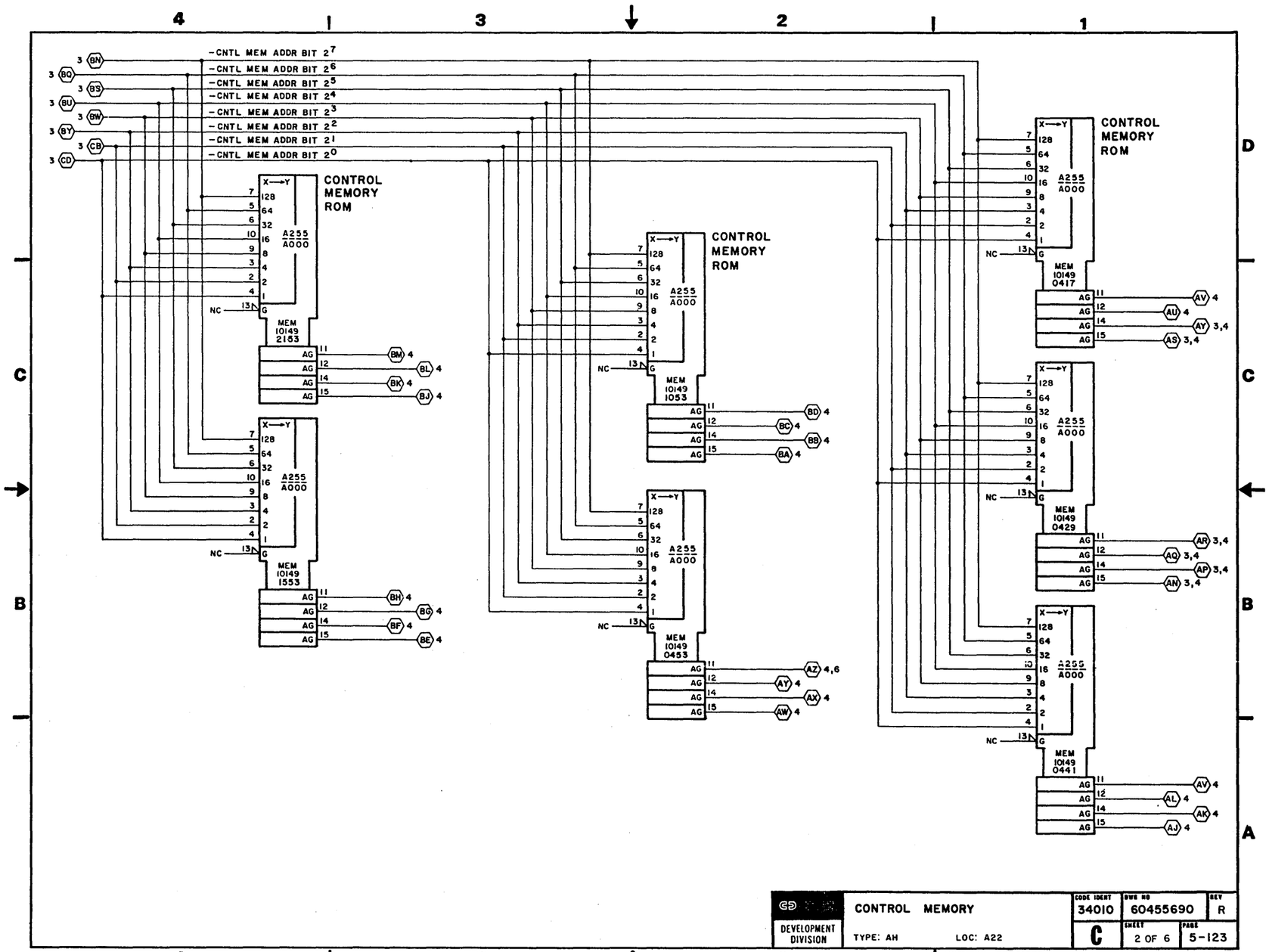

CHANNEL NUMBER RGTR
RGTR 10176 6617
CHANNEL BOARD SELECT
CODER 10162 6041
L.E.D. 1
L.E.D. 2
L.E.D. 3
L.E.D. 4
L.E.D. 5
AK (BK) P2A41 + STROBE C
P2A21 – CHAN NO 2^4
AJ (BJ) P2B34 – CHAN NO 2^3
P2A34 – CHAN NO 2^2
AJ (BJ) P2A42 – CHAN NO 2^1
P2B42 – CHAN NO 2^0
5 (AQ) + 2^4
AH P2A35 –SEND EMPTY
AH P2B40 –SEND FULL
AH P2A38 –SEND FLAG
AH P2B35 –CLR IN FLAG
1 (A) + FULL STAT 8-15 MUX
1 (B) + FULL STAT 0-7 MUX
2 (C) +INPUT FULL 8-14 MUX
2 (D) +INPUT FULL 0-7 MUX
3 (E) +INPUT FLAG MUX 0-7
3 (F) +INPUT FLAG MUX 8-15
+INPUT FULL P2A22 AG
+ EMPTY P2B24 AG
P2A24 NC
+NIC 6/12 P2B30 AF
+ CH16 FULL P2A32 AE
+ CH16 EMPTY P2B32 AF
+ CH16 FLAG P2B33 AE
-BD SEL P2B43 AB (BW)
+2^4 P2A33 AG (5)
+ SEL SPEC CH P2A31 AE,AH
+ BD SEL 12,13,14 P2B28 AF,A17
+BD SEL 8,9,10,11 P2A27 AF,A18
+BD SEL 4,5,6,7 P2B27 AF,A19
+BD SEL 0,1,2,3 P2A26 AF, A20
+2^3 (BW) 1,2,3,4,5
+2^3 (BV) 1,2,3,4,5
+2^2 (BU) 1,2,4
+2^2 (BT) 3,5
+PORT SEL 2^1 P2B37 AF, A20
+PORT SEL 2^1 P2A36 AF, A19
+PORT SEL 2^1 P2B36 AF, A18
+PORT SEL 2^1 P2B38 AF, A17
P2A37 NC
+2^1 (BS) 1,2,4
+2^1 (BR) 3,5
+2^0 (BQ) 1,2,4
+2^0 (BP) 3,5
+PORT SEL 2^0 P2A28 AF, A20
+PORT SEL 2^0 P2B29 AF, A19
+PORT SEL 2^0 P2A29 AF, A18
+PORT SEL 2^0 P2A30 AF, A17
P2B31 NC

NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

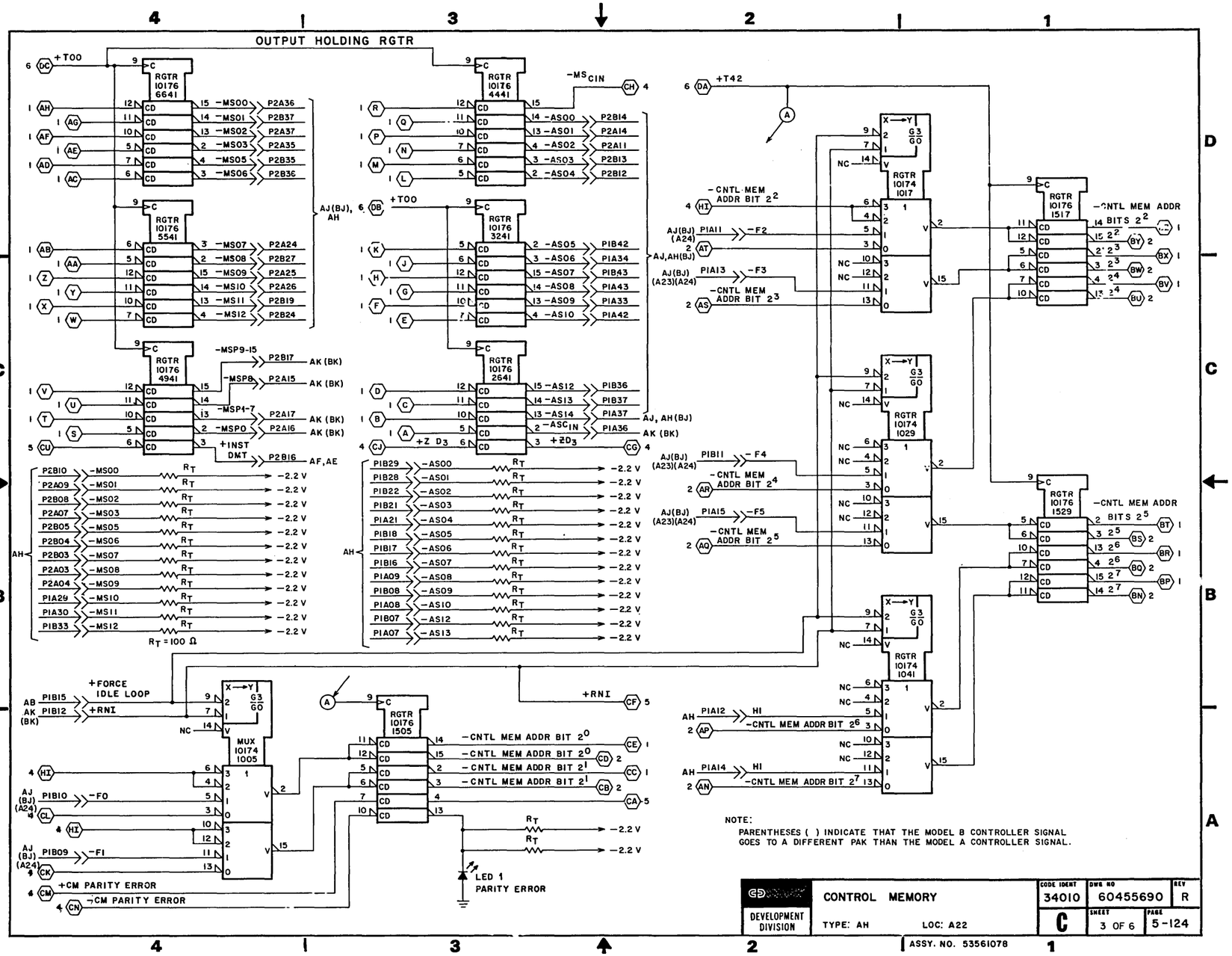
CONTROL DATA DEVELOPMENT DIVISION	CHANNEL CONTROL	DOCUMENT 34010	DWG NO 60455690	REV R
TYPE: AG LOC: A21 ASSY NO 11896398		SIZE C	SHEET 6 OF 6	PAGE 5-121

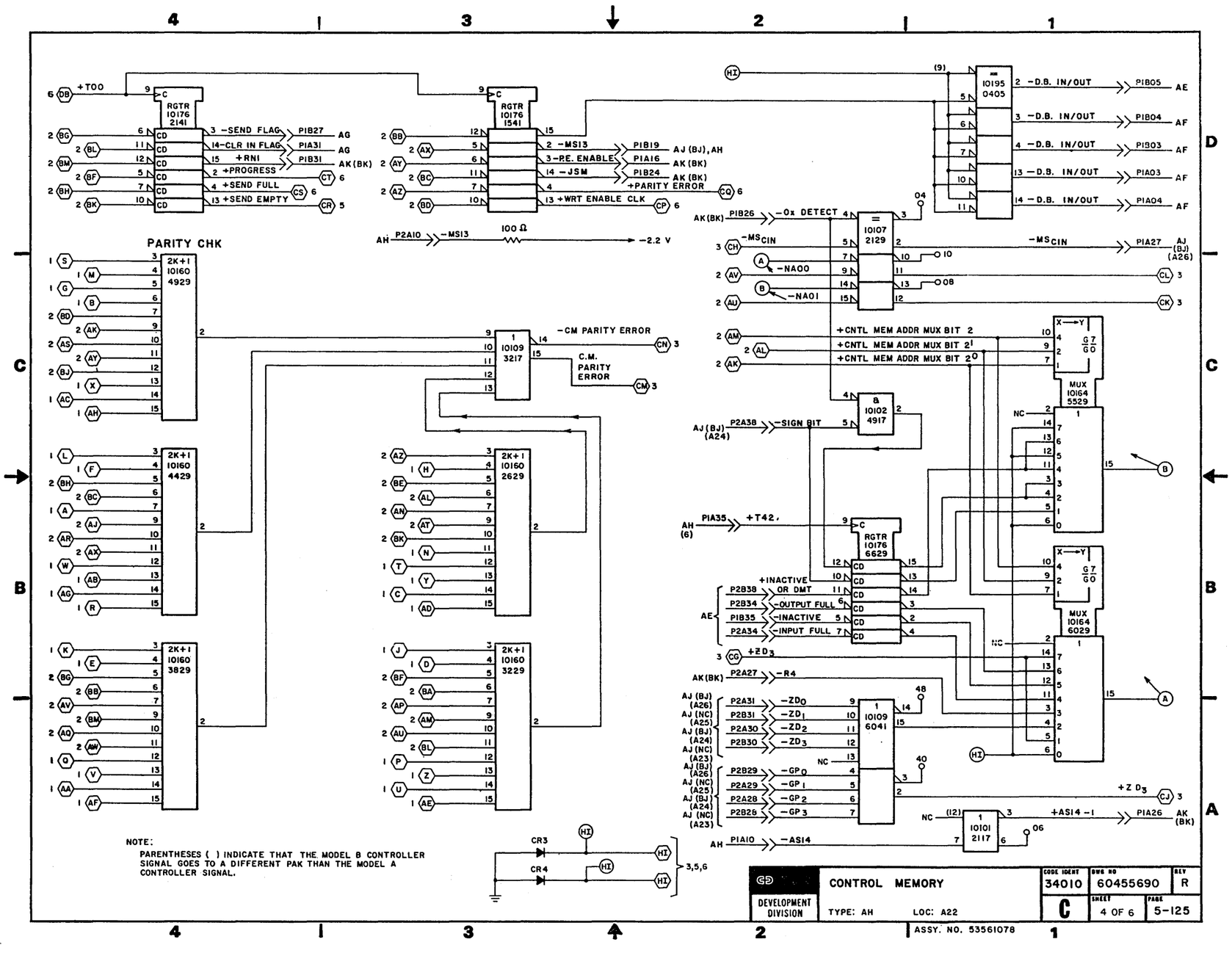


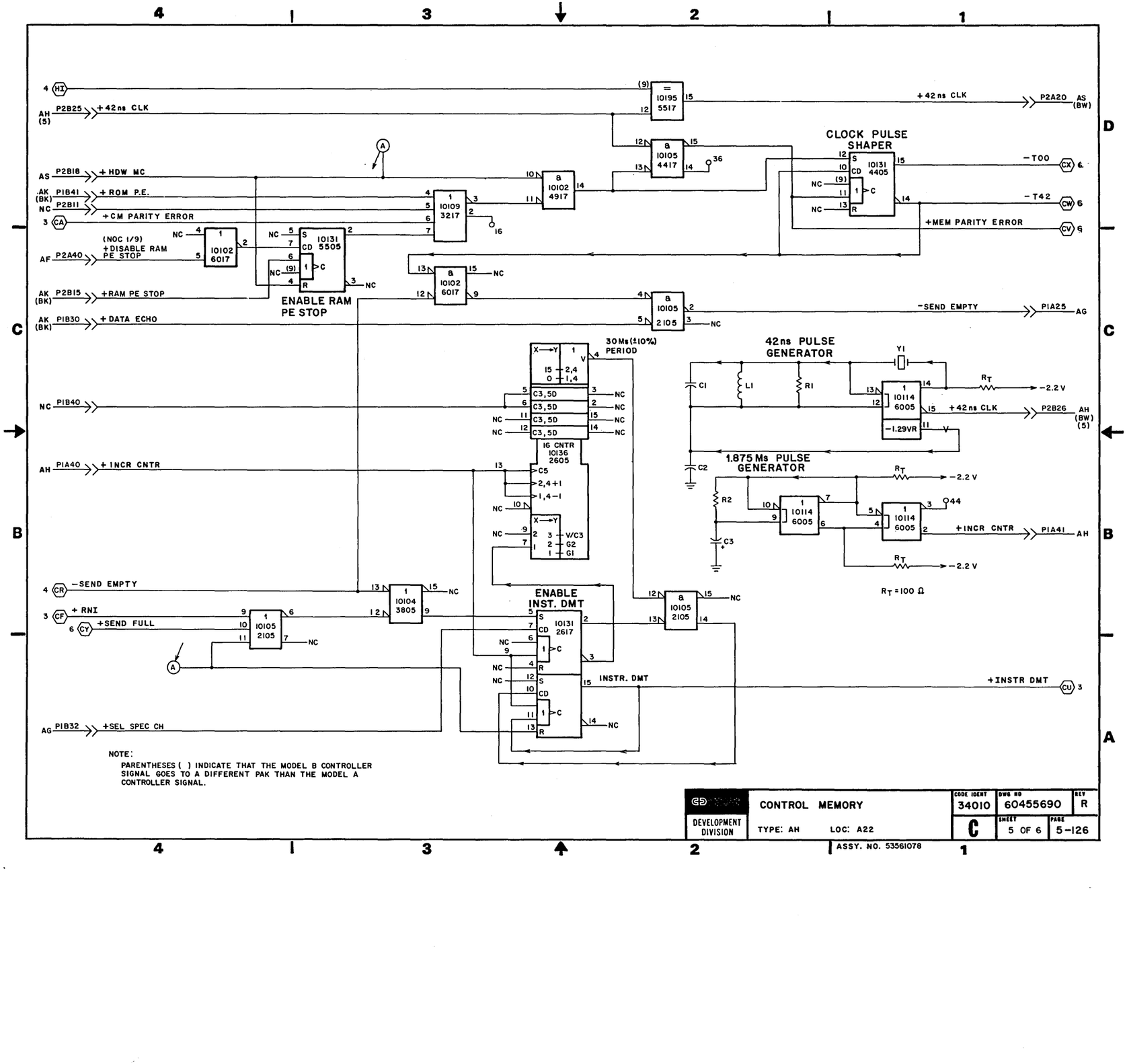
GD DEVELOPMENT DIVISION	CONTROL MEMORY	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AH LOC: A22 ASSY. NO. 53561078		C	SHEET 1 OF 6	PAGE 5-122

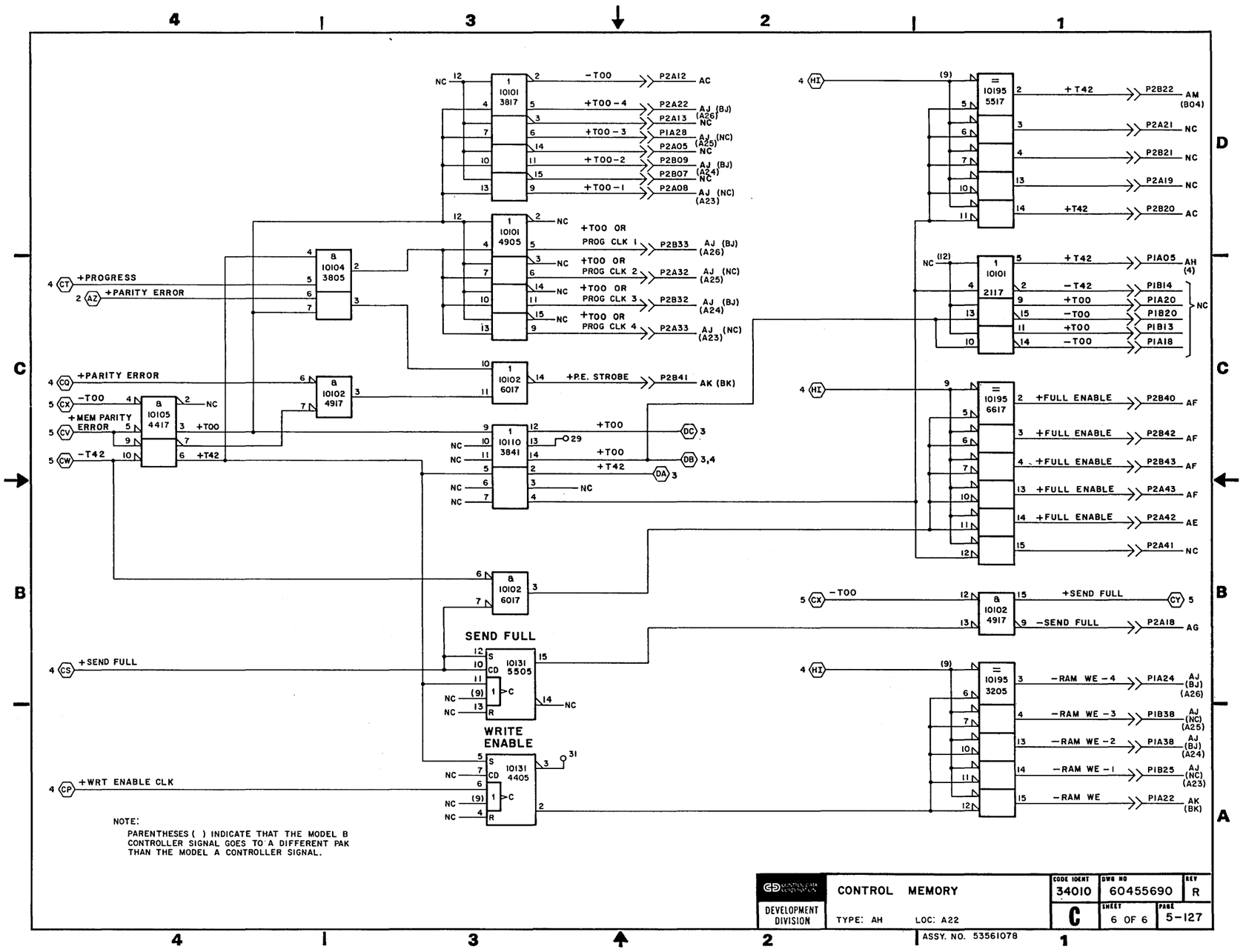


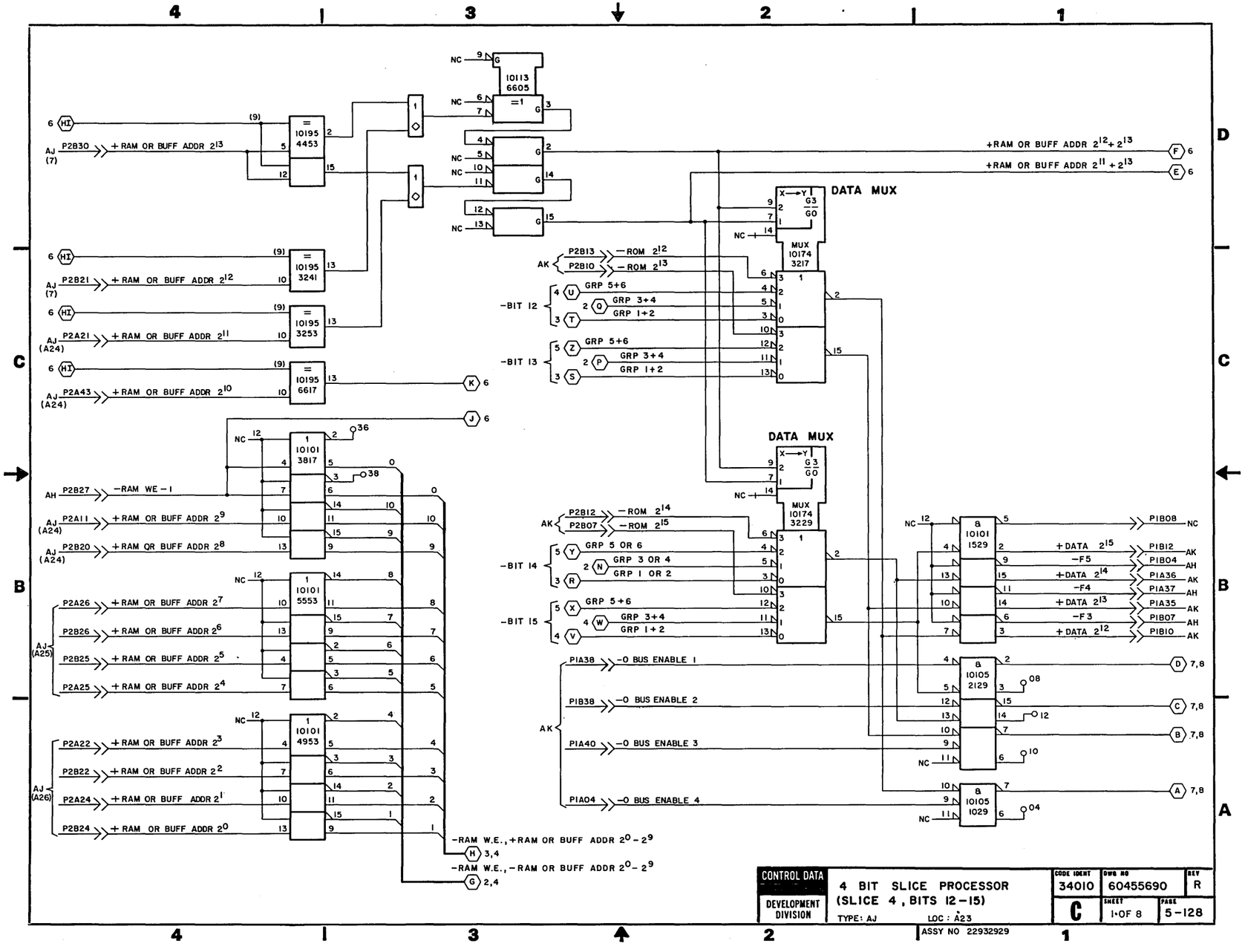
DEVELOPMENT DIVISION	CONTROL MEMORY	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AH LOC: A22	C	SHEET 2 OF 6	PAGE 5-123
	ASSY. NO. 53561078			

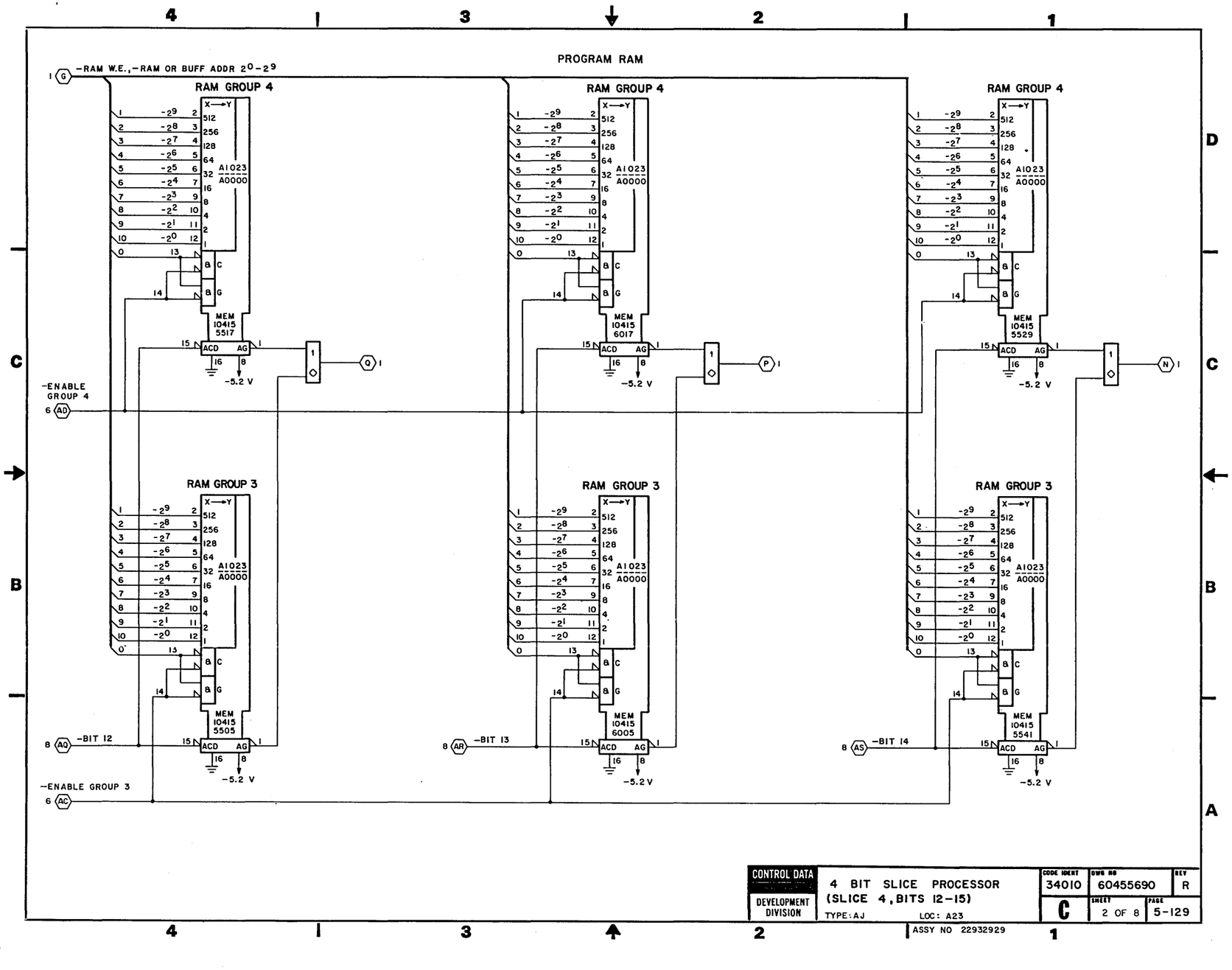

OUTPUT HOLDING RGTR
RGTR 10176 6641
RGTR 10176 5541
RGTR 10176 4941
RGTR 10176 4441
RGTR 10176 3241
RGTR 10176 2641
+T00
-MSCIN
+T42
AJ(BJ), AH
AJ, AH(BJ)
AK (BK)
AF, AE
+INST DMT
+Z D3
+2D3
RT = 100 Ω
-2.2 V
+FORCE IDLE LOOP
+RNI
MUX 10174 1005
-FO
-FI
+CM PARITY ERROR
¬CM PARITY ERROR
LED 1 PARITY ERROR
-CNTL MEM ADDR BIT 2^0
-CNTL MEM ADDR BIT 2^1
-CNTL MEM ADDR BIT 2^2
-CNTL MEM ADDR BIT 2^3
-CNTL MEM ADDR BIT 2^4
-CNTL MEM ADDR BIT 2^5
-CNTL MEM ADDR BIT 2^6
-CNTL MEM ADDR BIT 2^7
RGTR 10174 1017
RGTR 10174 1029
RGTR 10174 1041
RGTR 10176 1517
RGTR 10176 1529
RGTR 10176 1505
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL MEMORY
TYPE: AH
LOC: A22
ASSY. NO. 53561078
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 6
PAGE 5-124

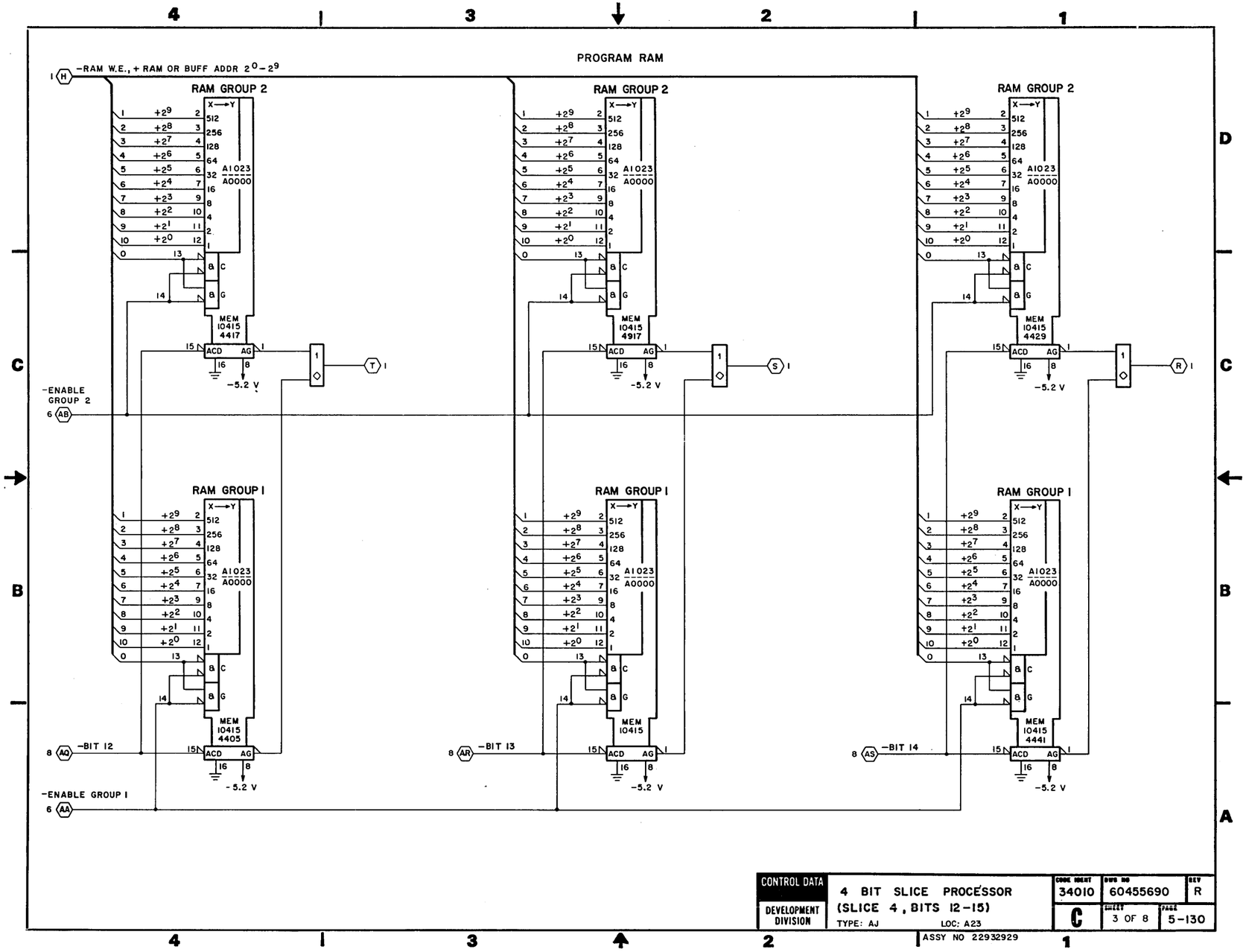

4
3
2
1
D
C
B
A
RGTR 10176 2141
RGTR 10176 1541
RGTR 10176 6629
10195 0405
10107 2129
10109 3217
10109 6041
10102 4917
10101 2117
MUX 10164 5529
MUX 10164 6029
G7 G0
2K+1 10160 4929
2K+1 10160 4429
2K+1 10160 2629
2K+1 10160 3829
2K+1 10160 3229
PARITY CHK
+T00
-SEND FLAG
-CLR IN FLAG
+RNI
+PROGRESS
+SEND FULL
+SEND EMPTY
-MSI3
-RE. ENABLE
-JSM
+PARITY ERROR
+WRT ENABLE CLK
100 Ω
-2.2 V
-D.B. IN/OUT
-Ox DETECT
-MSCIN
-NA00
-NA01
+CNTL MEM ADDR MUX BIT 2
+CNTL MEM ADDR MUX BIT 2¹
+CNTL MEM ADDR MUX BIT 2⁰
-CM PARITY ERROR
C.M. PARITY ERROR
-SIGN BIT
+T42,
+INACTIVE OR DMT
-OUTPUT FULL
-INACTIVE
-INPUT FULL
+ZD3
-R4
-ZD0
-ZD1
-ZD2
-ZD3
-GP0
-GP1
-GP2
-GP3
+ASI4-1
-ASI4
CR3
CR4
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL MEMORY
TYPE: AH LOC: A22
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
4 OF 6
PAGE 5-125
ASSY. NO. 53561078

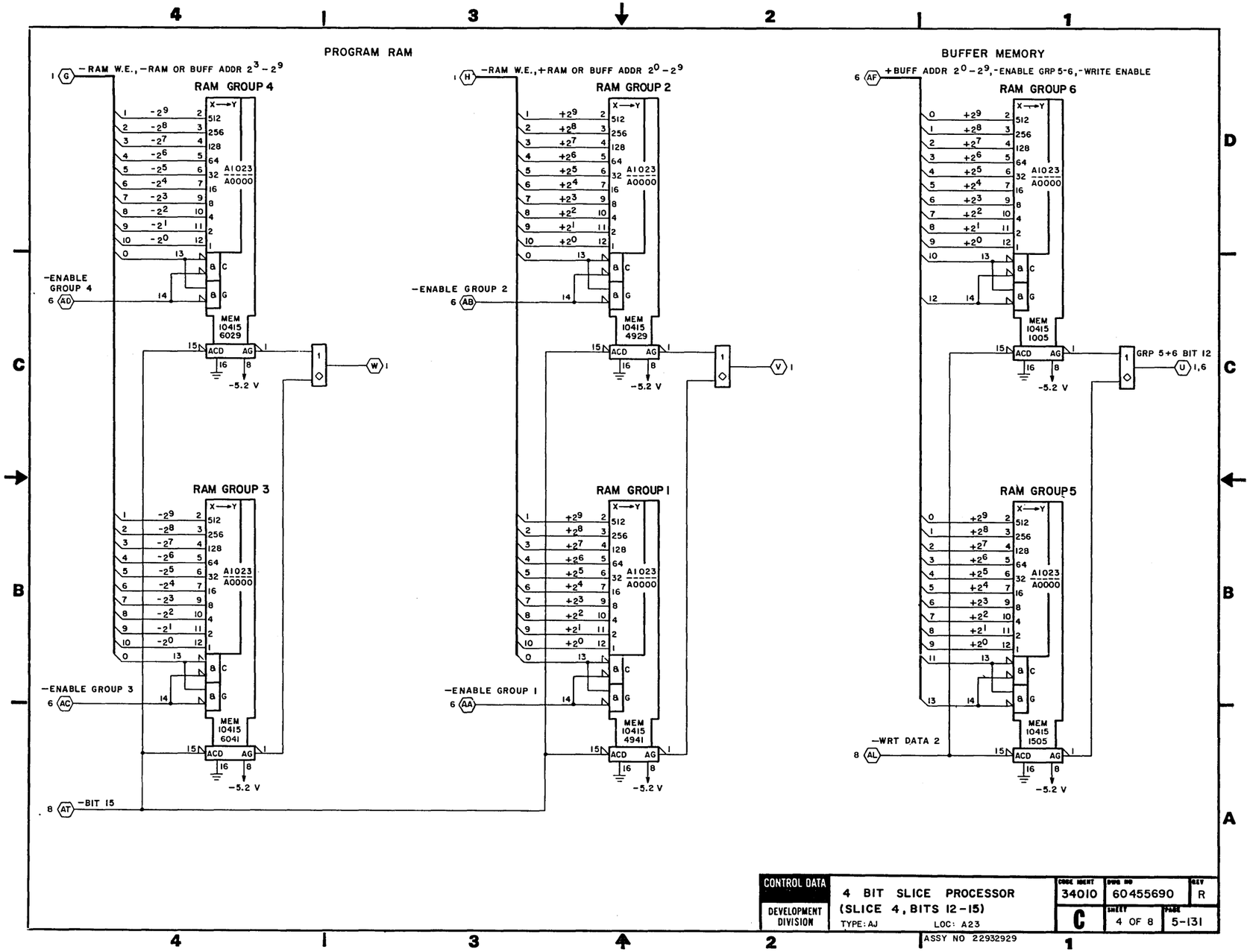

4 (HI)
AH (5) P2B25 +42ns CLK
AS P2B18 +HDW MC
AK (BK) P1B41 +ROM P.E.
NC P2B11
3 (CA) +CM PARITY ERROR
(NOC 1/9) +DISABLE RAM PE STOP
AF P2A40
AK (BK) P2B15 +RAM PE STOP
AK (BK) P1B30 +DATA ECHO
ENABLE RAM PE STOP
CLOCK PULSE SHAPER
+42ns CLK
P2A20 AS (BW)
-T00 (CX) 6
-T42 (CW) 6
+MEM PARITY ERROR (CV) 6
-SEND EMPTY
P1A25 AG
30Ms(±10%) PERIOD
42ns PULSE GENERATOR
C1
L1
R1
Y1
RT
-2.2 V
-1.29VR
+42ns CLK
P2B26 AH (BW) (5)
1.875Ms PULSE GENERATOR
C2
R2
C3
+INCR CNTR
P1A41 AH
RT = 100 Ω
NC P1B40
AH P1A40 +INCR CNTR
16 CNTR 10136 2605
C5
2,4+1
1,4-1
ENABLE INST. DMT
INSTR. DMT
+INSTR DMT (CU) 3
4 (CR) -SEND EMPTY
3 (CF) +RNI
6 (CY) +SEND FULL
AG P1B32 +SEL SPEC CH
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL MEMORY
TYPE: AH LOC: A22
ASSY. NO. 53561078
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 5 OF 6
PAGE 5-126
DEVELOPMENT DIVISION


4
3
2
1
D
C
B
A
1 10101 3817
-T00
P2A12 AC
+T00-4
P2A22 AJ (BJ)
P2A13 (A26) NC
+T00-3
P1A28 AJ (NC)
P2A05 (A25) NC
+T00-2
P2B09 AJ (BJ)
P2B07 (A24) NC
+T00-1
P2A08 AJ (NC) (A23)
1 10101 4905
+T00 OR PROG CLK 1
P2B33 AJ (BJ) (A26)
+T00 OR PROG CLK 2
P2A32 AJ (NC) (A25)
+T00 OR PROG CLK 3
P2B32 AJ (BJ) (A24)
+T00 OR PROG CLK 4
P2A33 AJ (NC) (A23)
1 10102 6017
+P.E. STROBE
P2B41 AK (BK)
1 10110 3841
+T00
DC 3
+T00
DB 3,4
+T42
DA 3
NC
8 10104 3805
+PROGRESS
+PARITY ERROR
8 10102 4917
8 10105 4417
+MEM PARITY ERROR
-T00
-T42
+T00
+T42
8 10102 6017
SEND FULL
+SEND FULL
10131 5505
WRITE ENABLE
+WRT ENABLE CLK
10131 4405
= 10195 5517
+T42
P2B22 AM (B04)
P2A21 NC
P2B21 NC
P2A19 NC
+T42
P2B20 AC
1 10101 2117
+T42
P1A05 AH (4)
-T42
P1B14
+T00
P1A20
-T00
P1B20
+T00
P1B13
-T00
P1A18
NC
= 10195 6617
+FULL ENABLE
P2B40 AF
P2B42 AF
P2B43 AF
P2A43 AF
P2A42 AE
P2A41 NC
8 10102 4917
-T00
+SEND FULL
CY 5
-SEND FULL
P2A18 AG
= 10195 3205
-RAM WE -4
P1A24 AJ (BJ) (A26)
-RAM WE -3
P1B38 AJ (NC) (A25)
-RAM WE -2
P1A38 AJ (BJ) (A24)
-RAM WE -1
P1B25 AJ (NC) (A23)
-RAM WE
P1A22 AK (BK)
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
CONTROL MEMORY
TYPE: AH LOC: A22
ASSY. NO. 53561078
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 6 OF 6
PAGE 5-127


4
3
2
1
D
C
B
A
6 HI
AJ (7) P2B30 + RAM OR BUFF ADDR 2^13
AJ (7) P2B21 + RAM OR BUFF ADDR 2^12
AJ (A24) P2A21 + RAM OR BUFF ADDR 2^11
AJ (A24) P2A43 + RAM OR BUFF ADDR 2^10
10195 4453
10195 3241
10195 3253
10195 6617
10113 6605 =1
K 6
J 6
AH P2B27 −RAM WE − 1
AJ (A24) P2A11 + RAM OR BUFF ADDR 2^9
AJ (A24) P2B20 + RAM OR BUFF ADDR 2^8
10101 3817
AJ (A25) P2A26 + RAM OR BUFF ADDR 2^7
P2B26 + RAM OR BUFF ADDR 2^6
P2B25 + RAM OR BUFF ADDR 2^5
P2A25 + RAM OR BUFF ADDR 2^4
10101 5553
AJ (A26) P2A22 + RAM OR BUFF ADDR 2^3
P2B22 + RAM OR BUFF ADDR 2^2
P2A24 + RAM OR BUFF ADDR 2^1
P2B24 + RAM OR BUFF ADDR 2^0
10101 4953
−RAM W.E., +RAM OR BUFF ADDR 2^0 − 2^9
H 3,4
−RAM W.E., −RAM OR BUFF ADDR 2^0 − 2^9
G 2,4
+RAM OR BUFF ADDR 2^12 + 2^13
+RAM OR BUFF ADDR 2^11 + 2^13
F 6
E 6
DATA MUX
MUX 10174 3217
AK P2B13 −ROM 2^12
P2B10 −ROM 2^13
−BIT 12 GRP 5+6 GRP 3+4 GRP 1+2
−BIT 13 GRP 5+6 GRP 3+4 GRP 1+2
DATA MUX
MUX 10174 3229
AK P2B12 −ROM 2^14
P2B07 −ROM 2^15
−BIT 14 GRP 5 OR 6 GRP 3 OR 4 GRP 1 OR 2
−BIT 15 GRP 5+6 GRP 3+4 GRP 1+2
10101 1529
P1B08 NC
+DATA 2^15 −F5 P1B12 AK P1B04 AH
+DATA 2^14 −F4 P1A36 AK P1A37 AH
+DATA 2^13 −F3 P1A35 AK P1B07 AH
+DATA 2^12 P1B10 AK
PIA38 −O BUS ENABLE 1
PIB38 −O BUS ENABLE 2
PIA40 −O BUS ENABLE 3
PIA04 −O BUS ENABLE 4
AK
10105 2129
10105 1029
D 7,8
C 7,8
B 7,8
A 7,8
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 4, BITS 12−15)
TYPE: AJ
LOC: A23
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 1 OF 8
PAGE 5-128


PROGRAM RAM
-RAM W.E., -RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 4
RAM GROUP 4
RAM GROUP 4
A1023
A0000
MEM
10415
5517
MEM
10415
6017
MEM
10415
5529
-5.2 V
-ENABLE
GROUP 4
RAM GROUP 3
RAM GROUP 3
RAM GROUP 3
MEM
10415
5505
MEM
10415
6005
MEM
10415
5541
-BIT 12
-BIT 13
-BIT 14
-ENABLE GROUP 3
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 4, BITS 12-15)
TYPE: AJ
LOC: A23
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 8
PAGE 5-129


PROGRAM RAM
-RAM W.E., + RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 2
RAM GROUP 1
A1023
A0000
MEM 10415 4417
MEM 10415 4917
MEM 10415 4429
MEM 10415 4405
MEM 10415
MEM 10415 4441
-5.2 V
-ENABLE GROUP 2
-ENABLE GROUP 1
-BIT 12
-BIT 13
-BIT 14
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 4, BITS 12-15)
TYPE: AJ
LOC: A23
ASSY NO 22932929
34010
60455690
R
C
3 OF 8
5-130



CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 4, BITS 12-15)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A23 ASSY NO 22932929	SIZE C	SHEET 4 OF 8	PAGE 5-131

BUFFER MEMORY

G (AF) +BUFF ADDR 2^0-2^9, -ENABLE GRP 5-6, -WRITE ENABLE

RAM GROUP 6

A1023 A0000

MEM 10415 1017

ACD AG

-5.2 V

GRP 5+6 BIT 13 (Z) 1,6

RAM GROUP 5

A1023 A0000

-WRT DATA 13 8 (AM)

MEM 10415 1517

ACD AG

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2105

ACD AG

-5.2 V

GRP 5+6 BIT 14 (Y) 1,6

RAM GROUP 5

A1023 A0000

-WRT DATA 14 8 (AN)

MEM 10415 2605

ACD AG

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2117

ACD AG

-5.2 V

GRP 5+6 BITS 15 (X) 1,6

RAM GROUP 5

A1023 A0000

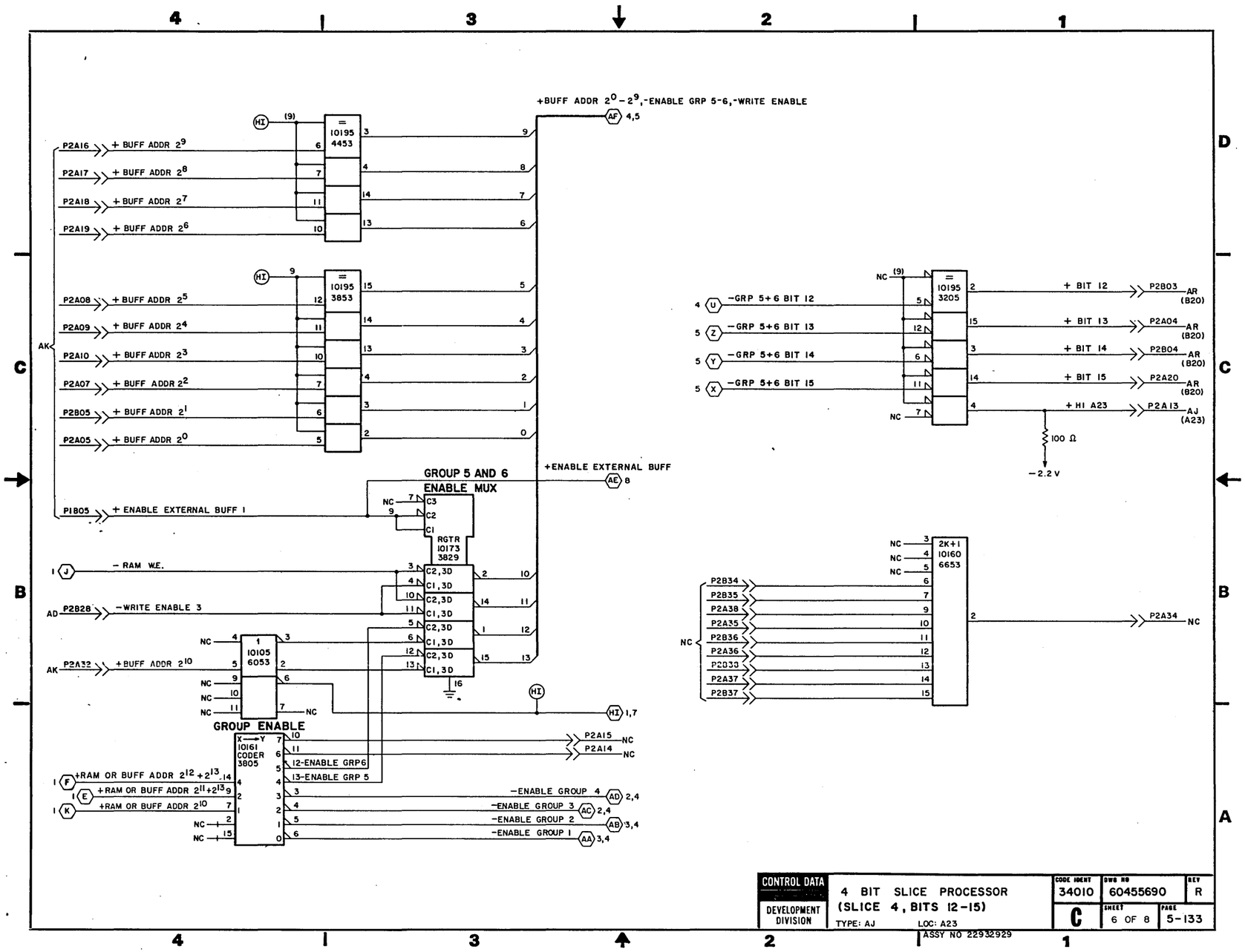
-WRT DATA 15 8 (AP)

MEM 10415 2617

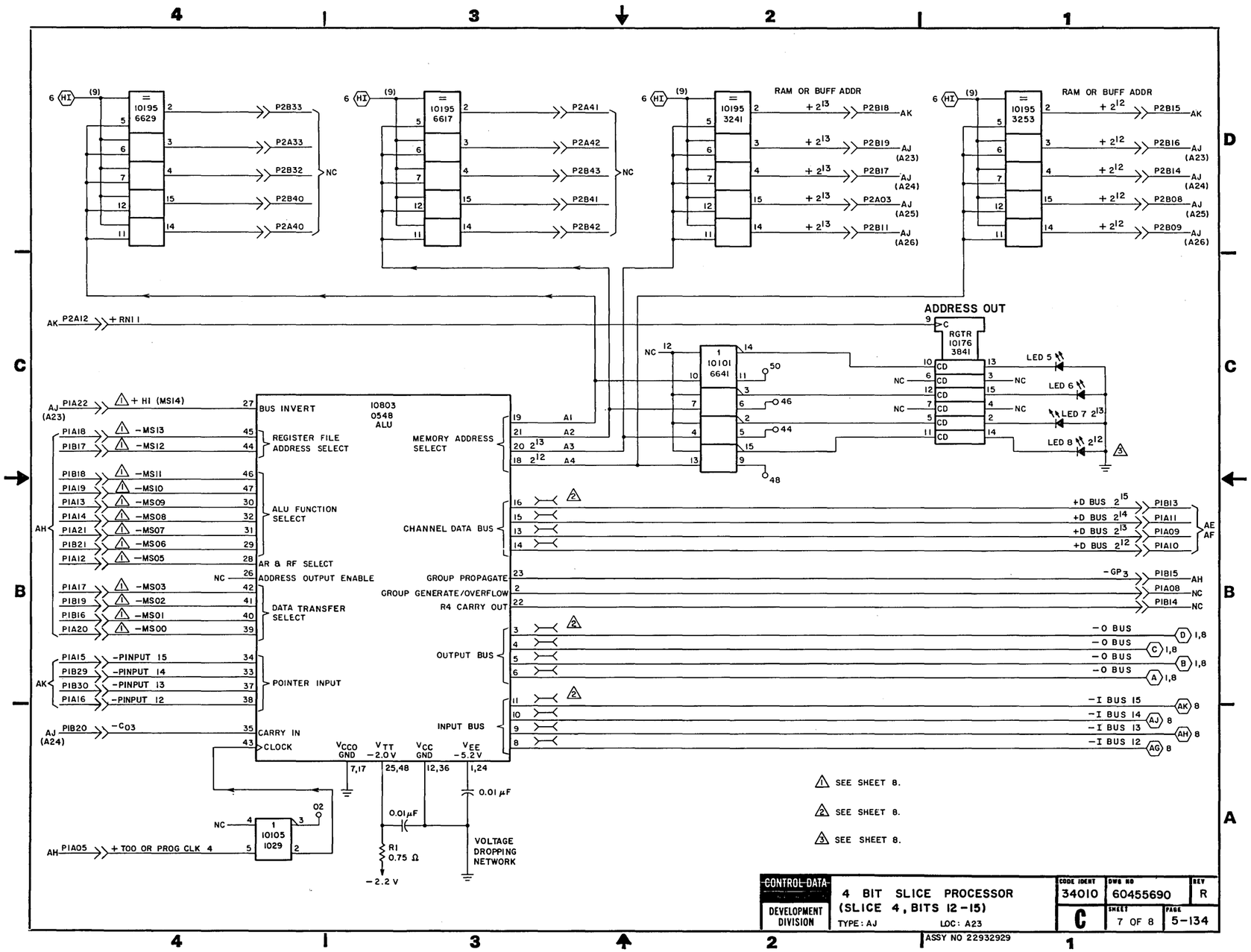
ACD AG

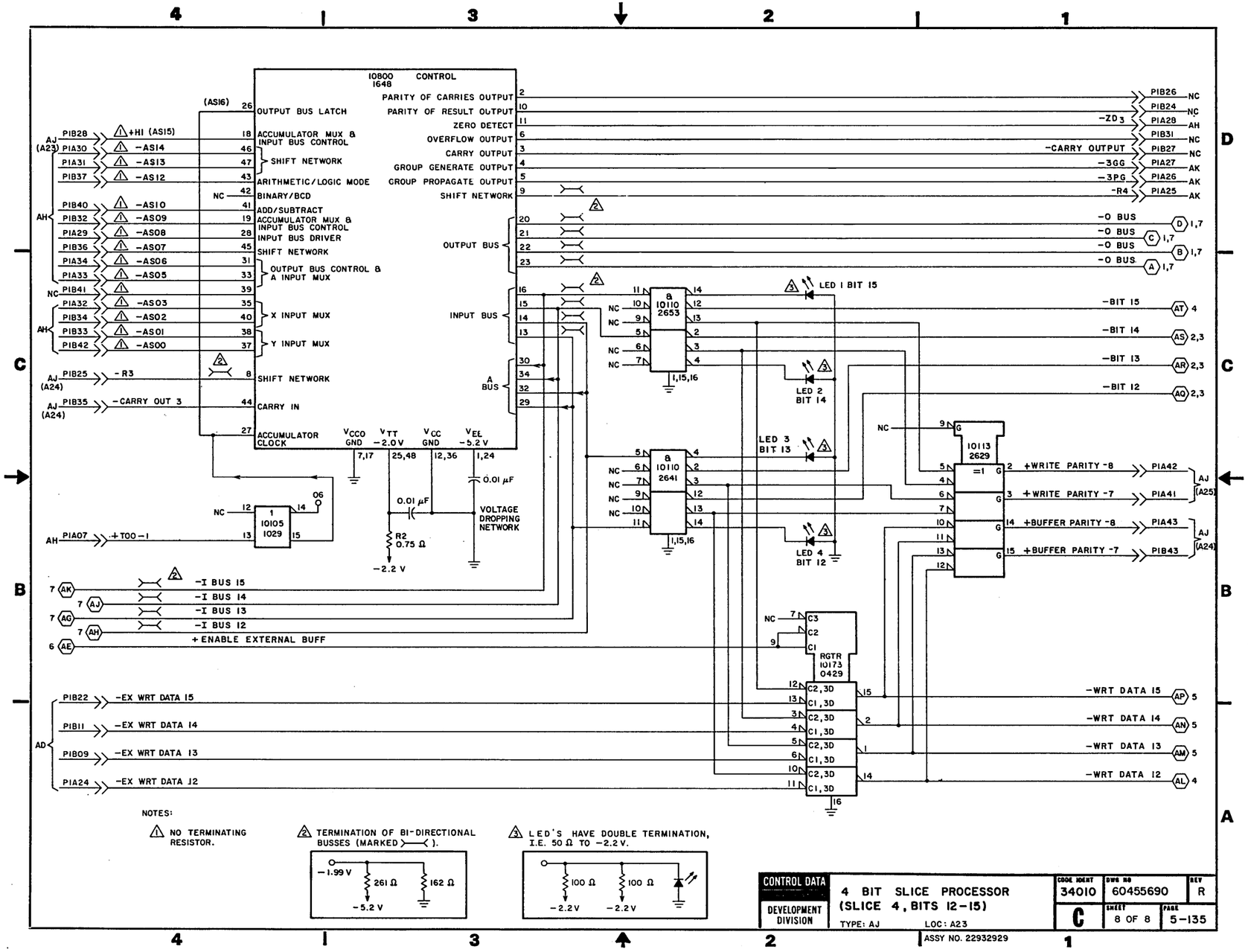
-5.2 V

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 4, BITS 12-15)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A23 ASSY NO 22932929	C	SHEET 5 OF 8	PAGE 5-132



CONTROL DATA DEVELOPMENT DIVISION	4 BIT SLICE PROCESSOR (SLICE 4, BITS 12-15) TYPE: AJ LOC: A23 ASSY NO 22932929	CODE IDENT 34010	DWG NO 60455690	REV R
		SIZE C	SHEET 6 OF 8	PAGE 5-133

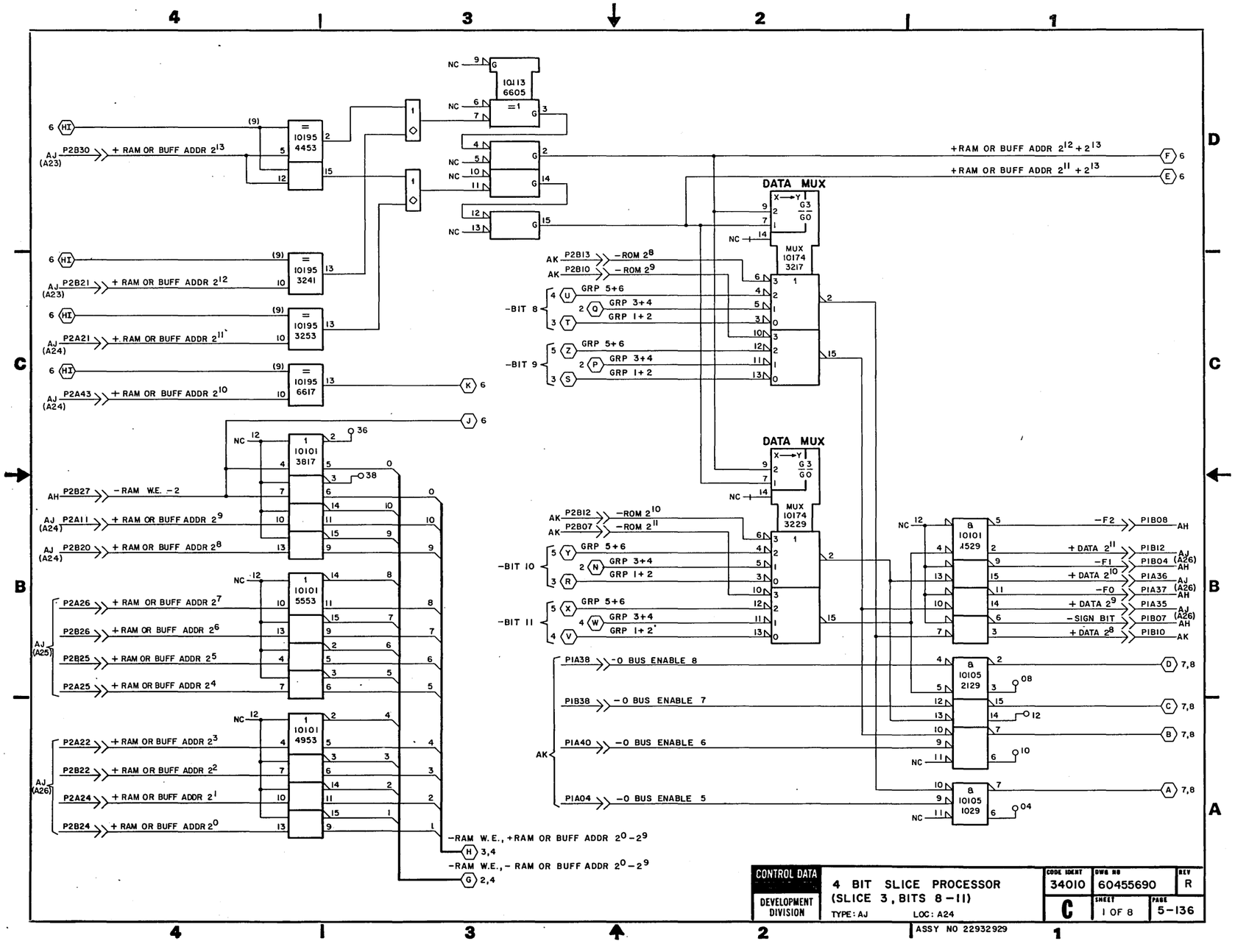

4
3
2
1
6 HI (9)
10195 6629
P2B33
P2A33
P2B32
P2B40
P2A40
NC
10195 6617
P2A41
P2A42
P2B43
P2B41
P2B42
RAM OR BUFF ADDR
10195 3241
+ 2^13
P2B18 AK
P2B19 AJ (A23)
P2B17 AJ (A24)
P2A03 AJ (A25)
P2B11 AJ (A26)
10195 3253
+ 2^12
P2B15 AK
P2B16 AJ (A23)
P2B14 AJ (A24)
P2B08 AJ (A25)
P2B09 AJ (A26)
ADDRESS OUT
RGTR 10176 3841
LED 5
LED 6
LED 7 2^13
LED 8 2^12
1 10101 6641
AK P2A12 + RN11
AJ (A23) PIA22 + HI (MSI4)
10803 0548 ALU
BUS INVERT
REGISTER FILE ADDRESS SELECT
ALU FUNCTION SELECT
AR & RF SELECT
ADDRESS OUTPUT ENABLE
DATA TRANSFER SELECT
POINTER INPUT
CARRY IN
CLOCK
MEMORY ADDRESS SELECT
CHANNEL DATA BUS
GROUP PROPAGATE
GROUP GENERATE/OVERFLOW
R4 CARRY OUT
OUTPUT BUS
INPUT BUS
+D BUS 2^15
+D BUS 2^14
+D BUS 2^13
+D BUS 2^12
-GP3
-O BUS
-I BUS 15
-I BUS 14
-I BUS 13
-I BUS 12
VCCO GND 7,17
VTT -2.0 V 25,48
VCC GND 12,36
VEE -5.2 V 1,24
0.01 µF
RI 0.75 Ω
-2.2 V
VOLTAGE DROPPING NETWORK
1 10105 1029
AH PIA05 + TOO OR PROG CLK 4
SEE SHEET 8.
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR (SLICE 4, BITS 12-15)
TYPE: AJ
LOC: A23
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
7 OF 8
PAGE 5-134

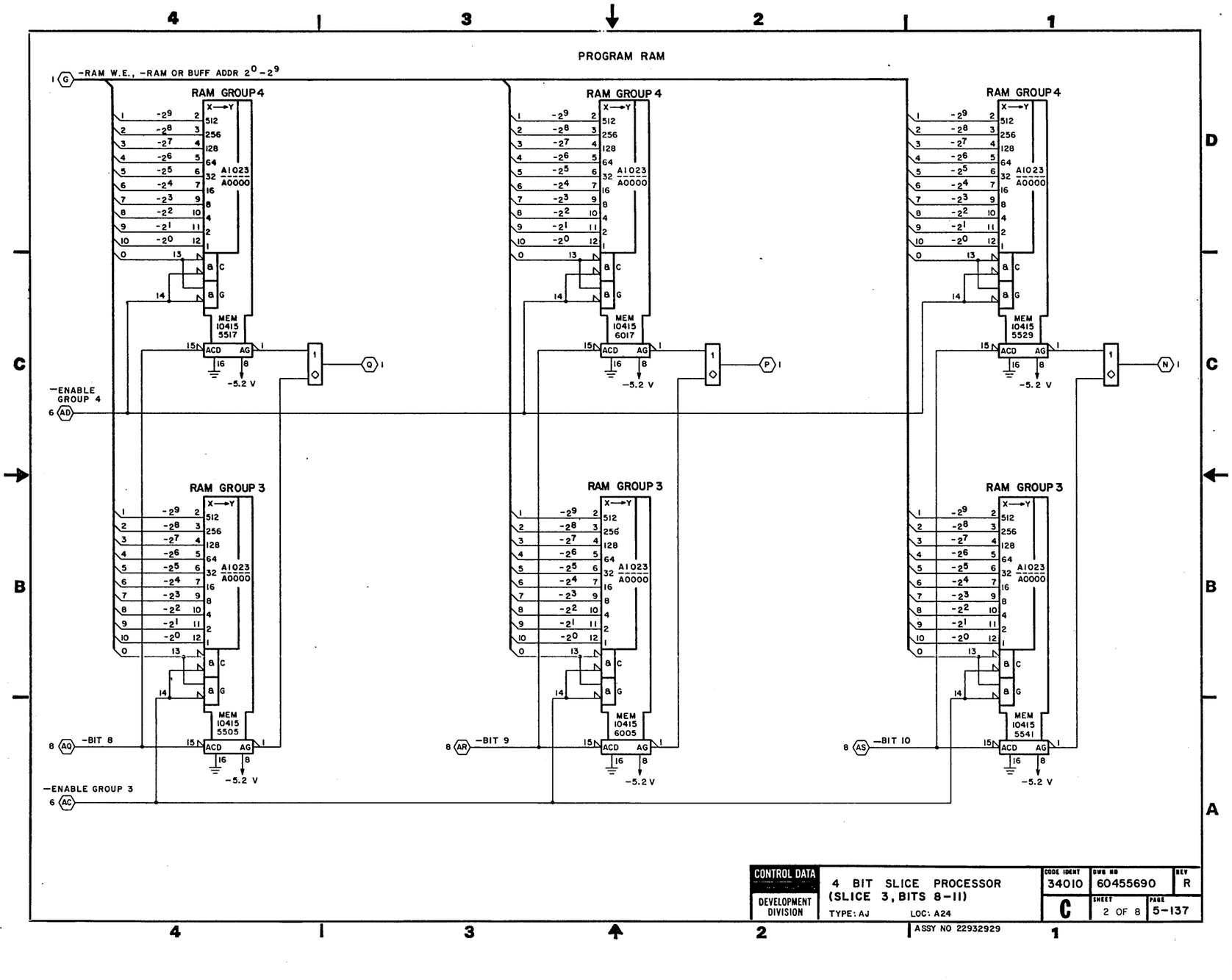


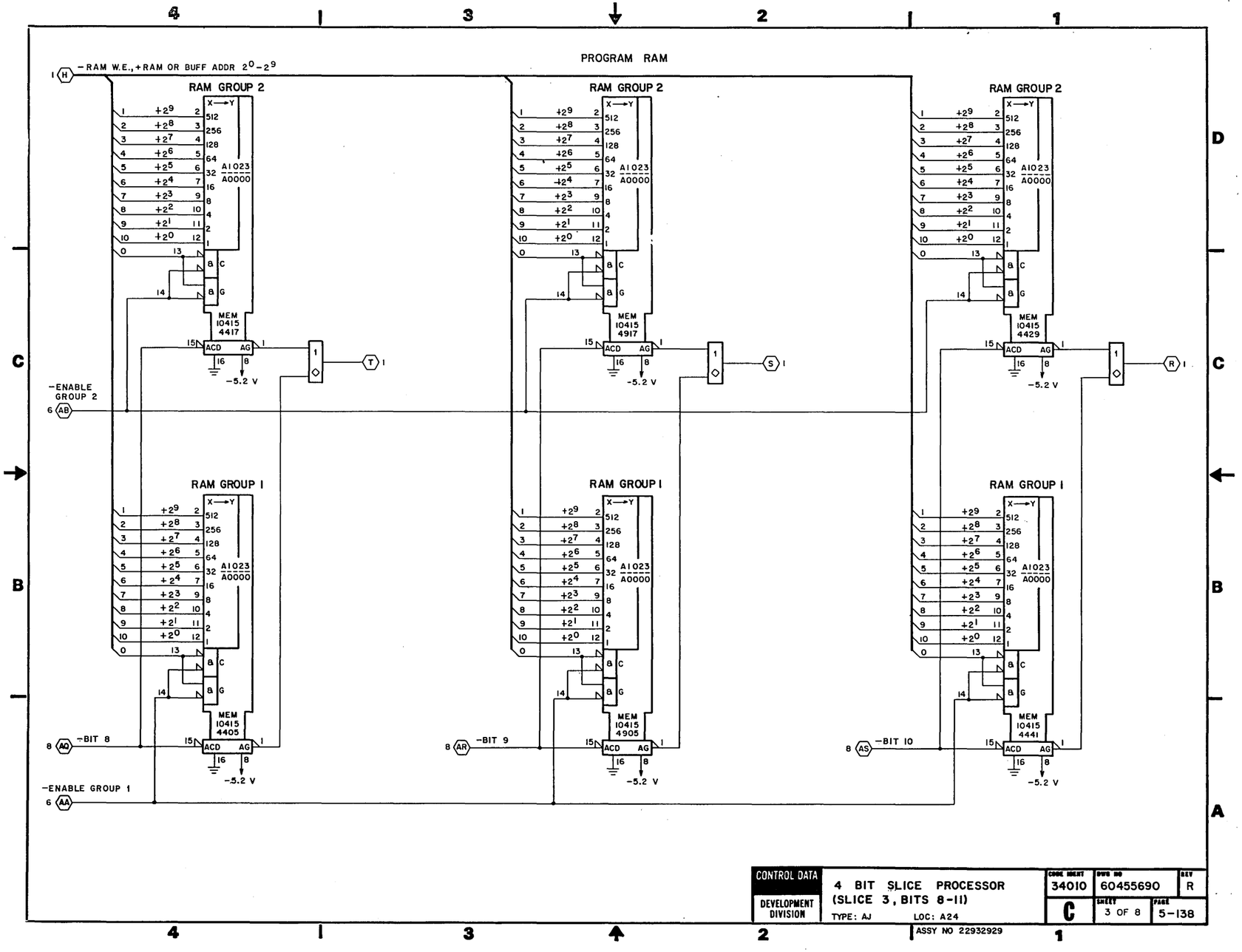
NOTES:

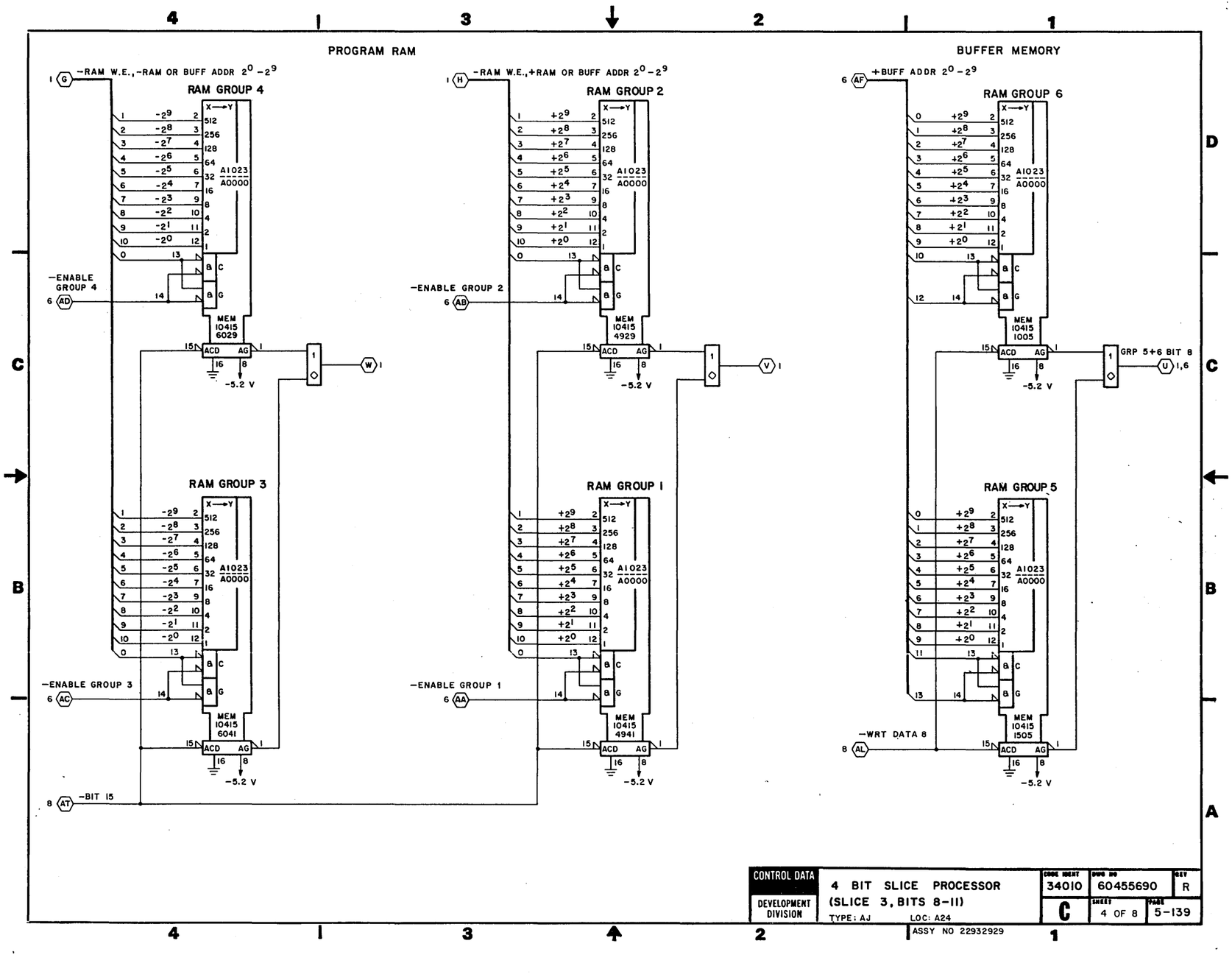
1. NO TERMINATING RESISTOR.
2. TERMINATION OF BI-DIRECTIONAL BUSSES (MARKED >—<).
3. LED'S HAVE DOUBLE TERMINATION, I.E. 50 Ω TO −2.2 V.

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 4, BITS 12-15)	CODE IDENT 34010	DWG NO 60455690 REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A23	SIZE C	SHEET 8 OF 8 PAGE 5-135
	ASSY NO. 22932929		


+RAM OR BUFF ADDR 2^12 + 2^13
+RAM OR BUFF ADDR 2^11 + 2^13
DATA MUX
MUX 10174 3217
MUX 10174 3229
-ROM 2^8
-ROM 2^9
-ROM 2^10
-ROM 2^11
GRP 5+6
GRP 3+4
GRP 1+2
-BIT 8
-BIT 9
-BIT 10
-BIT 11
+ RAM OR BUFF ADDR 2^13
+ RAM OR BUFF ADDR 2^12
+ RAM OR BUFF ADDR 2^11
+ RAM OR BUFF ADDR 2^10
+ RAM OR BUFF ADDR 2^9
+ RAM OR BUFF ADDR 2^8
+ RAM OR BUFF ADDR 2^7
+ RAM OR BUFF ADDR 2^6
+ RAM OR BUFF ADDR 2^5
+ RAM OR BUFF ADDR 2^4
+ RAM OR BUFF ADDR 2^3
+ RAM OR BUFF ADDR 2^2
+ RAM OR BUFF ADDR 2^1
+ RAM OR BUFF ADDR 2^0
-RAM W.E. -2
-RAM W.E., +RAM OR BUFF ADDR 2^0-2^9
-RAM W.E., - RAM OR BUFF ADDR 2^0-2^9
-O BUS ENABLE 8
-O BUS ENABLE 7
-O BUS ENABLE 6
-O BUS ENABLE 5
+ DATA 2^11
+ DATA 2^10
+ DATA 2^9
+ DATA 2^8
-F2
-F1
-F0
-SIGN BIT
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 3, BITS 8-11)
TYPE: AJ
LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 8
PAGE 5-136


PROGRAM RAM
-RAM W.E., -RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 4
RAM GROUP 3
A1023
A0000
MEM 10415 5517
MEM 10415 6017
MEM 10415 5529
MEM 10415 5505
MEM 10415 6005
MEM 10415 5541
-5.2 V
-ENABLE GROUP 4
-ENABLE GROUP 3
-BIT 8
-BIT 9
-BIT 10
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR (SLICE 3, BITS 8-11)
TYPE: AJ
LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 8
PAGE 5-137


PROGRAM RAM
-RAM W.E., +RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 2
RAM GROUP 1
A1023
A0000
MEM
10415
4417
4917
4429
4905
4441
-5.2 V
-ENABLE GROUP 2
-ENABLE GROUP 1
-BIT 8
-BIT 9
-BIT 10
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 3, BITS 8-11)
TYPE: AJ
LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 8
PAGE 5-138


PROGRAM RAM
BUFFER MEMORY
-RAM W.E.,-RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 4
-ENABLE GROUP 4
MEM 10415 6029
-5.2 V
RAM GROUP 3
-ENABLE GROUP 3
MEM 10415 6041
-BIT 15
-RAM W.E.,+RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 2
-ENABLE GROUP 2
MEM 10415 4929
RAM GROUP 1
-ENABLE GROUP 1
MEM 10415 4941
+BUFF ADDR 2^0-2^9
RAM GROUP 6
GRP 5+6 BIT 8
MEM 10415 1005
RAM GROUP 5
-WRT DATA 8
MEM 10415 1505
A1023 A0000
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 3, BITS 8-11)
TYPE: AJ LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 4 OF 8
PAGE 5-139

BUFFER MEMORY

6 (AF) +BUFF ADDR 2^0–2^9, -ENABLE GRP 5-6, -WRITE ENABLE

RAM GROUP 6

A1023 A0000

MEM 10415 1017

GRP 5+6 BIT 9 (Z) 1,6

-5.2 V

RAM GROUP 5

A1023 A0000

MEM 10415 1517

8 (AM) -WRT DATA 9

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2105

GRP 5+6 BIT 10 (Y) 1,6

-5.2 V

RAM GROUP 5

A1023 A0000

MEM 10415 2605

8 (AN) -WRT DATA 10

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2117

GRP 5+6 BIT 11 (X) 1,6

-5.2 V

RAM GROUP 5

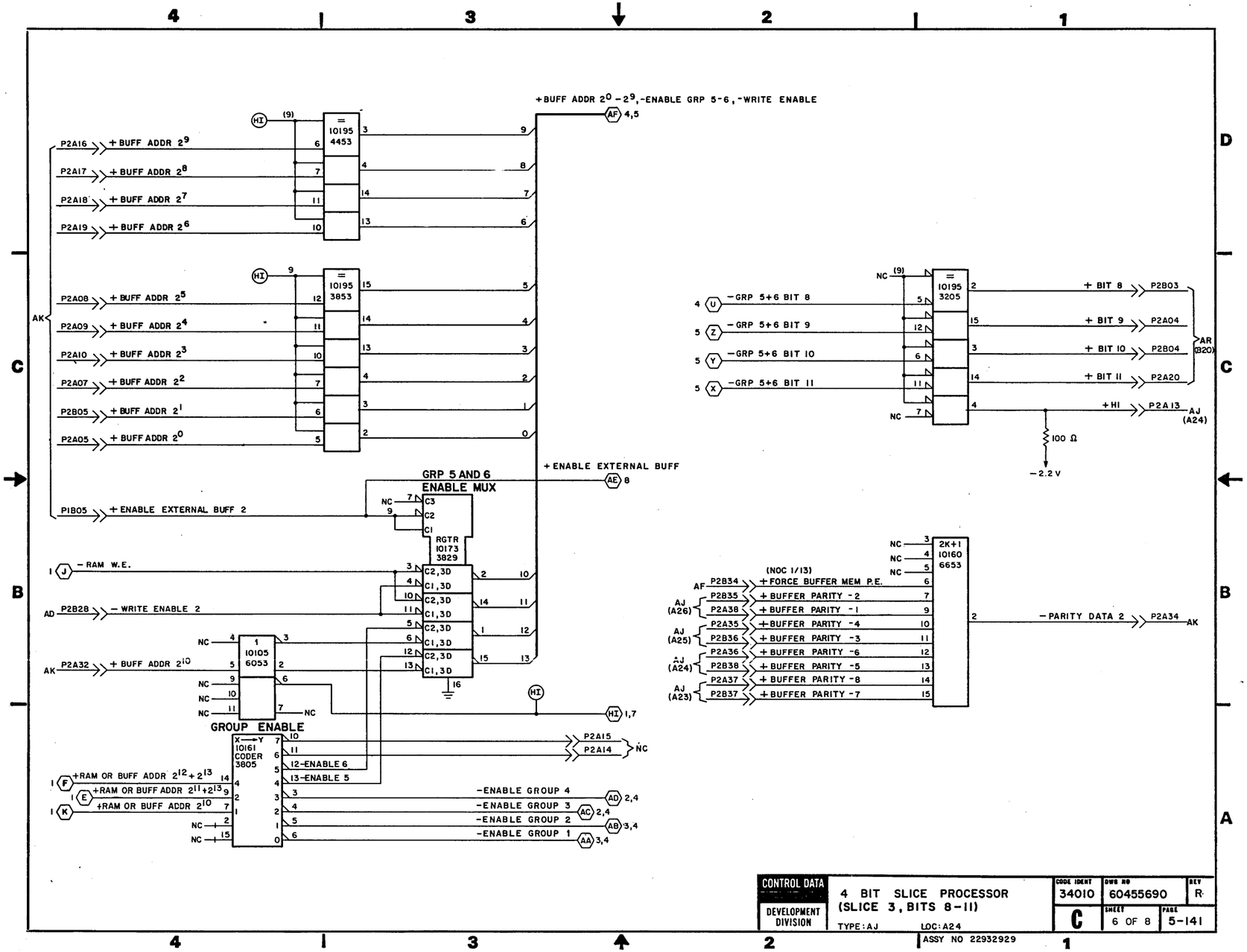
A1023 A0000

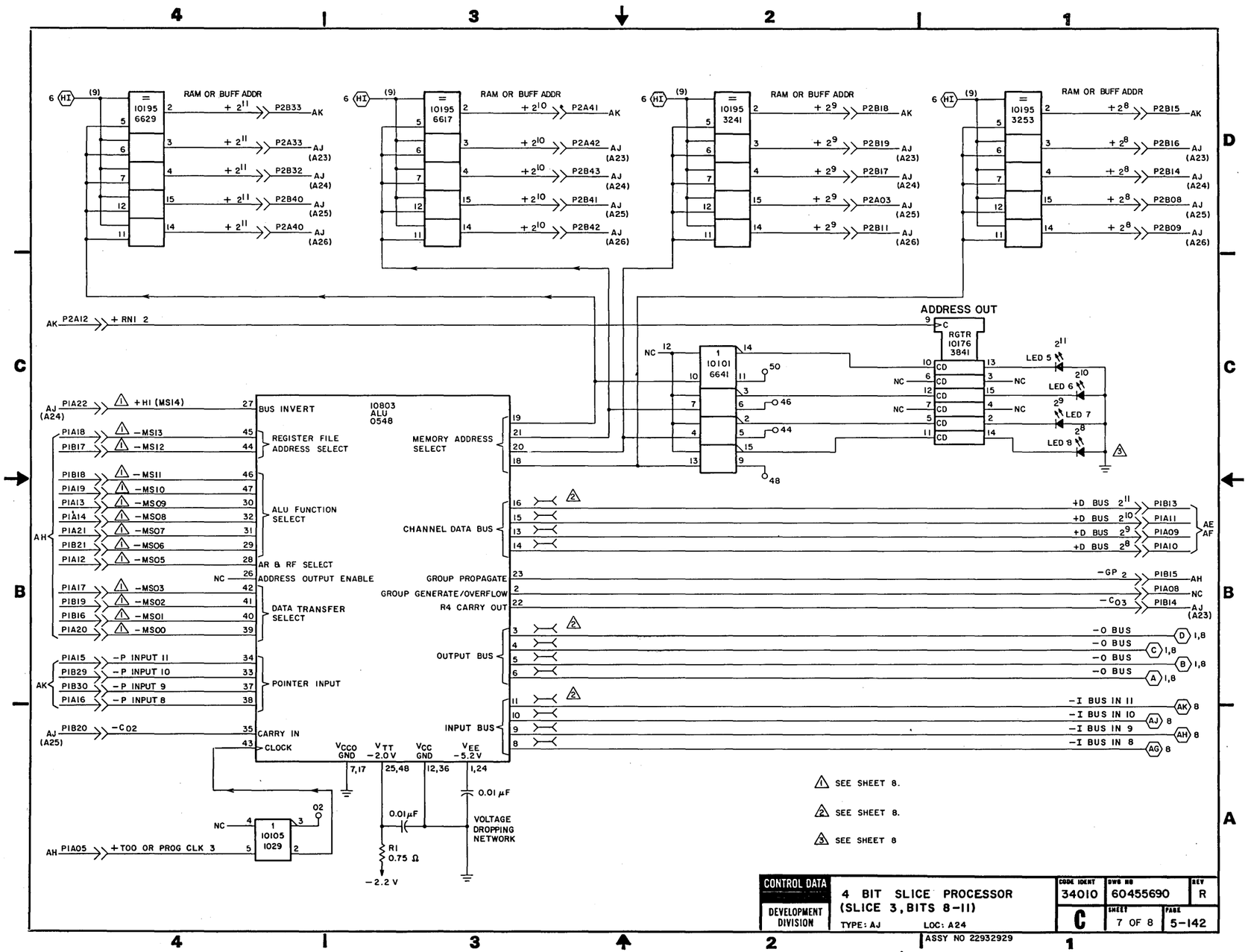
MEM 10415 2617

8 (AP) -WRT DATA 11

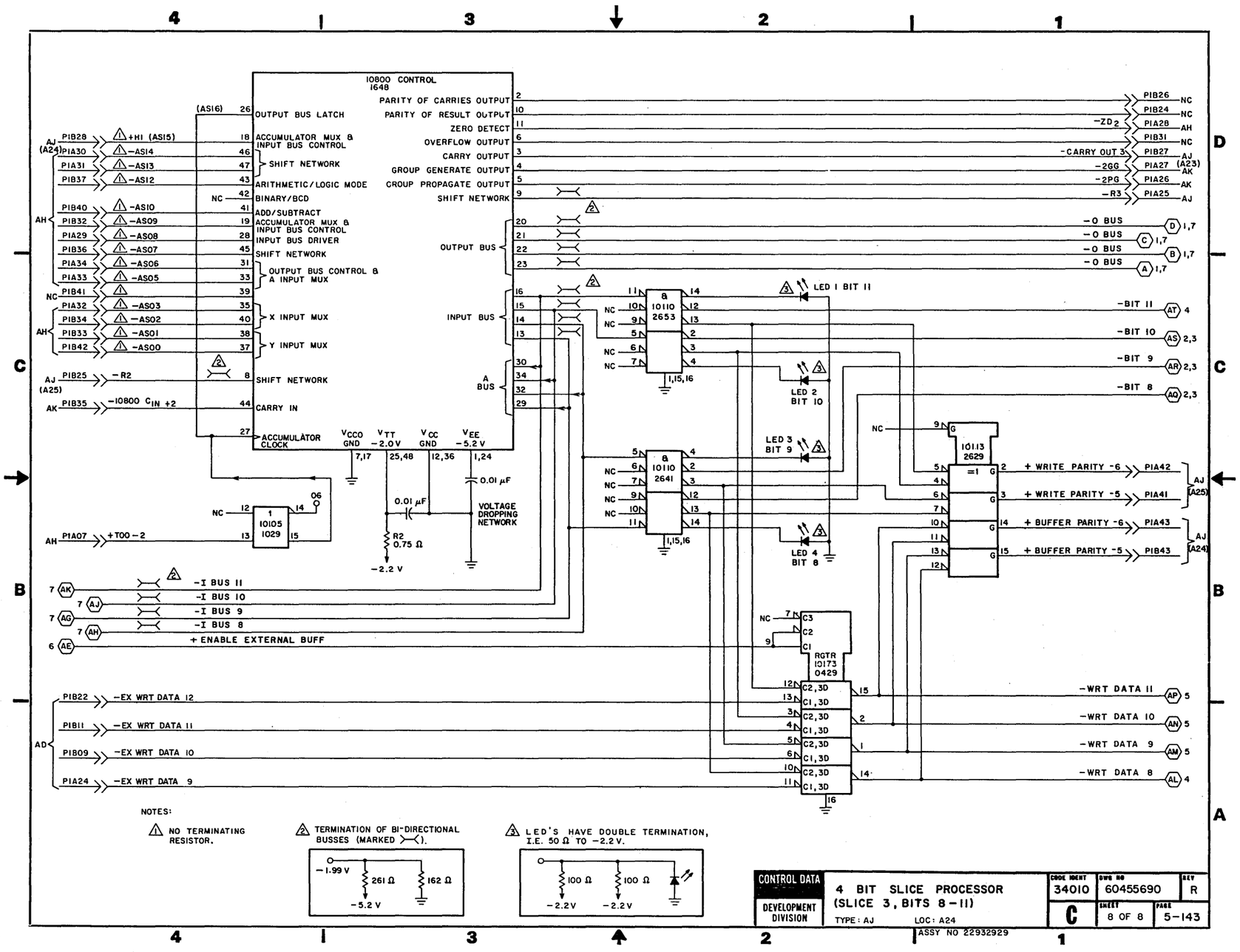
-5.2 V

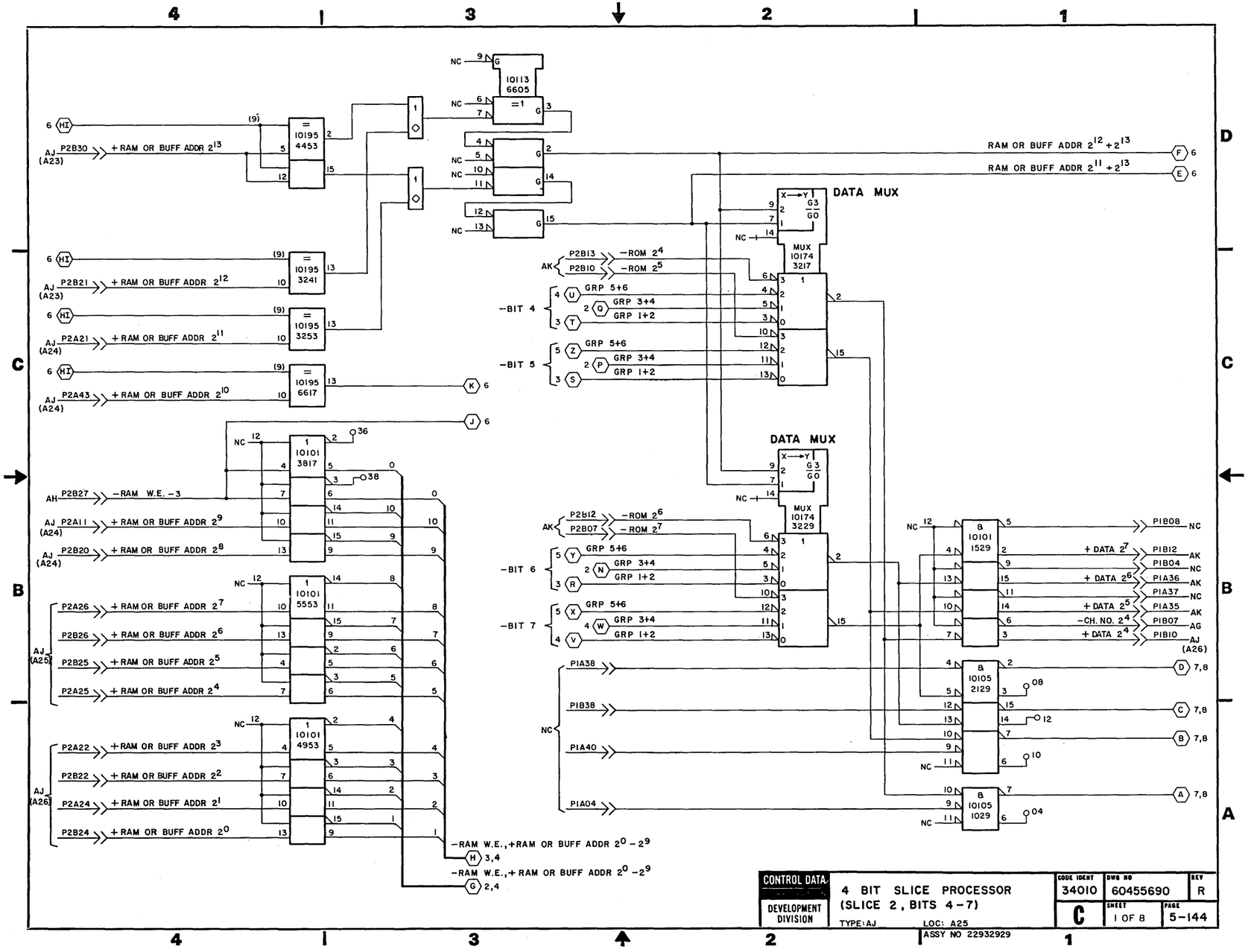
CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 3, BITS 8-11)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A24 ASSY NO 22932929	C	SHEET 5 OF 8	PAGE 5-140


+BUFF ADDR 2^0 - 2^9, -ENABLE GRP 5-6, -WRITE ENABLE
AF 4,5
10195 4453
P2A16 + BUFF ADDR 2^9
P2A17 + BUFF ADDR 2^8
P2A18 + BUFF ADDR 2^7
P2A19 + BUFF ADDR 2^6
10195 3853
P2A08 + BUFF ADDR 2^5
P2A09 + BUFF ADDR 2^4
P2A10 + BUFF ADDR 2^3
P2A07 + BUFF ADDR 2^2
P2B05 + BUFF ADDR 2^1
P2A05 + BUFF ADDR 2^0
AK
+ENABLE EXTERNAL BUFF
AE 8
GRP 5 AND 6 ENABLE MUX
P1B05 + ENABLE EXTERNAL BUFF 2
RGTR 10173 3829
J - RAM W.E.
AD P2B28 - WRITE ENABLE 2
AK P2A32 + BUFF ADDR 2^10
10105 6053
HI 1,7
GROUP ENABLE
10161 CODER 3805
F +RAM OR BUFF ADDR 2^12+2^13
E +RAM OR BUFF ADDR 2^11+2^13
K +RAM OR BUFF ADDR 2^10
12-ENABLE 6
13-ENABLE 5
P2A15
P2A14
NC
-ENABLE GROUP 4
-ENABLE GROUP 3
-ENABLE GROUP 2
-ENABLE GROUP 1
AD 2,4
AC 2,4
AB 3,4
AA 3,4
10195 3205
U -GRP 5+6 BIT 8
Z -GRP 5+6 BIT 9
Y -GRP 5+6 BIT 10
X -GRP 5+6 BIT 11
+ BIT 8 P2B03
+ BIT 9 P2A04
+ BIT 10 P2B04
+ BIT 11 P2A20
AR (B20)
+HI P2A13
AJ (A24)
100 Ω
-2.2 V
2K+1 10160 6653
(NOC 1/13)
+FORCE BUFFER MEM P.E.
+BUFFER PARITY -2
+BUFFER PARITY -1
+BUFFER PARITY -4
+BUFFER PARITY -3
+BUFFER PARITY -6
+BUFFER PARITY -5
+BUFFER PARITY -8
+BUFFER PARITY -7
- PARITY DATA 2 P2A34 AK
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 3, BITS 8-11)
TYPE: AJ
LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 6 OF 8
PAGE 5-141



CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 3, BITS 8-11)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A24 ASSY NO 22932929	C	SHEET 7 OF 8	PAGE 5-142


10800 CONTROL
1648
PARITY OF CARRIES OUTPUT
PARITY OF RESULT OUTPUT
ZERO DETECT
OVERFLOW OUTPUT
CARRY OUTPUT
GROUP GENERATE OUTPUT
GROUP PROPAGATE OUTPUT
SHIFT NETWORK
OUTPUT BUS LATCH
ACCUMULATOR MUX & INPUT BUS CONTROL
SHIFT NETWORK
ARITHMETIC/LOGIC MODE
BINARY/BCD
ADD/SUBTRACT
ACCUMULATOR MUX & INPUT BUS CONTROL
INPUT BUS DRIVER
SHIFT NETWORK
OUTPUT BUS CONTROL & A INPUT MUX
X INPUT MUX
Y INPUT MUX
SHIFT NETWORK
CARRY IN
ACCUMULATOR CLOCK
OUTPUT BUS
INPUT BUS
A BUS
+HI (ASI5)
-ASI4
-ASI3
-ASI2
-ASI0
-ASO9
-ASO8
-ASO7
-ASO6
-ASO5
-ASO3
-ASO2
-ASO1
-ASO0
-R2
-10800 CIN +2
+TOO-2
VCCO GND
VTT -2.0V
VCC GND
VEE -5.2V
0.01 µF
R2 0.75 Ω
-2.2 V
VOLTAGE DROPPING NETWORK
-I BUS 11
-I BUS 10
-I BUS 9
-I BUS 8
+ ENABLE EXTERNAL BUFF
-EX WRT DATA 12
-EX WRT DATA 11
-EX WRT DATA 10
-EX WRT DATA 9
LED 1 BIT 11
LED 2 BIT 10
LED 3 BIT 9
LED 4 BIT 8
-BIT 11
-BIT 10
-BIT 9
-BIT 8
-O BUS
-ZD2
-CARRY OUT 3
-2GG
-2PG
-R3
+ WRITE PARITY -6
+ WRITE PARITY -5
+ BUFFER PARITY -6
+ BUFFER PARITY -5
-WRT DATA 11
-WRT DATA 10
-WRT DATA 9
-WRT DATA 8
10110 2653
10110 2641
10105 1029
10113 2629
RGTR 10173 0429
NOTES:
1 NO TERMINATING RESISTOR.
2 TERMINATION OF BI-DIRECTIONAL BUSSES (MARKED >—<).
3 LED'S HAVE DOUBLE TERMINATION, I.E. 50 Ω TO -2.2 V.
-1.99 V
261 Ω
162 Ω
-5.2 V
100 Ω
100 Ω
-2.2V
-2.2V
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 3, BITS 8-11)
TYPE: AJ
LOC: A24
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 8 OF 8
PAGE 5-143


10113 6605 =1
10195 4453
10195 3241
10195 3253
10195 6617
10101 3817
10101 5553
10101 4953
DATA MUX
MUX 10174 3217
MUX 10174 3229
8 10101 1529
8 10105 2129
8 10105 1029
RAM OR BUFF ADDR 2^12 +2^13
RAM OR BUFF ADDR 2^11 +2^13
+RAM OR BUFF ADDR 2^13
+RAM OR BUFF ADDR 2^12
+RAM OR BUFF ADDR 2^11
+RAM OR BUFF ADDR 2^10
-RAM W.E. -3
+RAM OR BUFF ADDR 2^9
+RAM OR BUFF ADDR 2^8
+RAM OR BUFF ADDR 2^7
+RAM OR BUFF ADDR 2^6
+RAM OR BUFF ADDR 2^5
+RAM OR BUFF ADDR 2^4
+RAM OR BUFF ADDR 2^3
+RAM OR BUFF ADDR 2^2
+RAM OR BUFF ADDR 2^1
+RAM OR BUFF ADDR 2^0
-ROM 2^4
-ROM 2^5
-ROM 2^6
-ROM 2^7
GRP 5+6
GRP 3+4
GRP 1+2
-BIT 4
-BIT 5
-BIT 6
-BIT 7
+DATA 2^7
+DATA 2^6
+DATA 2^5
-CH. NO. 2^4
+DATA 2^4
-RAM W.E.,+RAM OR BUFF ADDR 2^0 - 2^9
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 2, BITS 4-7)
TYPE: AJ
LOC: A25
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 1 OF 8
PAGE 5-144

PROGRAM RAM

-RAM W.E., -RAM OR BUFF ADDR 2^0-2^9 (1 G)

RAM GROUP 4

RAM GROUP 4

RAM GROUP 4

RAM GROUP 3

RAM GROUP 3

RAM GROUP 3

-ENABLE GROUP 4 (6 AD)

-ENABLE GROUP 3 (6 AC)

8 (AQ) -BIT 4

8 (AR) -BIT 5

8 (AS) -BIT 6

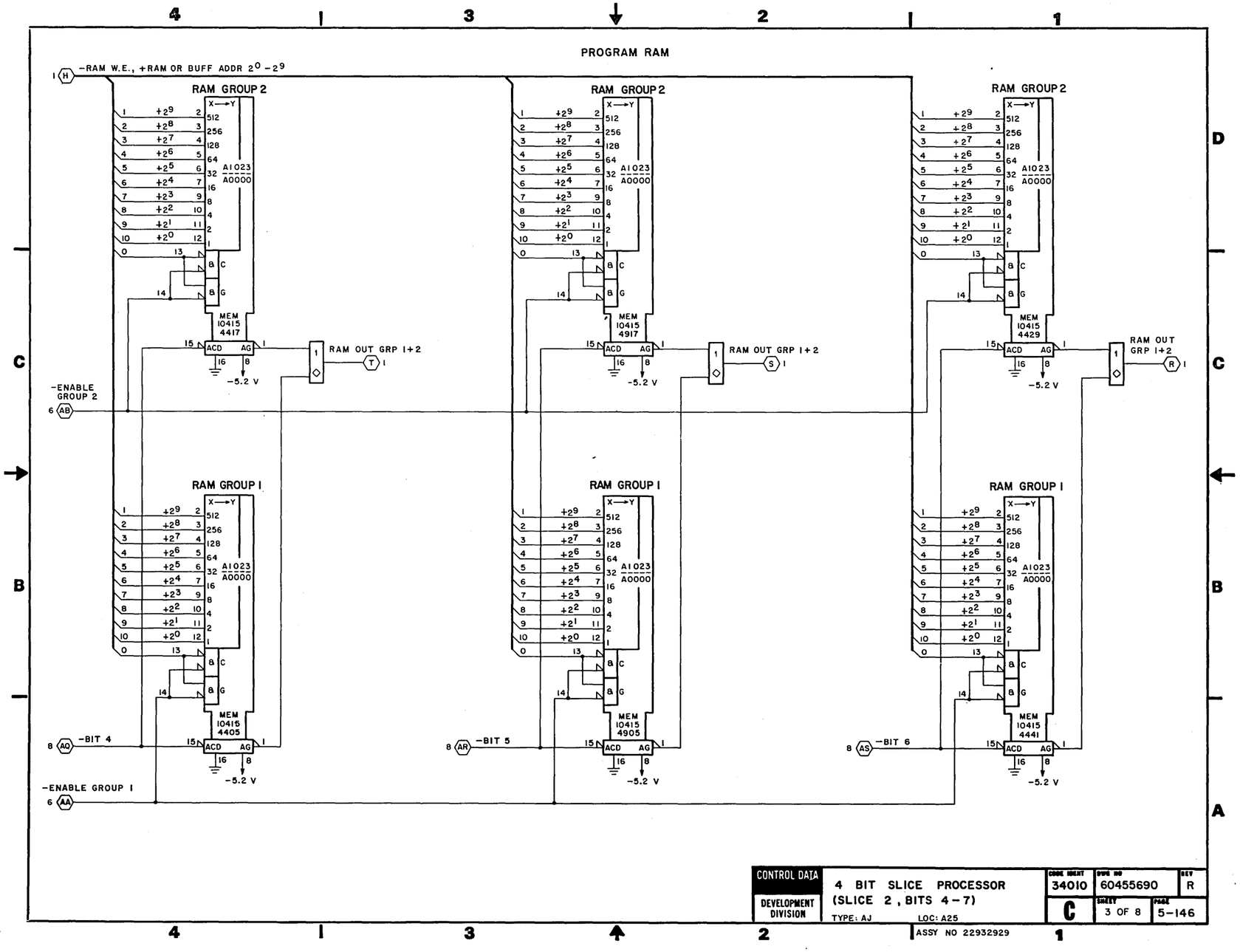
1 (Q) 1

1 (P) 1

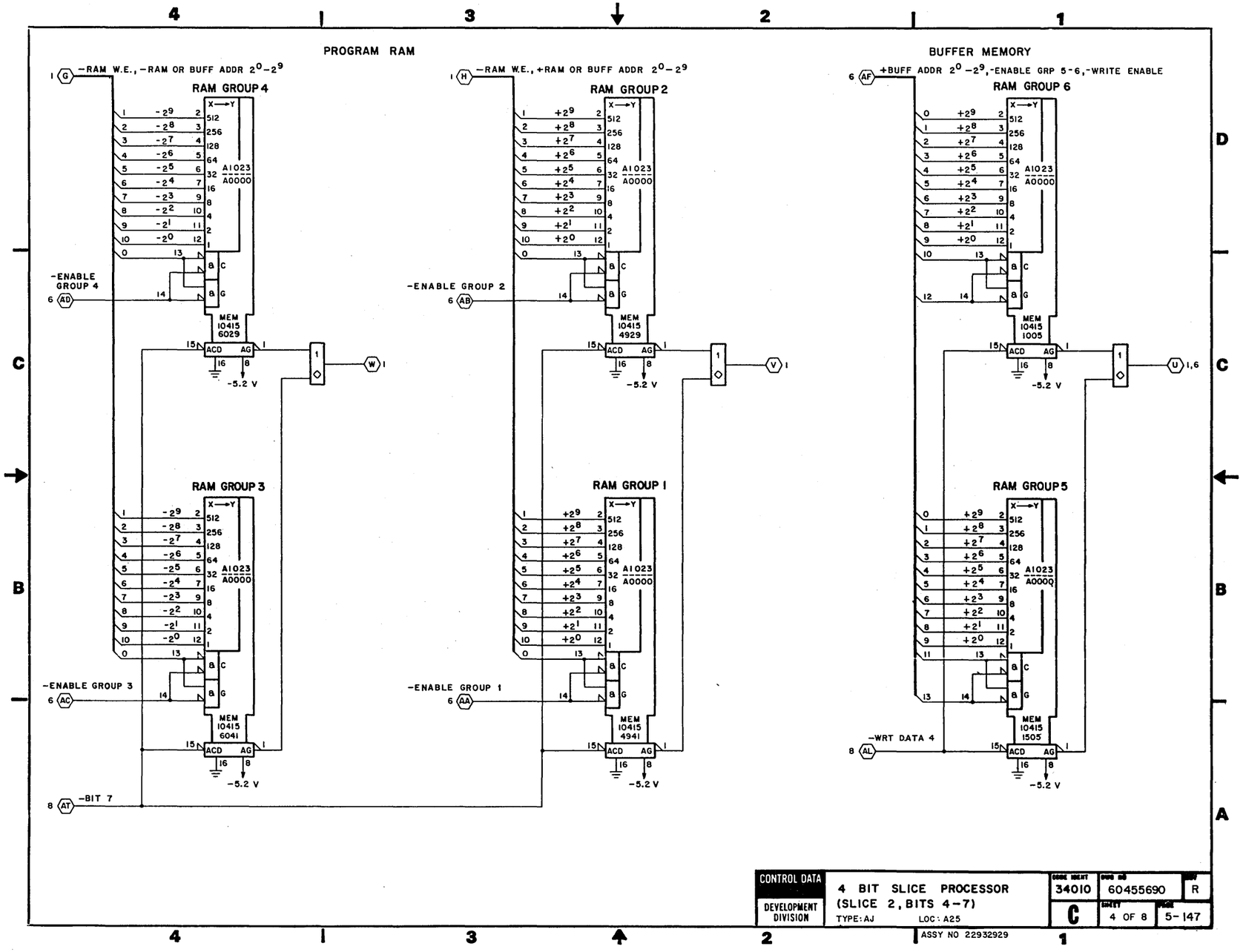
1 (N) 1

-5.2 V

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A25	C	SHEET 2 OF 8	PAGE 5-145
	ASSY NO 22932929			



CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A25 ASSY NO 22932929	C	SHEET 3 OF 8	PAGE 5-146



CONTROL DATA DEVELOPMENT DIVISION	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7) TYPE: AJ LOC: A25	34010 C	60455690 R
	ASSY NO 22932929	SHEET 4 OF 8	PAGE 5-147

BUFFER MEMORY

6 (AF) +BUFF ADDR 2^0-2^9, -ENABLE GRP 5-6, -WRITE ENABLE

RAM GROUP 6

A1023 A0000

MEM 10415 1017

-5.2 V

(Z) 1,6

RAM GROUP 5

A1023 A0000

MEM 10415 1517

8 (AM) -WRT DATA 5

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2105

(Y) 1,6

-5.2 V

RAM GROUP 5

A1023 A0000

MEM 10415 2605

8 (AN) -WRT DATA 6

-5.2 V

RAM GROUP 6

A1023 A0000

MEM 10415 2117

(X) 1,6

-5.2 V

RAM GROUP 5

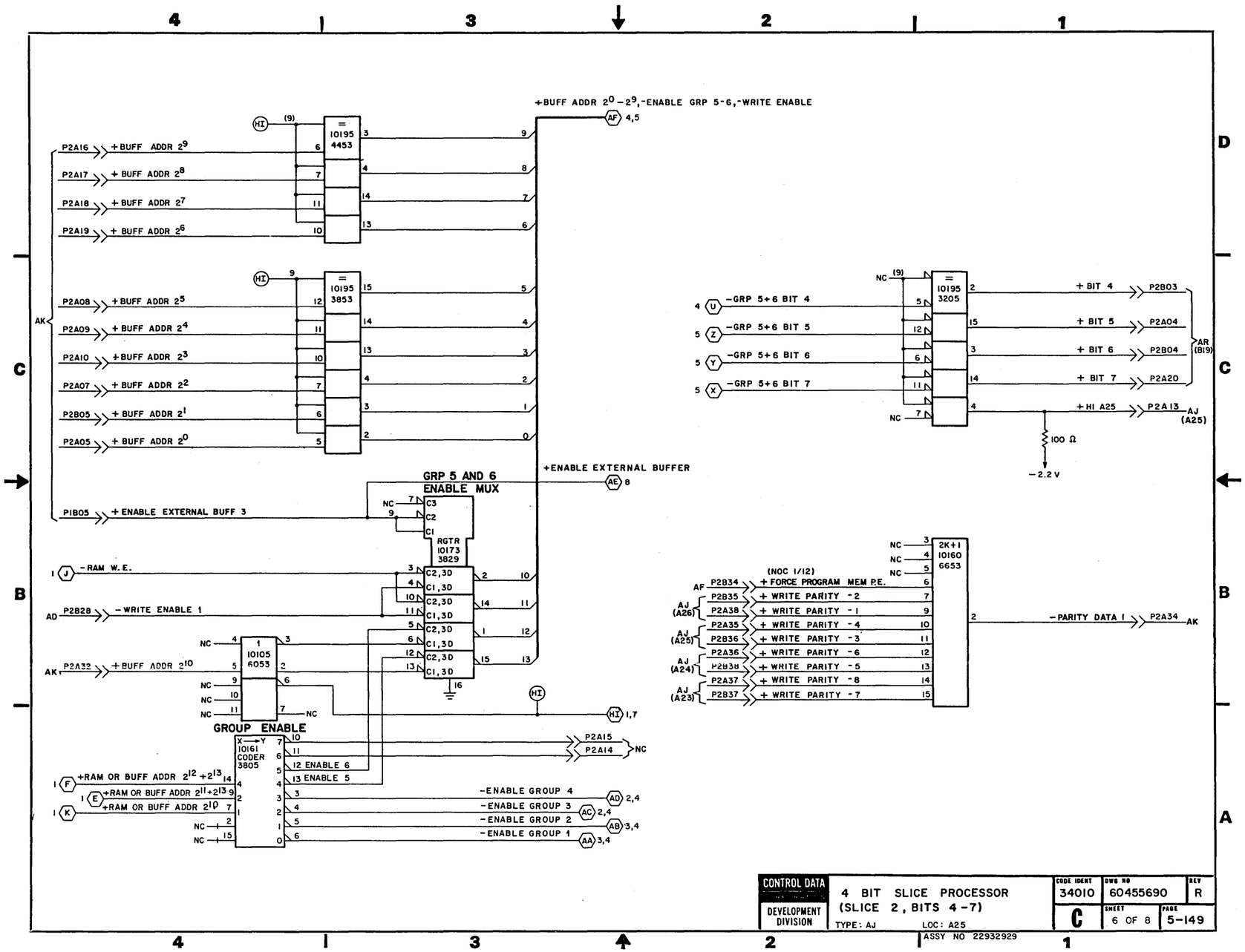
A1023 A0000

MEM 10415 2617

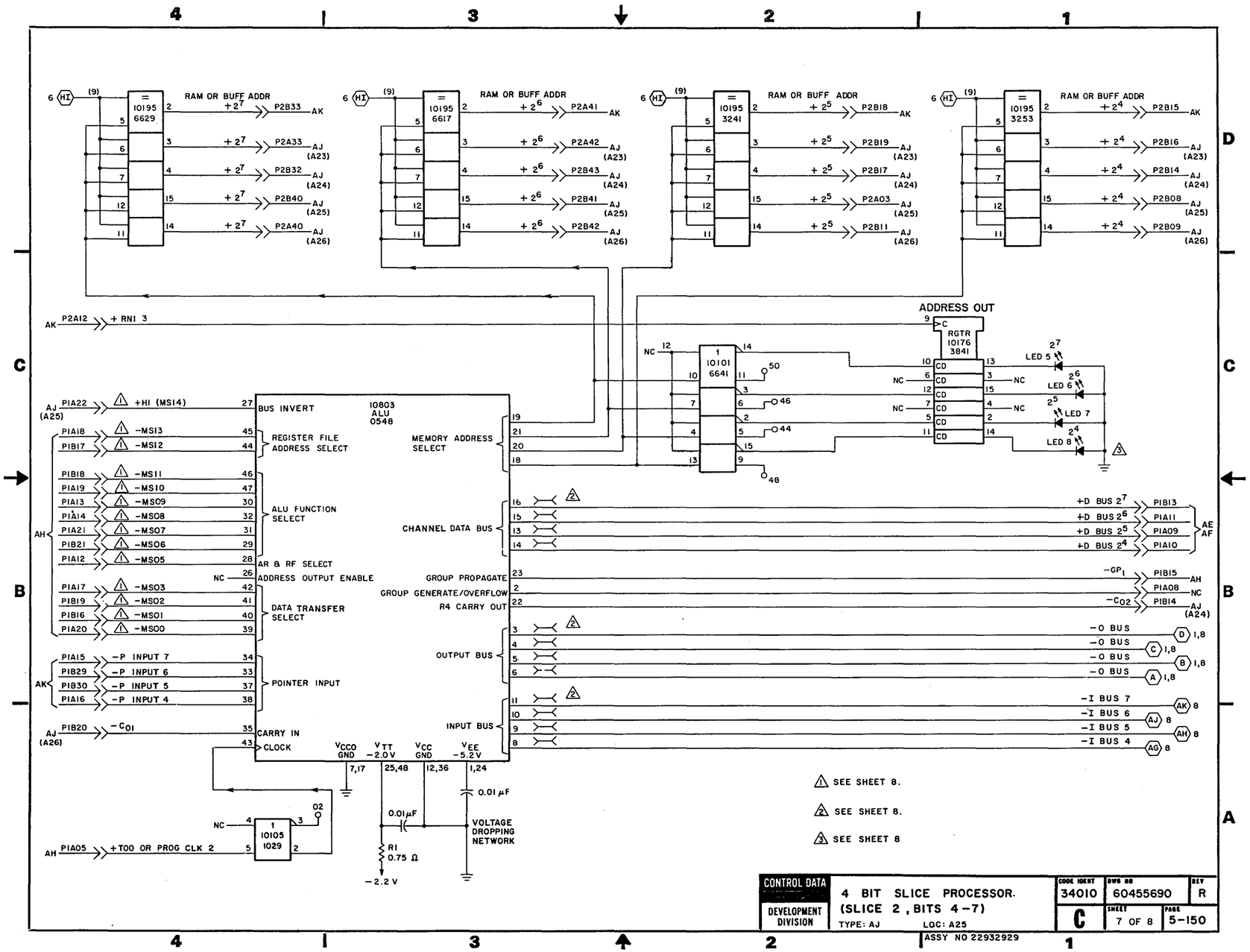
8 (AP) -WRT DATA 7

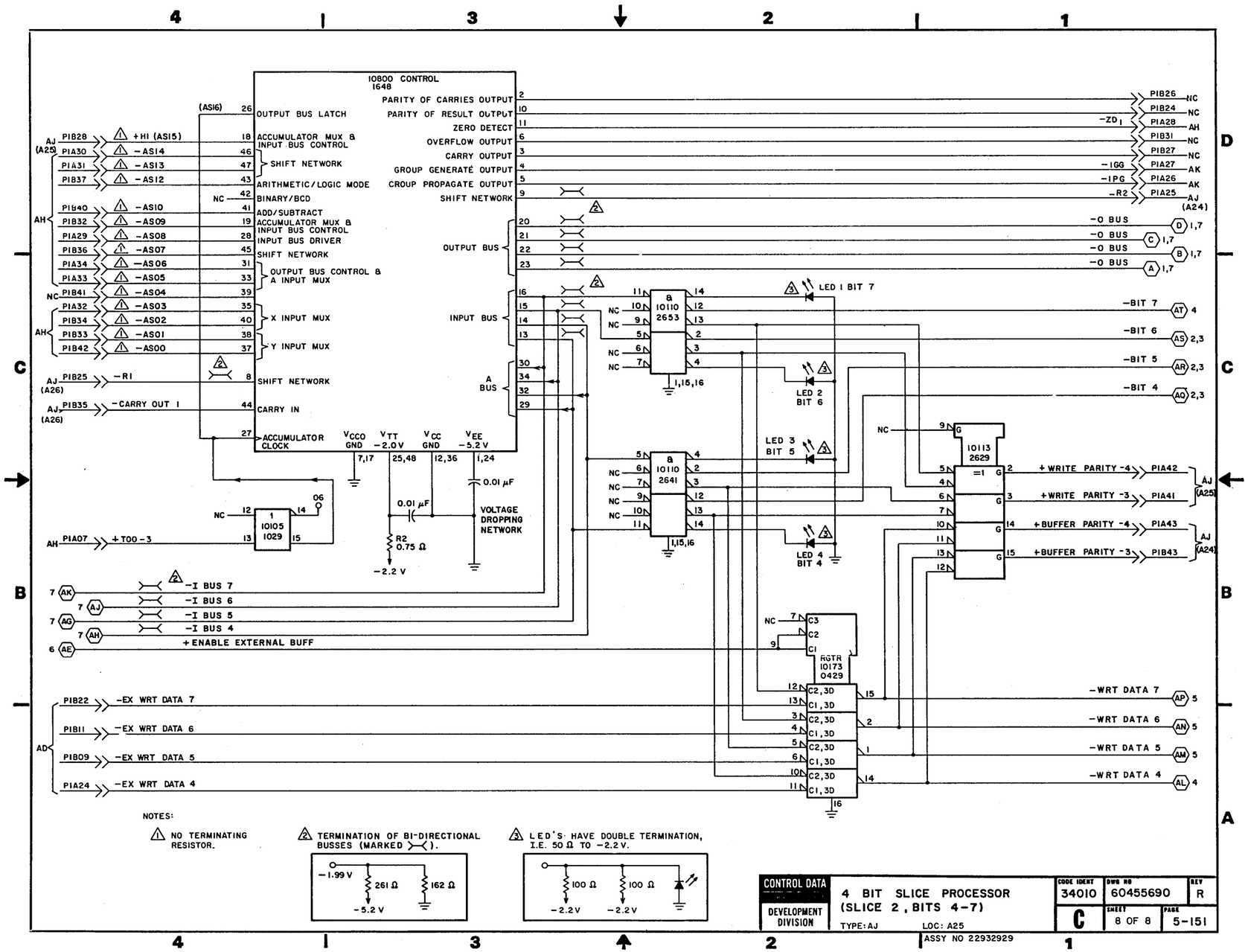
-5.2 V

CONTROL DATA / DEVELOPMENT DIVISION	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7)		CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AJ LOC: A25	ASSY NO. 22932929	C	SHEET 5 OF 8	PAGE 5-148


+BUFF ADDR 2^0-2^9,-ENABLE GRP 5-6,-WRITE ENABLE
AF 4,5
HI (9) = 10195 4453
P2A16 +BUFF ADDR 2^9
P2A17 +BUFF ADDR 2^8
P2A18 +BUFF ADDR 2^7
P2A19 +BUFF ADDR 2^6
HI 9 = 10195 3853
P2A08 +BUFF ADDR 2^5
P2A09 +BUFF ADDR 2^4
P2A10 +BUFF ADDR 2^3
P2A07 +BUFF ADDR 2^2
P2B05 +BUFF ADDR 2^1
P2A05 +BUFF ADDR 2^0
AK
GRP 5 AND 6 ENABLE MUX
+ENABLE EXTERNAL BUFFER
AE 8
P1B05 +ENABLE EXTERNAL BUFF 3
RGTR 10173 3829
J -RAM W.E.
AD P2B28 -WRITE ENABLE 1
AK P2A32 +BUFF ADDR 2^{10}
10105 6053
GROUP ENABLE
10161 CODER 3805
F +RAM OR BUFF ADDR $2^{12}+2^{13}$
E +RAM OR BUFF ADDR $2^{11}+2^{13}$
K +RAM OR BUFF ADDR 2^{10}
12 ENABLE 6
13 ENABLE 5
HI 1,7
P2A15
P2A14 NC
-ENABLE GROUP 4 AD 2,4
-ENABLE GROUP 3 AC 2,4
-ENABLE GROUP 2 AB 3,4
-ENABLE GROUP 1 AA 3,4
NC (9) = 10195 3205
U -GRP 5+6 BIT 4
Z -GRP 5+6 BIT 5
Y -GRP 5+6 BIT 6
X -GRP 5+6 BIT 7
+BIT 4 P2B03
+BIT 5 P2A04
+BIT 6 P2B04
+BIT 7 P2A20
AR (B19)
+HI A25 P2A13 AJ (A25)
100 Ω
-2.2 V
2K+1 10160 6653
(NOC 1/12)
AF P2B34 +FORCE PROGRAM MEM P.E.
AJ (A26) P2B35 +WRITE PARITY -2
P2A38 +WRITE PARITY -1
AJ (A25) P2A35 +WRITE PARITY -4
P2B36 +WRITE PARITY -3
AJ (A24) P2A36 +WRITE PARITY -6
P2B38 +WRITE PARITY -5
P2A37 +WRITE PARITY -8
AJ (A23) P2B37 +WRITE PARITY -7
-PARITY DATA 1 P2A34 AK

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7)	CODE IDENT 34010	DWG NO 60455690 REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A25 ASSY NO 22932929	C	SHEET 6 OF 8 PAGE 5-149

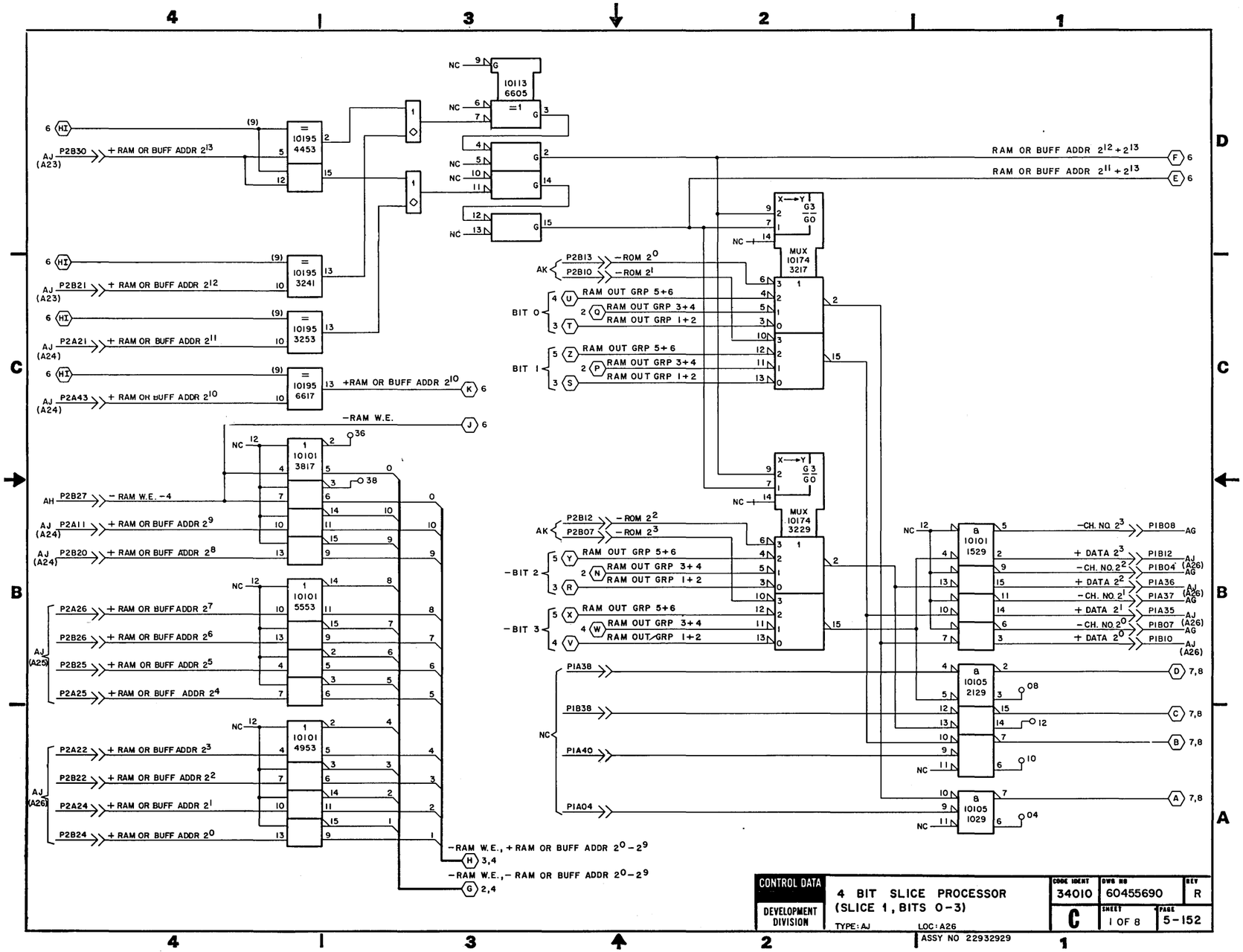

RAM OR BUFF ADDR
10195 6629
10195 6617
10195 3241
10195 3253
ADDRESS OUT
RGTR 10176 3841
10101 6641
10803 ALU 0548
BUS INVERT
REGISTER FILE ADDRESS SELECT
ALU FUNCTION SELECT
AR & RF SELECT
ADDRESS OUTPUT ENABLE
DATA TRANSFER SELECT
POINTER INPUT
CARRY IN
CLOCK
MEMORY ADDRESS SELECT
CHANNEL DATA BUS
GROUP PROPAGATE
GROUP GENERATE/OVERFLOW
R4 CARRY OUT
OUTPUT BUS
INPUT BUS
VOLTAGE DROPPING NETWORK
10105 1029
SEE SHEET 8.
SEE SHEET 8.
SEE SHEET 8
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR.
(SLICE 2, BITS 4-7)
TYPE: AJ
LOC: A25
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 7 OF 8
PAGE 5-150

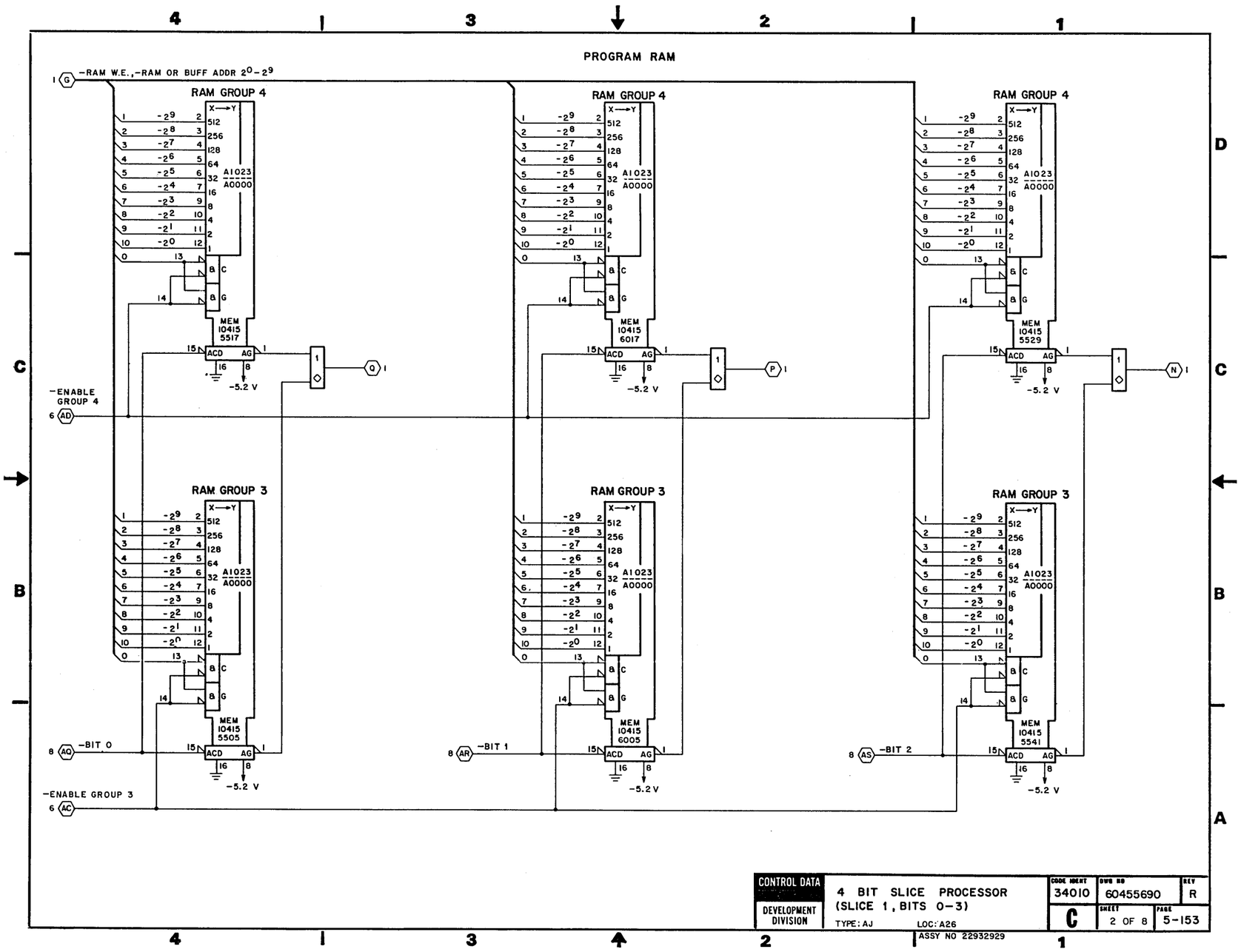


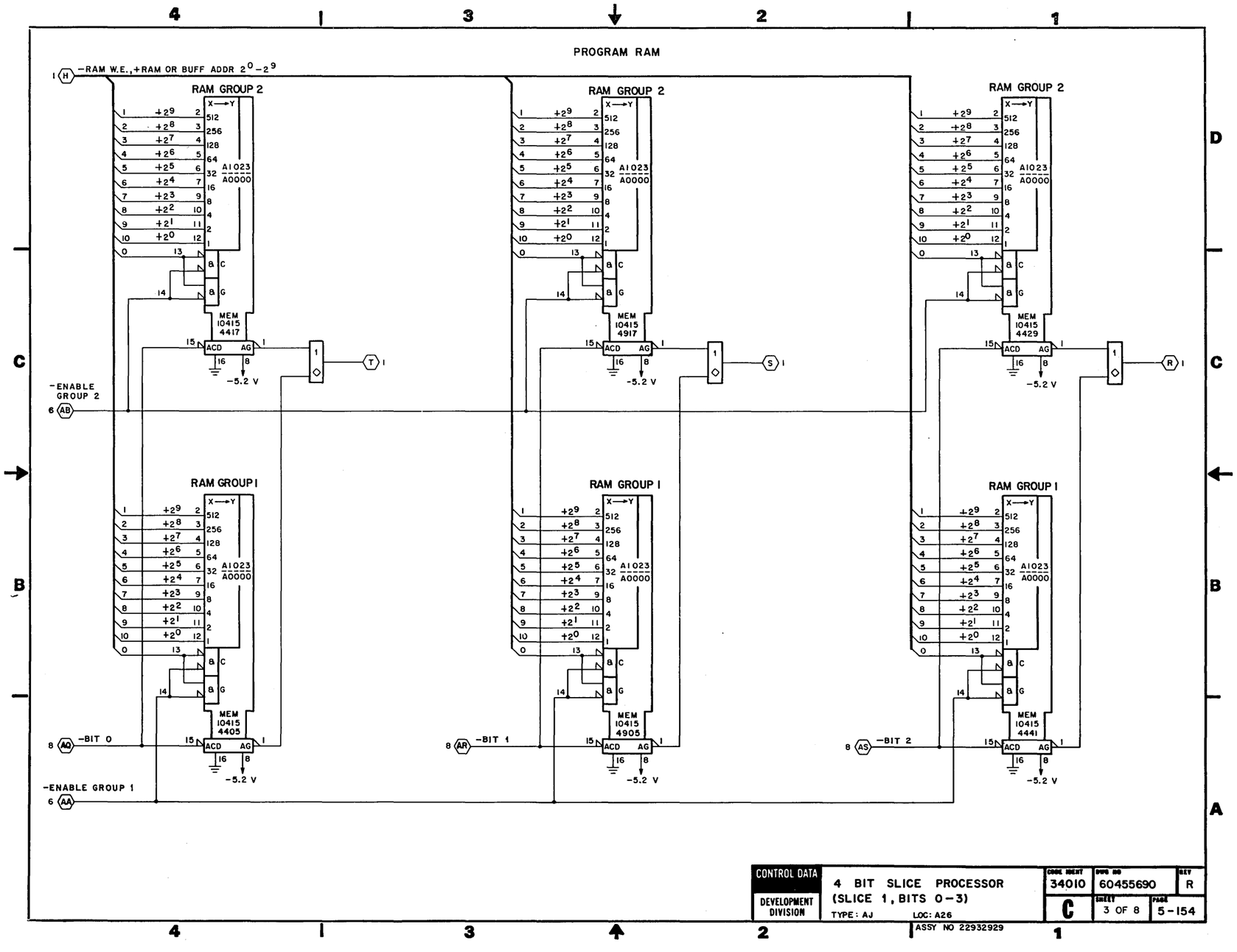
NOTES:

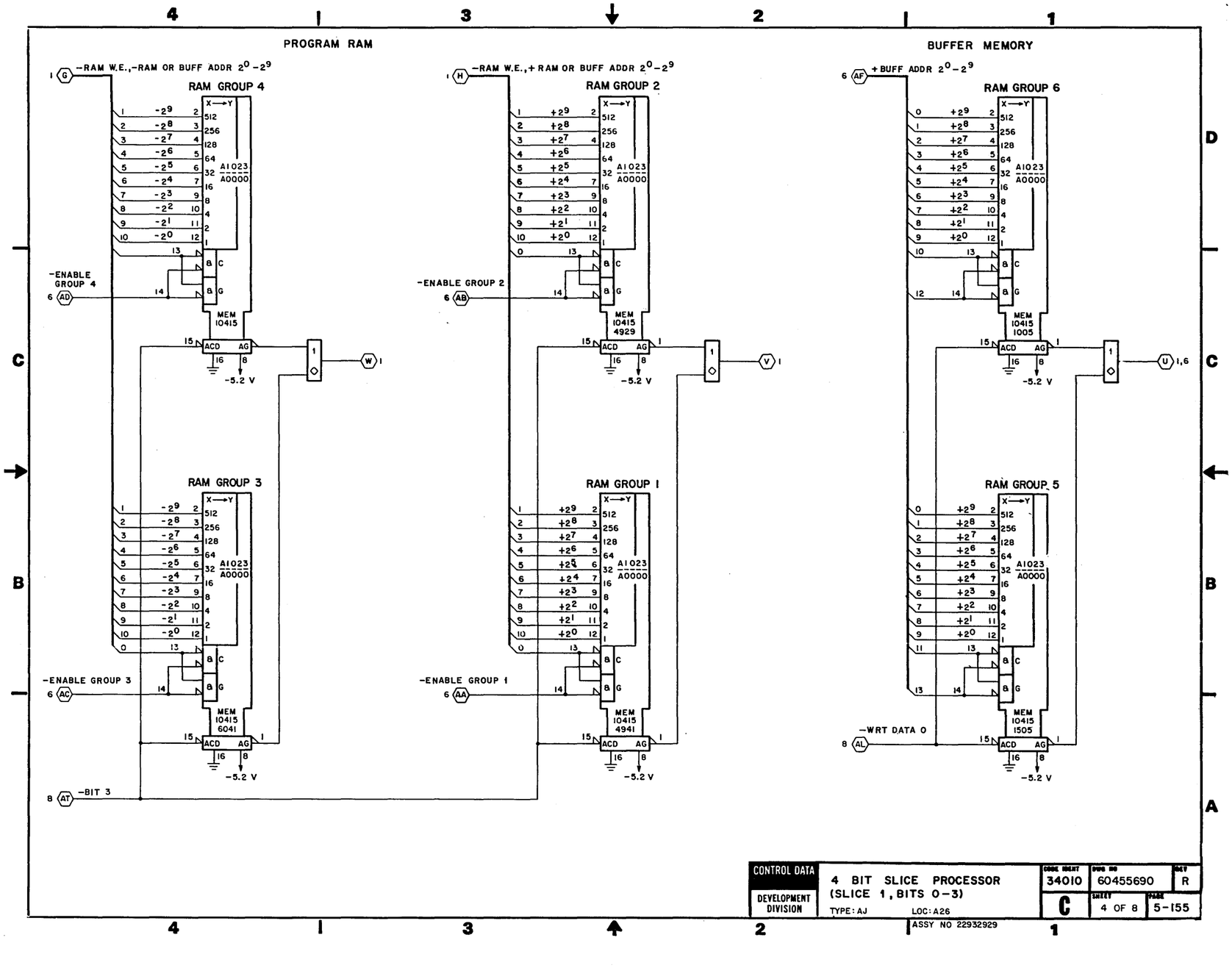
1. NO TERMINATING RESISTOR.
2. TERMINATION OF BI-DIRECTIONAL BUSSES (MARKED >—<). −1.99 V, 261 Ω, 162 Ω, −5.2 V
3. LED'S HAVE DOUBLE TERMINATION, I.E. 50 Ω TO −2.2 V. 100 Ω, 100 Ω, −2.2 V, −2.2 V

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 2, BITS 4-7)		CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A25	ASSY NO 22932929	C	SHEET 8 OF 8	PAGE 5-151


4
3
2
1
D
C
B
A
10113 6605
=1
10195 4453
10195 3241
10195 3253
10195 6617
+RAM OR BUFF ADDR 2^10
-RAM W.E.
1 10101 3817
1 10101 5553
1 10101 4953
-RAM W.E., +RAM OR BUFF ADDR 2^0-2^9
-RAM W.E., -RAM OR BUFF ADDR 2^0-2^9
RAM OR BUFF ADDR 2^12+2^13
RAM OR BUFF ADDR 2^11+2^13
MUX 10174 3217
MUX 10174 3229
-ROM 2^0
-ROM 2^1
-ROM 2^2
-ROM 2^3
RAM OUT GRP 5+6
RAM OUT GRP 3+4
RAM OUT GRP 1+2
BIT 0
BIT 1
-BIT 2
-BIT 3
8 10101 1529
8 10105 2129
8 10105 1029
-CH. NO 2^3
+ DATA 2^3
-CH. NO. 2^2
+ DATA 2^2
-CH. NO. 2^1
+ DATA 2^1
-CH. NO. 2^0
+ DATA 2^0
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ
LOC: A26
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 1 OF 8
PAGE 5-152


PROGRAM RAM
-RAM W.E.,-RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 4
RAM GROUP 3
A1023
A0000
MEM 10415 5517
MEM 10415 6017
MEM 10415 5529
MEM 10415 5505
MEM 10415 6005
MEM 10415 5541
-5.2 V
-ENABLE GROUP 4
-ENABLE GROUP 3
-BIT 0
-BIT 1
-BIT 2
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ
LOC: A26
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 8
PAGE 5-153


PROGRAM RAM
-RAM W.E., +RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 2
RAM GROUP 1
A1023
A0000
MEM
10415
4417
4917
4429
4405
4905
4441
-5.2 V
-ENABLE GROUP 2
-ENABLE GROUP 1
-BIT 0
-BIT 1
-BIT 2
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ
LOC: A26
ASSY NO 22932929
34010
60455690
R
C
3 OF 8
5-154


PROGRAM RAM
BUFFER MEMORY
-RAM W.E.,-RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 4
-ENABLE GROUP 4
RAM GROUP 3
-ENABLE GROUP 3
-BIT 3
-RAM W.E.,+RAM OR BUFF ADDR 2^0-2^9
RAM GROUP 2
-ENABLE GROUP 2
RAM GROUP 1
-ENABLE GROUP 1
+BUFF ADDR 2^0-2^9
RAM GROUP 6
RAM GROUP 5
-WRT DATA 0
A1023
A0000
MEM 10415
MEM 10415 4929
MEM 10415 1005
MEM 10415 6041
MEM 10415 4941
MEM 10415 1505
ACD
AG
-5.2 V
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ
LOC: A26
ASSY NO 22932929
34010
60455690
R
C
4 OF 8
5-155

BUFFER MEMORY

6 (AF) +BUFF ADDR 2^0-2^9

RAM GROUP 6

RAM GROUP 5

MEM 10415 1017 — A1023 A0000 — -5.2 V — (Z) 1,6

MEM 10415 2105 — A1023 A0000 — -5.2 V — (Y) 1,6

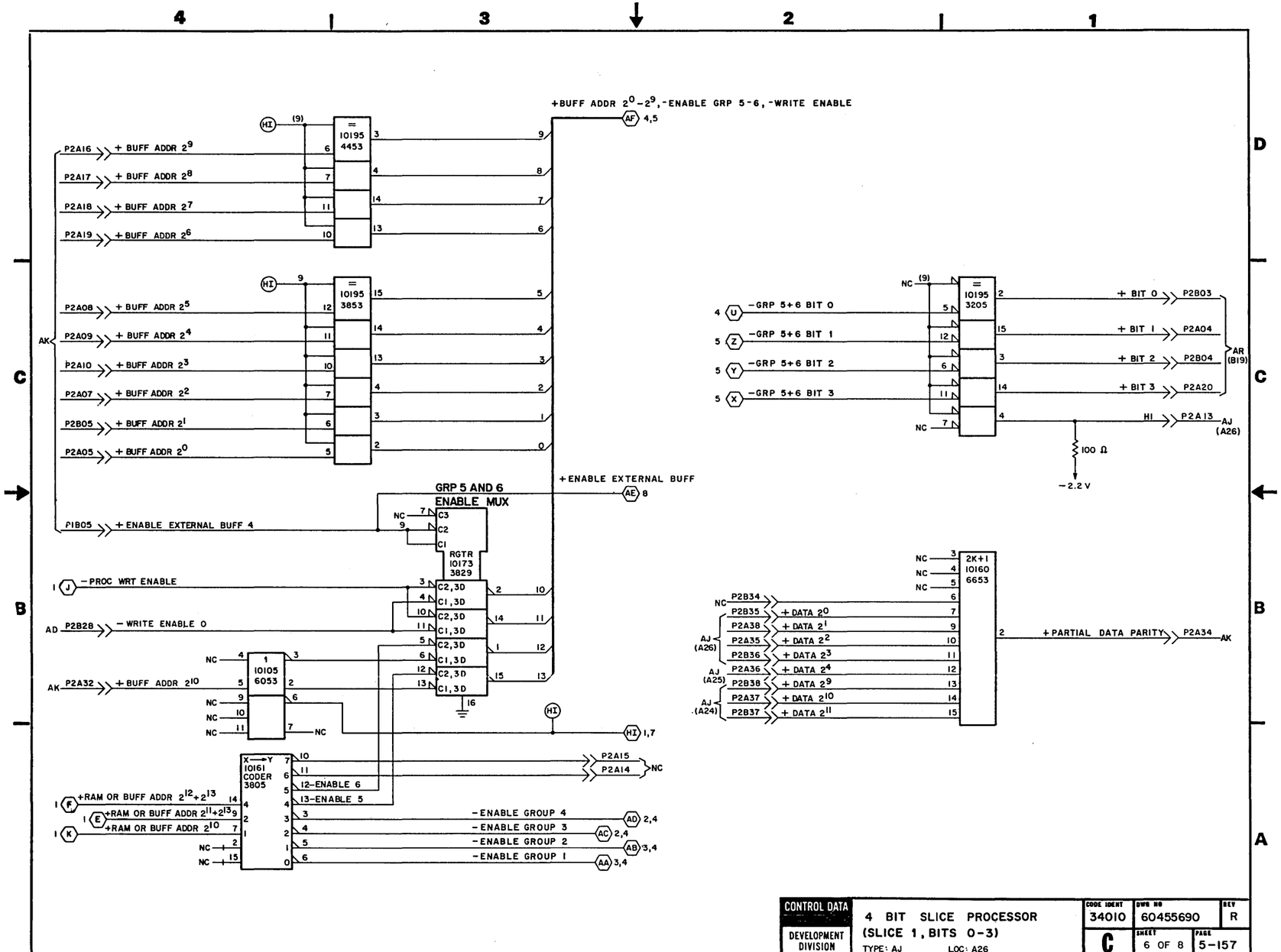
MEM 10415 2117 — A1023 A0000 — -5.2 V — (X) 1,6

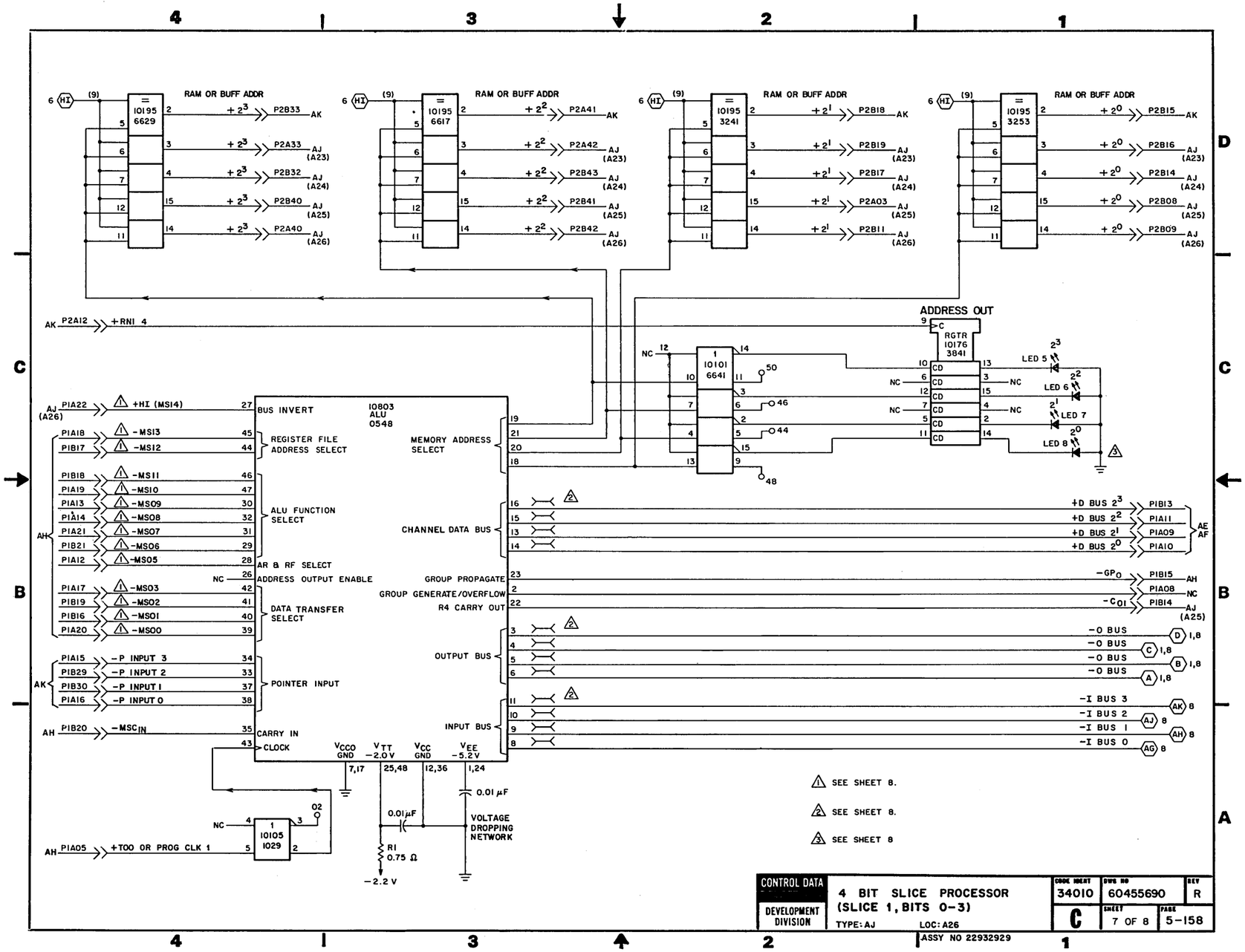
MEM 10415 1517 — A1023 A0000 — -WRT DATA 1 — 8 (AM) — -5.2 V

MEM 10415 2605 — A1023 A0000 — -WRT DATA 2 — 8 (AN) — -5.2 V

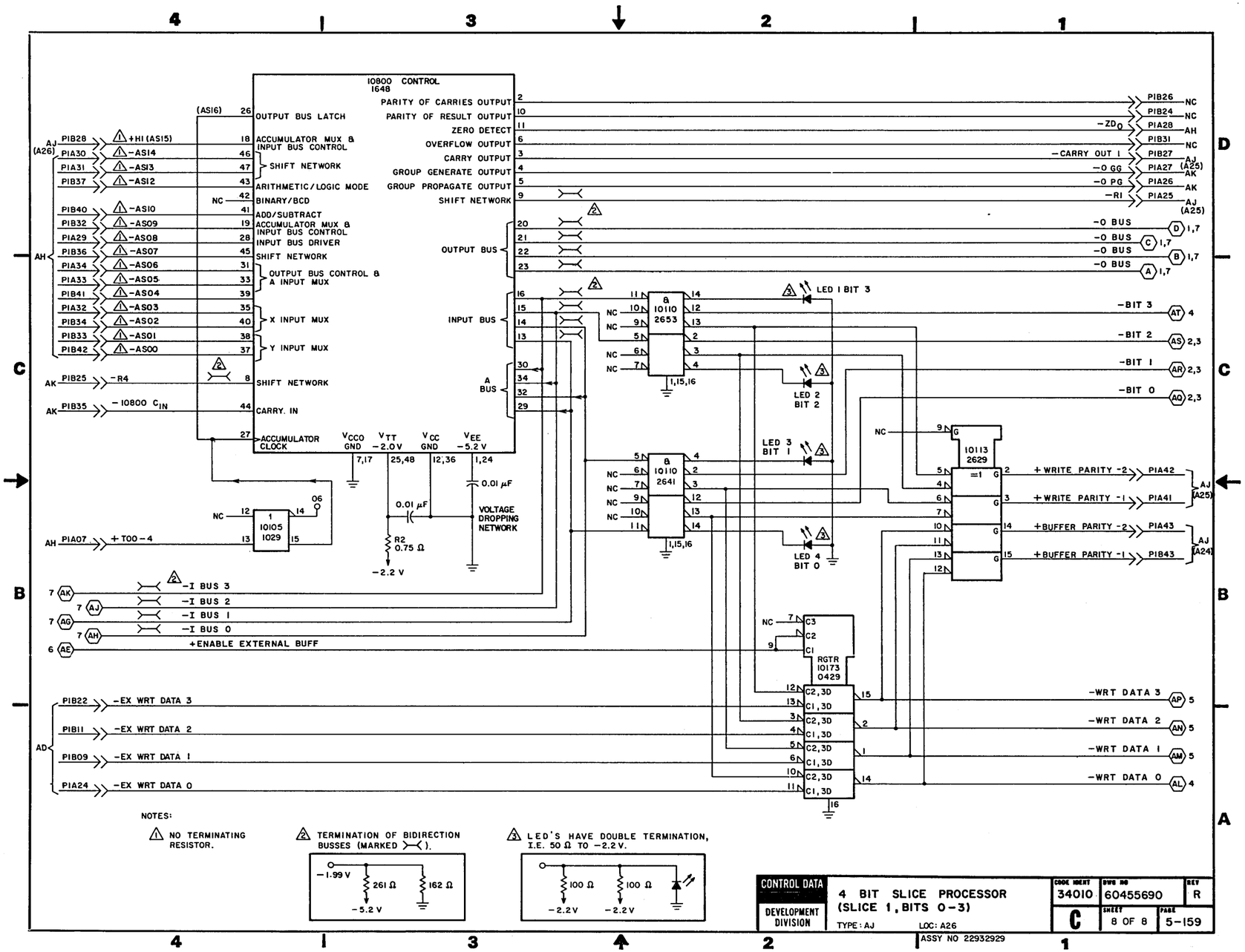
MEM 10415 2617 — A1023 A0000 — -WRT DATA 3 — F (AP) — -5.2 V

CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 1, BITS 0-3)		CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A26	ASSY NO 22932929	C	SHEET 5 OF 8	PAGE 5-156


+BUFF ADDR 2^0-2^9,-ENABLE GRP 5-6,-WRITE ENABLE
AF 4,5
10195 4453
P2A16 + BUFF ADDR 2^9
P2A17 + BUFF ADDR 2^8
P2A18 + BUFF ADDR 2^7
P2A19 + BUFF ADDR 2^6
10195 3853
P2A08 + BUFF ADDR 2^5
P2A09 + BUFF ADDR 2^4
P2A10 + BUFF ADDR 2^3
P2A07 + BUFF ADDR 2^2
P2B05 + BUFF ADDR 2^1
P2A05 + BUFF ADDR 2^0
10195 3205
-GRP 5+6 BIT 0
-GRP 5+6 BIT 1
-GRP 5+6 BIT 2
-GRP 5+6 BIT 3
+ BIT 0 P2B03
+ BIT 1 P2A04
+ BIT 2 P2B04
+ BIT 3 P2A20
AR (B19)
HI P2A13 AJ (A26)
100 Ω
-2.2 V
+ENABLE EXTERNAL BUFF
AE 8
GRP 5 AND 6 ENABLE MUX
P1B05 + ENABLE EXTERNAL BUFF 4
RGTR 10173 3829
-PROC WRT ENABLE
-WRITE ENABLE 0
10105 6053
P2A32 + BUFF ADDR 2^10
HI 1,7
10161 CODER 3805
+RAM OR BUFF ADDR 2^12+2^13
+RAM OR BUFF ADDR 2^11+2^13
+RAM OR BUFF ADDR 2^10
12-ENABLE 6
13-ENABLE 5
P2A15
P2A14 NC
-ENABLE GROUP 4 AD 2,4
-ENABLE GROUP 3 AC 2,4
-ENABLE GROUP 2 AB 3,4
-ENABLE GROUP 1 AA 3,4
2K+1 10160 6653
P2B34
P2B35 + DATA 2^0
P2A38 + DATA 2^1
P2A35 + DATA 2^2
P2B36 + DATA 2^3
P2A36 + DATA 2^4
P2B38 + DATA 2^9
P2A37 + DATA 2^10
P2B37 + DATA 2^11
+PARTIAL DATA PARITY P2A34 AK
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ LOC: A26
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
6 OF 8
PAGE 5-157



CONTROL DATA	4 BIT SLICE PROCESSOR (SLICE 1, BITS 0-3)	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE: AJ LOC: A26 ASSY NO 22932929	C	SHEET 7 OF 8	PAGE 5-158


10800 CONTROL
1648
PARITY OF CARRIES OUTPUT
PARITY OF RESULT OUTPUT
ZERO DETECT
OVERFLOW OUTPUT
CARRY OUTPUT
GROUP GENERATE OUTPUT
GROUP PROPAGATE OUTPUT
SHIFT NETWORK
OUTPUT BUS
INPUT BUS
A BUS
OUTPUT BUS LATCH
ACCUMULATOR MUX & INPUT BUS CONTROL
SHIFT NETWORK
ARITHMETIC/LOGIC MODE
BINARY/BCD
ADD/SUBTRACT
ACCUMULATOR MUX & INPUT BUS CONTROL
INPUT BUS DRIVER
SHIFT NETWORK
OUTPUT BUS CONTROL & A INPUT MUX
X INPUT MUX
Y INPUT MUX
SHIFT NETWORK
CARRY. IN
ACCUMULATOR CLOCK
VCCO GND
VTT −2.0 V
VCC GND
VEE −5.2 V
0.01 μF
VOLTAGE DROPPING NETWORK
R2 0.75 Ω
−2.2 V
+HI (AS15)
−AS14
−AS13
−AS12
−AS10
−AS09
−AS08
−AS07
−AS06
−AS05
−AS04
−AS03
−AS02
−AS01
−AS00
−R4
− 10800 C_{IN}
+ TOO − 4
−I BUS 3
−I BUS 2
−I BUS 1
−I BUS 0
+ENABLE EXTERNAL BUFF
−EX WRT DATA 3
−EX WRT DATA 2
−EX WRT DATA 1
−EX WRT DATA 0
8 10110 2653
8 10110 2641
1,15,16
LED 1 BIT 3
LED 2 BIT 2
LED 3 BIT 1
LED 4 BIT 0
10113 2629
RGTR 10173 0429
+WRITE PARITY −2
+WRITE PARITY −1
+BUFFER PARITY −2
+BUFFER PARITY −1
−ZD0
−CARRY OUT 1
−O GG
−O PG
−RI
−O BUS
−BIT 3
−BIT 2
−BIT 1
−BIT 0
−WRT DATA 3
−WRT DATA 2
−WRT DATA 1
−WRT DATA 0
NOTES:
1 NO TERMINATING RESISTOR.
2 TERMINATION OF BIDIRECTION BUSSES (MARKED).
3 LED'S HAVE DOUBLE TERMINATION, I.E. 50 Ω TO −2.2 V.
−1.99 V
261 Ω
162 Ω
−5.2 V
100 Ω
100 Ω
−2.2 V
−2.2 V
CONTROL DATA
DEVELOPMENT DIVISION
4 BIT SLICE PROCESSOR
(SLICE 1, BITS 0-3)
TYPE: AJ
LOC: A26
ASSY NO 22932929
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 8 OF 8
PAGE 5-159

MODEL B

BLOCK DIAGRAMS

READ PARITY CHECK

AJ (A23) P1B31 +RAM OR BUFF ADDR 2^{13}

AJ (A26) P2A34 +PARTIAL DATA PARITY

(4)AK P2B36 −RAM PARITY

(6)AK P2A36 −ROM PARITY

AJ (A23) P2B37 +DATA 2^{15}

P2B34 +DATA 2^{14}

P2B41 +DATA 2^{13}

P2A40 +DATA 2^{12}

AJ (A24) P2B40 +DATA 2^{8}

P2A37 +DATA 2^{7}

AJ (A25) P2B38 +DATA 2^{6}

P2A38 +DATA 2^{5}

AS P2B18 +HDW MC

AH P2B25 −PARITY ENBL

AH P2A26 −P.E. STROBE

AH P2A09 +RNI

AJ (A23) P2B43 −R4

AH P2B42 +AS 14−1

2K+1 10160 6653

10104 6017

10131 6029

10105 6005

10105 6641

L.E.D.1 ROM P.E.

L.E.D. 2 RAM P.E.

+ROM P.E. P2B19 AH

+RAM P.E. STOP P2A18 AH

+RAM P.E. STATUS (NICO/12) P2B31 AF

10110 4453

+RNI P2B10 AH

+RNI 1 P2A11 AJ (A23)

+RNI 2 P2A10 AJ (A24)

+RNI 3 P2A08 AJ (A25)

+RNI 4 P2A07 AJ (A26)

10195 5517

10104 6017

NS DL17 6605

10105 6617

10105 6005

R=100Ω → V_T

10195 4905

−O BUS ENABLE 5 P2B35

−O BUS ENABLE 6 P2A05

−O BUS ENABLE 7 P2A12 AJ (A24)

−O BUS ENABLE 8 P2B11

−O BUS ENABLE 1 P2A04

−O BUS ENABLE 2 P2B05

−O BUS ENABLE 3 P2B04 AJ (A23)

−O BUS ENABLE 4 P2B03

+STROBE C P2B33 AG

10105 6617

−R4 P2A42 AJ (A26)

−R4 P2A41 AH

10104 6041

10105 6641

B REG

−Ox DETECT P2A35 AH

RGTR 10176 6629

+DATA 2^{7} C 2

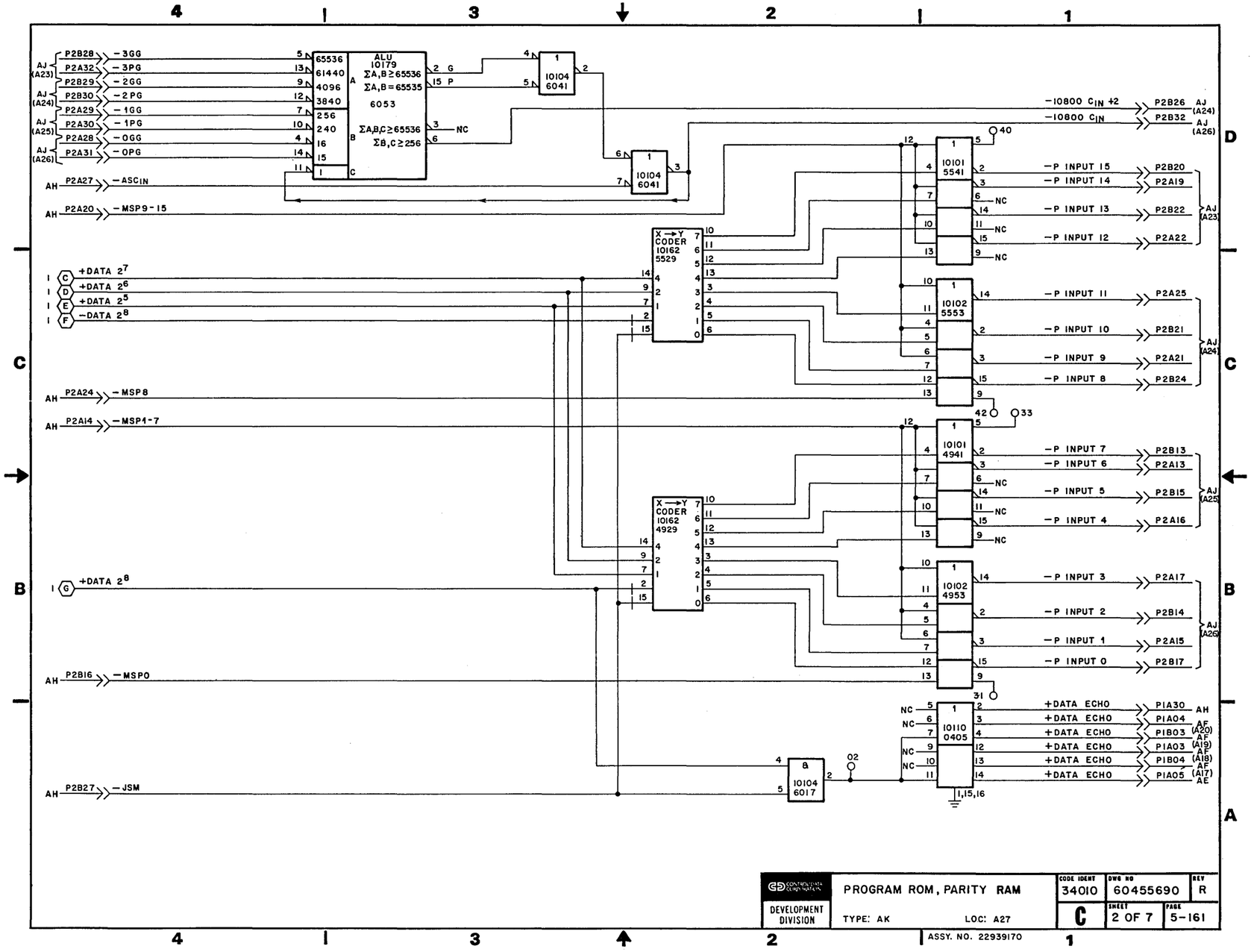
+DATA 2^{6} D 2

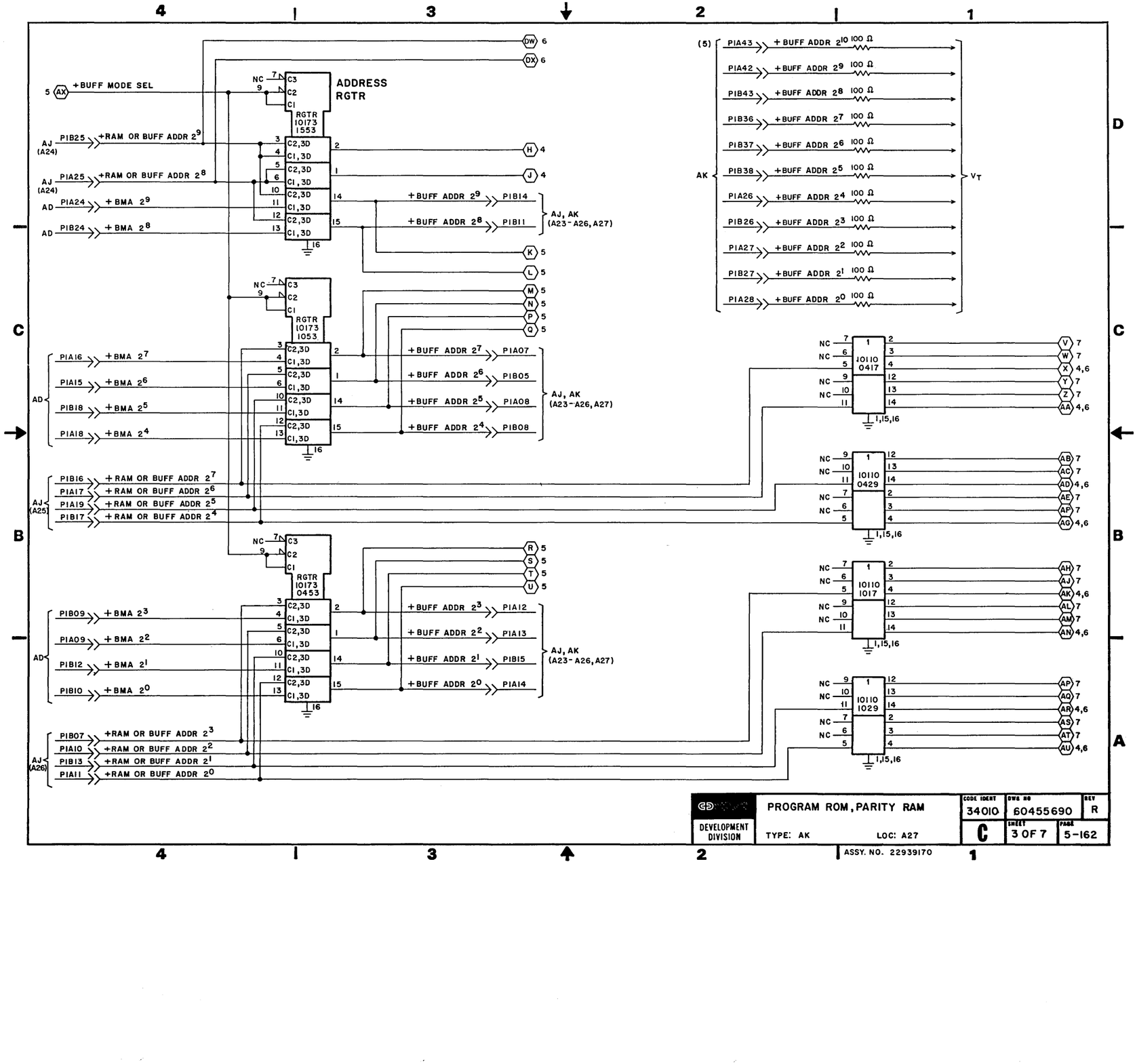
+DATA 2^{5} E 2

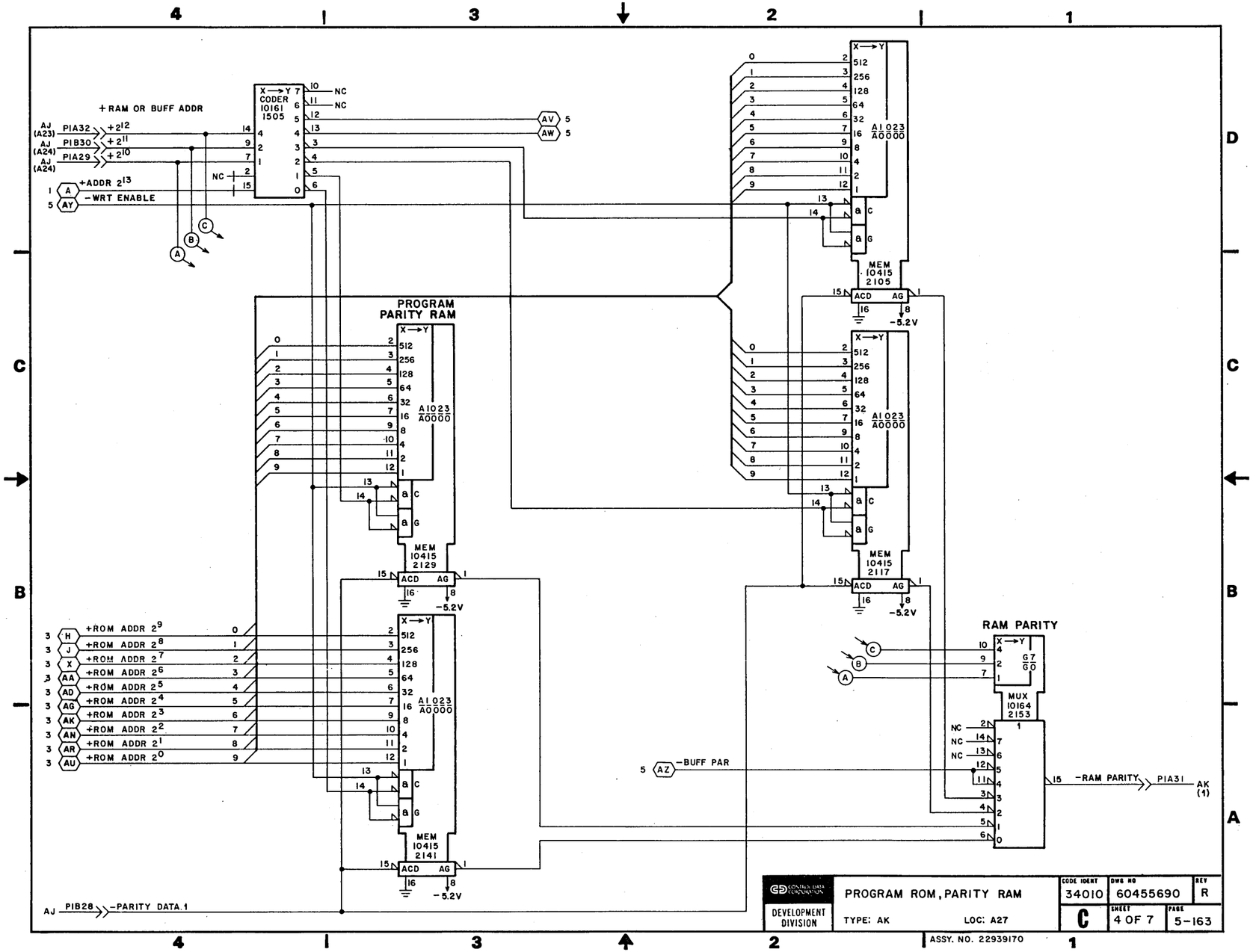
+DATA 2^{8} F 2

+DATA 2^{8} G 2

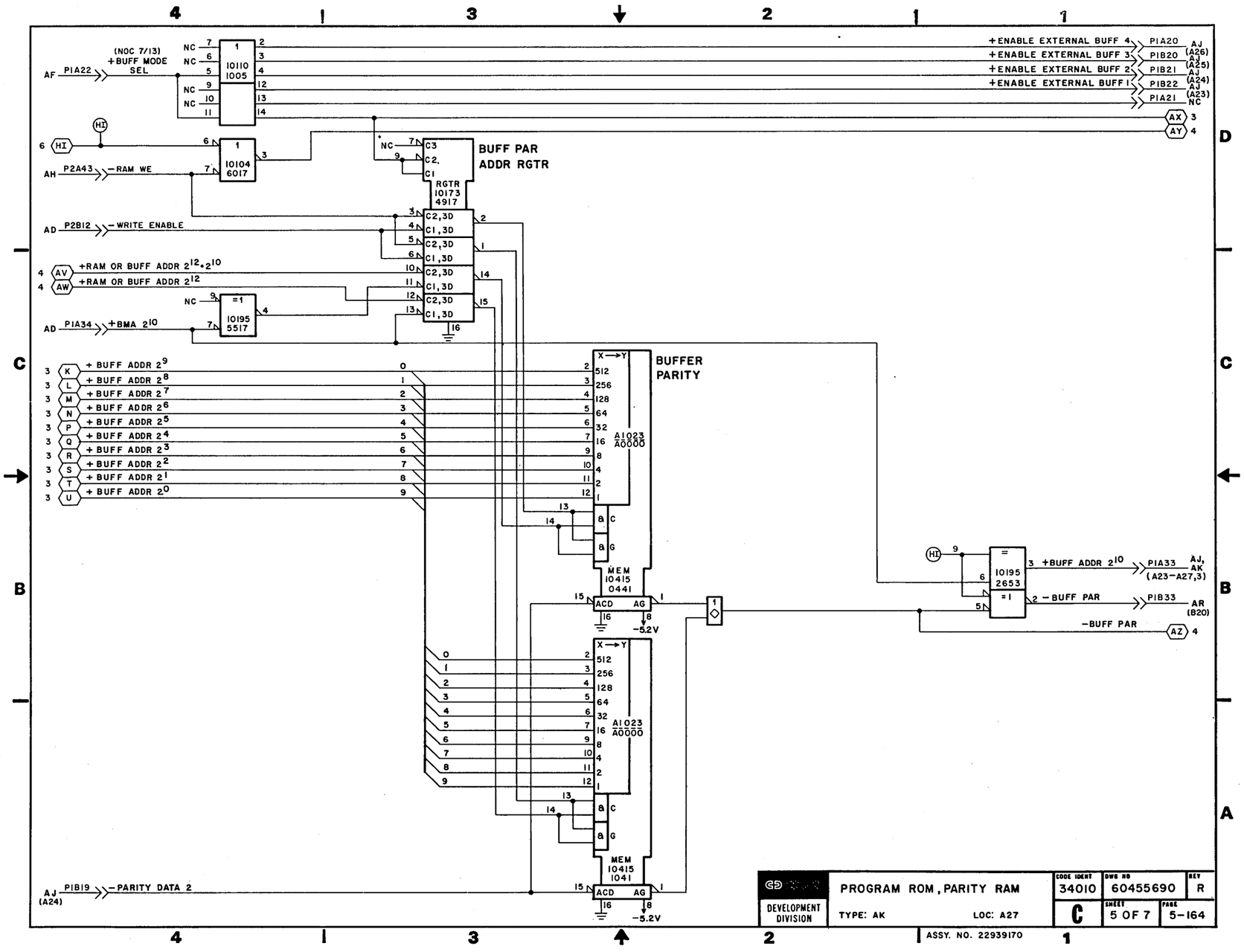
GD DEVELOPMENT DIVISION	PROGRAM ROM, PARITY RAM	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AK LOC: A27	C	SHEET 1 OF 7	PAGE 5−160
	ASSY. NO. 22939170			


ALU 10179 ΣA,B≥65536 ΣA,B=65535 6053 ΣA,B,C≥65536 ΣB,C≥256
65536 61440 4096 3840 256 240 16 15
10104 6041
10101 5541
10102 5553
10101 4941
10102 4953
10110 0405
X→Y CODER 10162 5529
X→Y CODER 10162 4929
10104 6017
-10800 C_IN +2
-10800 C_IN
-P INPUT 15
-P INPUT 14
-P INPUT 13
-P INPUT 12
-P INPUT 11
-P INPUT 10
-P INPUT 9
-P INPUT 8
-P INPUT 7
-P INPUT 6
-P INPUT 5
-P INPUT 4
-P INPUT 3
-P INPUT 2
-P INPUT 1
-P INPUT 0
+DATA ECHO
-3GG
-3PG
-2GG
-2PG
-1GG
-1PG
-0GG
-0PG
-ASC_IN
-MSP9-15
+DATA 2^7
+DATA 2^6
+DATA 2^5
-DATA 2^8
-MSP8
-MSP1-7
+DATA 2^8
-MSP0
-JSM
PROGRAM ROM, PARITY RAM
TYPE: AK
LOC: A27
ASSY. NO. 22939170
DEVELOPMENT DIVISION
34010
60455690
R
C
2 OF 7
5-161

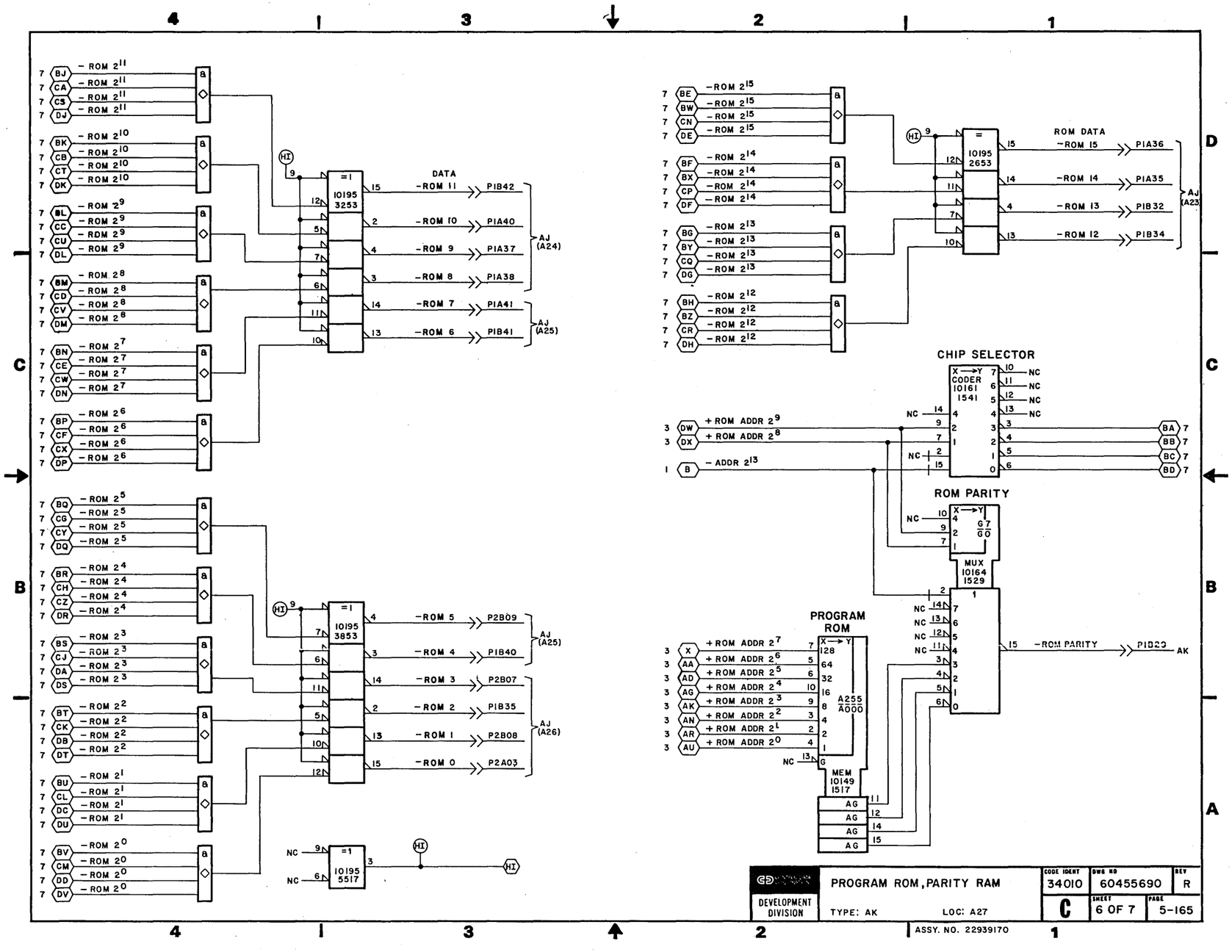

ADDRESS RGTR
RGTR 10173 1553
RGTR 10173 1053
RGTR 10173 0453
+BUFF MODE SEL
+RAM OR BUFF ADDR 2^9
+RAM OR BUFF ADDR 2^8
+BMA 2^9
+BMA 2^8
+BMA 2^7
+BMA 2^6
+BMA 2^5
+BMA 2^4
+RAM OR BUFF ADDR 2^7
+RAM OR BUFF ADDR 2^6
+RAM OR BUFF ADDR 2^5
+RAM OR BUFF ADDR 2^4
+BMA 2^3
+BMA 2^2
+BMA 2^1
+BMA 2^0
+RAM OR BUFF ADDR 2^3
+RAM OR BUFF ADDR 2^2
+RAM OR BUFF ADDR 2^1
+RAM OR BUFF ADDR 2^0
+BUFF ADDR 2^9
+BUFF ADDR 2^8
+BUFF ADDR 2^7
+BUFF ADDR 2^6
+BUFF ADDR 2^5
+BUFF ADDR 2^4
+BUFF ADDR 2^3
+BUFF ADDR 2^2
+BUFF ADDR 2^1
+BUFF ADDR 2^0
AJ, AK (A23-A26, A27)
+BUFF ADDR 2^10 100 Ω
+BUFF ADDR 2^9 100 Ω
+BUFF ADDR 2^8 100 Ω
+BUFF ADDR 2^7 100 Ω
+BUFF ADDR 2^6 100 Ω
+BUFF ADDR 2^5 100 Ω
+BUFF ADDR 2^4 100 Ω
+BUFF ADDR 2^3 100 Ω
+BUFF ADDR 2^2 100 Ω
+BUFF ADDR 2^1 100 Ω
+BUFF ADDR 2^0 100 Ω
10110 0417
10110 0429
10110 1017
10110 1029
PROGRAM ROM, PARITY RAM
TYPE: AK
LOC: A27
DEVELOPMENT DIVISION
ASSY. NO. 22939170
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 7
PAGE 5-162

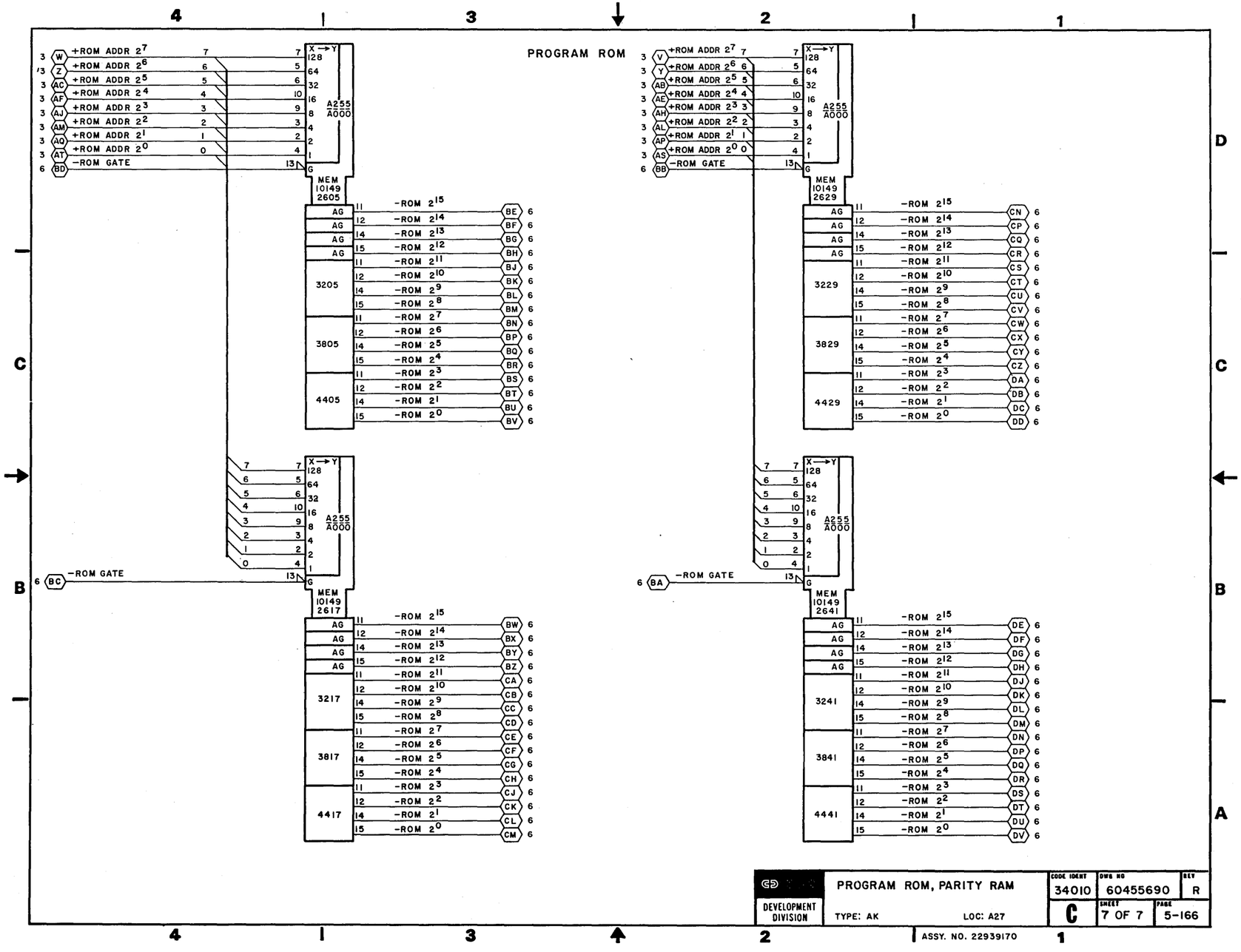


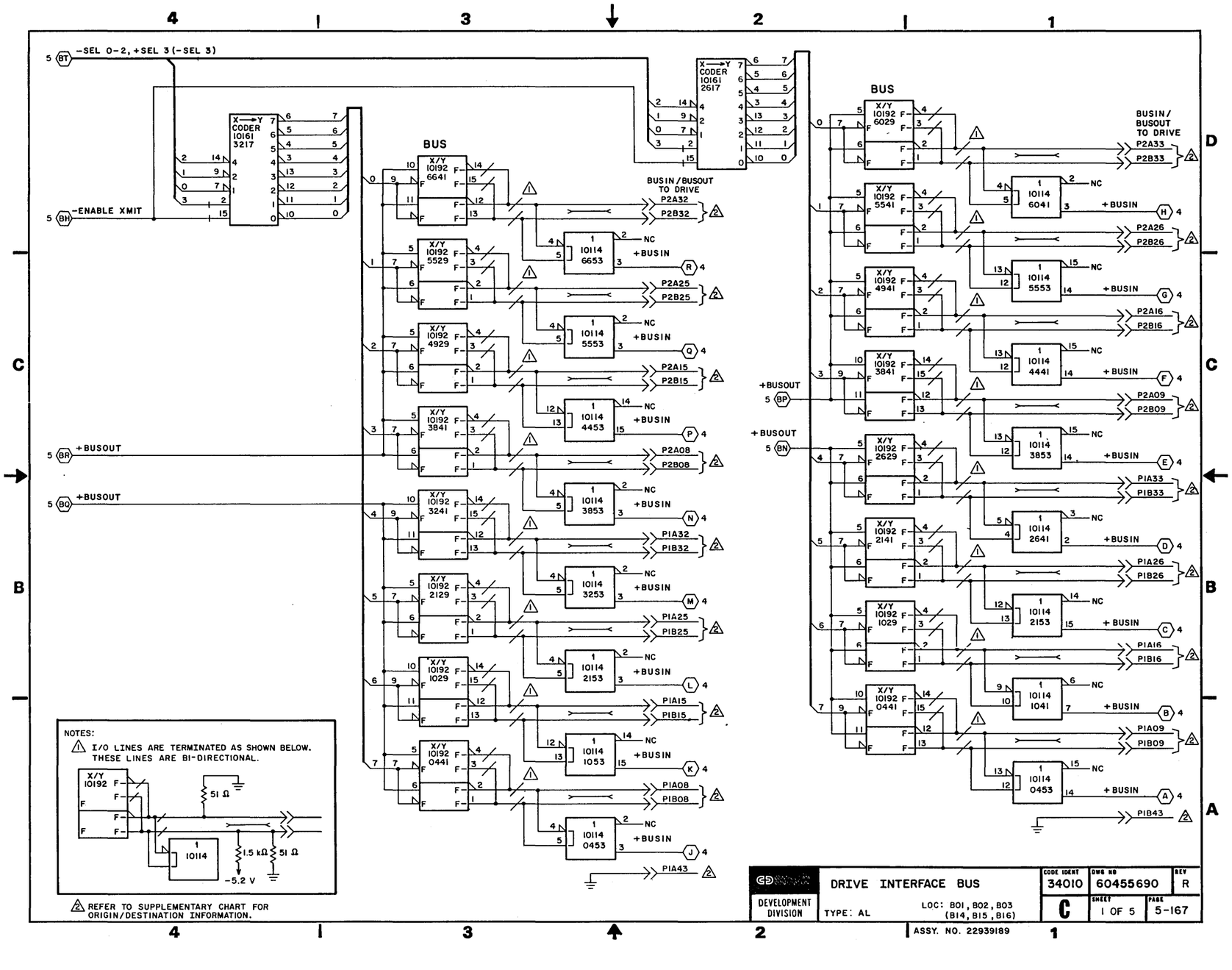
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	PROGRAM ROM, PARITY RAM	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AK LOC: A27	C	SHEET 4 OF 7	PAGE 5-163
	ASSY. NO. 22939170			

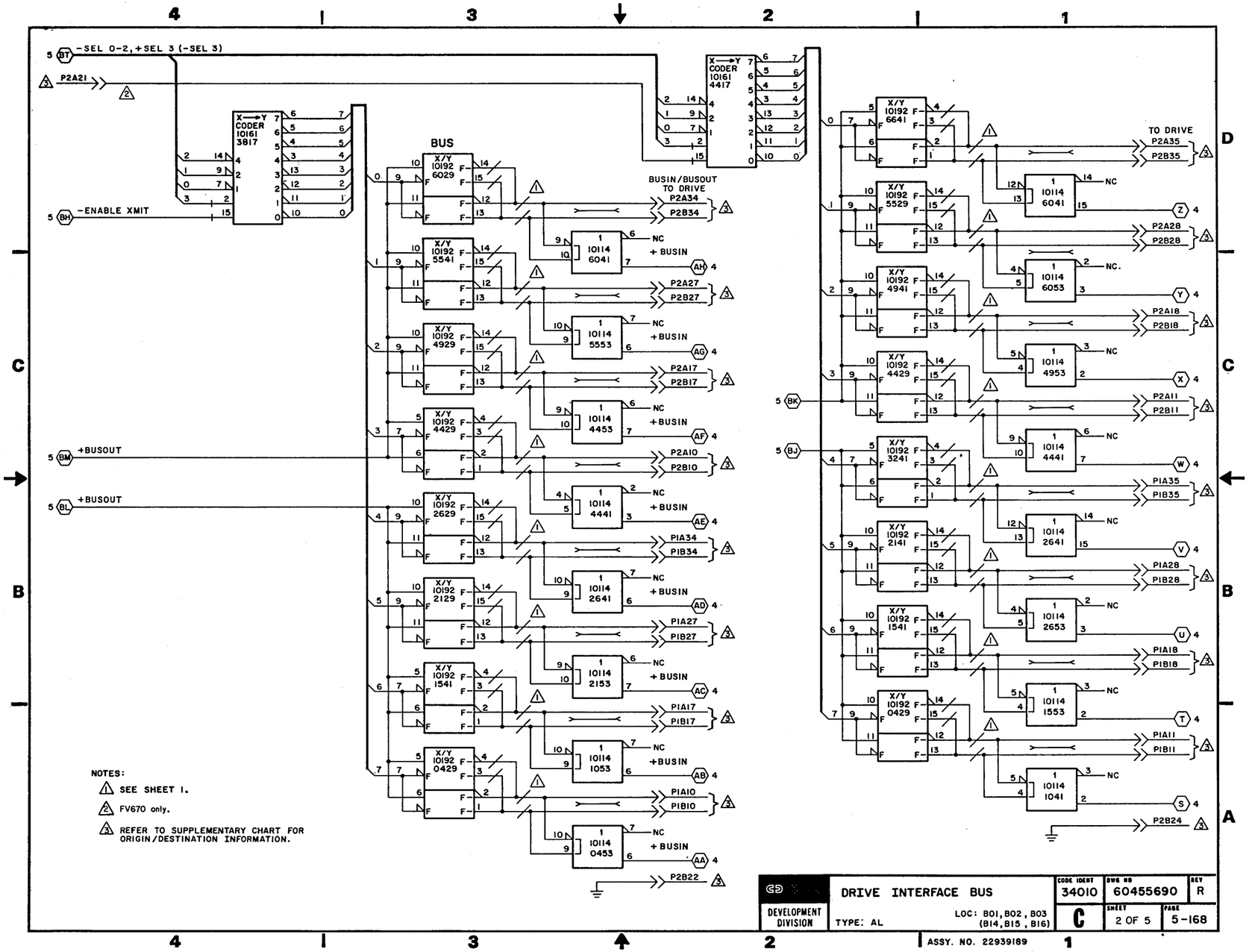

(NOC 7/13) +BUFF MODE SEL
AF P1A22
10110 1005
AH P2A43 -RAM WE
AD P2B12 -WRITE ENABLE
4 AV +RAM OR BUFF ADDR 2^12•2^10
4 AW +RAM OR BUFF ADDR 2^12
AD P1A34 +BMA 2^10
10104 6017
10195 5517
BUFF PAR ADDR RGTR
RGTR 10173 4917
3 K +BUFF ADDR 2^9
3 L +BUFF ADDR 2^8
3 M +BUFF ADDR 2^7
3 N +BUFF ADDR 2^6
3 P +BUFF ADDR 2^5
3 Q +BUFF ADDR 2^4
3 R +BUFF ADDR 2^3
3 S +BUFF ADDR 2^2
3 T +BUFF ADDR 2^1
3 U +BUFF ADDR 2^0
BUFFER PARITY
A1023 A0000
MEM 10415 0441
MEM 10415 1041
ACD AG
-5.2V
AJ (A24) P1B19 -PARITY DATA 2
+ENABLE EXTERNAL BUFF 4 P1A20 AJ (A26)
+ENABLE EXTERNAL BUFF 3 P1B20 AJ (A25)
+ENABLE EXTERNAL BUFF 2 P1B21 AJ (A24)
+ENABLE EXTERNAL BUFF 1 P1B22 AJ (A23)
P1A21 NC
AX 3
AY 4
10195 2653
3 +BUFF ADDR 2^10 P1A33 AJ, AK (A23-A27,3)
2 -BUFF PAR P1B33 AR (B20)
-BUFF PAR AZ 4

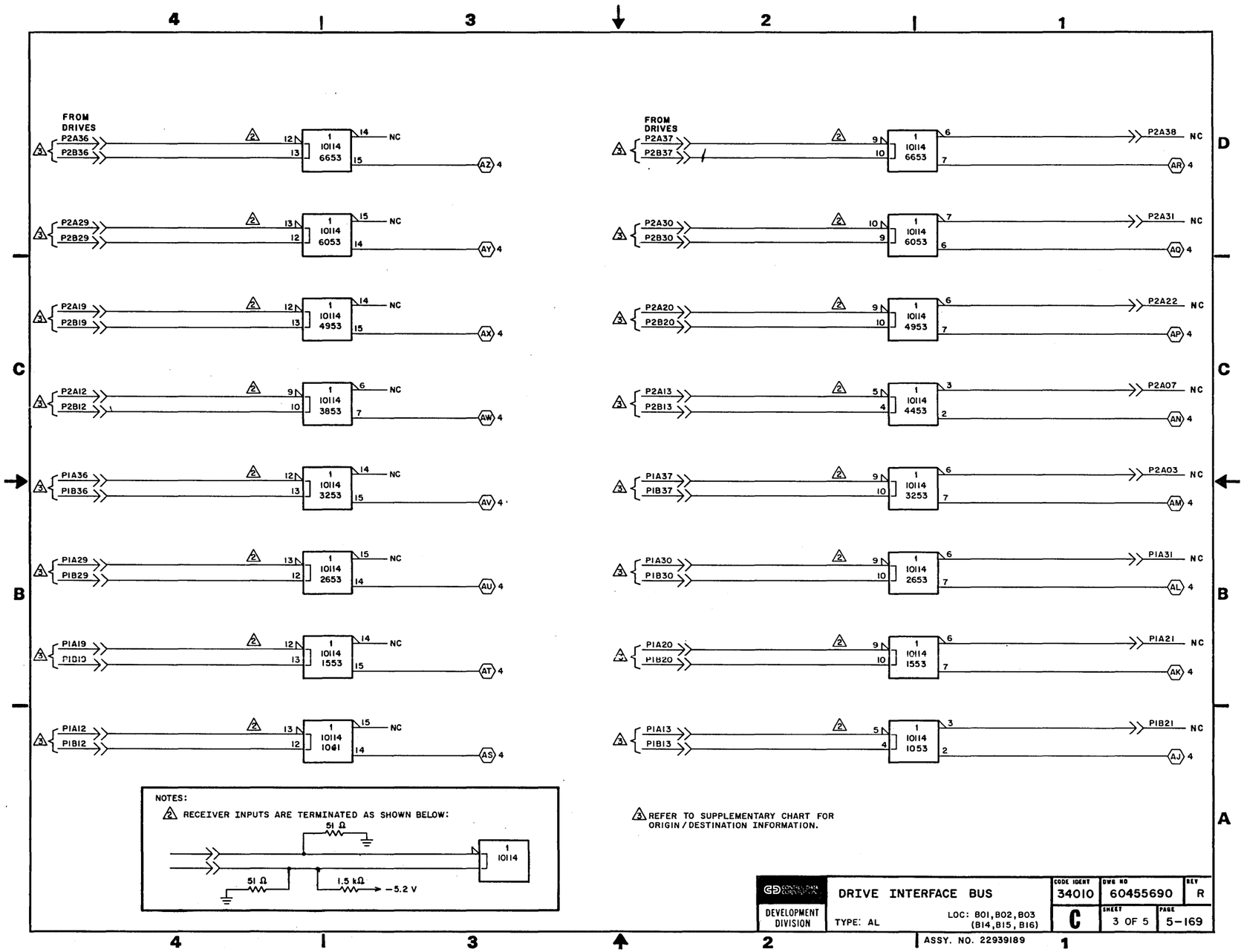
DEVELOPMENT DIVISION	PROGRAM ROM, PARITY RAM	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AK LOC: A27	C	SHEET 5 OF 7	PAGE 5-164
	ASSY. NO. 22939170			


4
1
3
2
1
D
C
B
A
7 BJ – ROM 2^11
7 CA – ROM 2^11
7 CS – ROM 2^11
7 DJ – ROM 2^11
7 BK – ROM 2^10
7 CB – ROM 2^10
7 CT – ROM 2^10
7 DK – ROM 2^10
7 BL – ROM 2^9
7 CC – ROM 2^9
7 CU – ROM 2^9
7 DL – ROM 2^9
7 BM – ROM 2^8
7 CD – ROM 2^8
7 CV – ROM 2^8
7 DM – ROM 2^8
7 BN – ROM 2^7
7 CE – ROM 2^7
7 CW – ROM 2^7
7 DN – ROM 2^7
7 BP – ROM 2^6
7 CF – ROM 2^6
7 CX – ROM 2^6
7 DP – ROM 2^6
7 BQ – ROM 2^5
7 CG – ROM 2^5
7 CY – ROM 2^5
7 DQ – ROM 2^5
7 BR – ROM 2^4
7 CH – ROM 2^4
7 CZ – ROM 2^4
7 DR – ROM 2^4
7 BS – ROM 2^3
7 CJ – ROM 2^3
7 DA – ROM 2^3
7 DS – ROM 2^3
7 BT – ROM 2^2
7 CK – ROM 2^2
7 DB – ROM 2^2
7 DT – ROM 2^2
7 BU – ROM 2^1
7 CL – ROM 2^1
7 DC – ROM 2^1
7 DU – ROM 2^1
7 BV – ROM 2^0
7 CM – ROM 2^0
7 DD – ROM 2^0
7 DV – ROM 2^0
HI
=1
10195
3253
DATA
15 –ROM 11 P1B42
2 –ROM 10 P1A40
4 –ROM 9 P1A37
3 –ROM 8 P1A38
14 –ROM 7 P1A41
13 –ROM 6 P1B41
AJ (A24)
AJ (A25)
=1
10195
3853
4 –ROM 5 P2B09
3 –ROM 4 P1B40
14 –ROM 3 P2B07
2 –ROM 2 P1B35
13 –ROM 1 P2B08
15 –ROM 0 P2A03
AJ (A26)
NC
=1
10195
5517
3
HI
7 BE –ROM 2^15
7 BW –ROM 2^15
7 CN –ROM 2^15
7 DE –ROM 2^15
7 BF –ROM 2^14
7 BX –ROM 2^14
7 CP –ROM 2^14
7 DF –ROM 2^14
7 BG –ROM 2^13
7 BY –ROM 2^13
7 CQ –ROM 2^13
7 DG –ROM 2^13
7 BH –ROM 2^12
7 BZ –ROM 2^12
7 CR –ROM 2^12
7 DH –ROM 2^12
HI
=
10195
2653
ROM DATA
15 –ROM 15 P1A36
14 –ROM 14 P1A35
4 –ROM 13 P1B32
13 –ROM 12 P1B34
AJ (A23)
CHIP SELECTOR
X→Y CODER 10161 1541
NC
NC
NC
NC
BA 7
BB 7
BC 7
BD 7
3 DW + ROM ADDR 2^9
3 DX + ROM ADDR 2^8
1 B – ADDR 2^13
ROM PARITY
X→Y
G7
G0
MUX
10164
1529
NC
NC
NC
NC
15 –ROM PARITY P1D22 AK
PROGRAM ROM
3 X + ROM ADDR 2^7
3 AA + ROM ADDR 2^6
3 AD + ROM ADDR 2^5
3 AG + ROM ADDR 2^4
3 AK + ROM ADDR 2^3
3 AN + ROM ADDR 2^2
3 AR + ROM ADDR 2^1
3 AU + ROM ADDR 2^0
A255
A000
MEM
10149
1517
AG
AG
AG
AG
GD DEVELOPMENT DIVISION
PROGRAM ROM, PARITY RAM
TYPE: AK LOC: A27
ASSY. NO. 22939170
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 6 OF 7
PAGE 5-165


PROGRAM ROM
+ROM ADDR 2^7
+ROM ADDR 2^6
+ROM ADDR 2^5
+ROM ADDR 2^4
+ROM ADDR 2^3
+ROM ADDR 2^2
+ROM ADDR 2^1
+ROM ADDR 2^0
-ROM GATE
X → Y
128
64
32
16
8
4
2
1
A255
A000
MEM
10149
2605
2617
2629
2641
-ROM 2^15
-ROM 2^14
-ROM 2^13
-ROM 2^12
-ROM 2^11
-ROM 2^10
-ROM 2^9
-ROM 2^8
-ROM 2^7
-ROM 2^6
-ROM 2^5
-ROM 2^4
-ROM 2^3
-ROM 2^2
-ROM 2^1
-ROM 2^0
3205
3805
4405
3217
3817
4417
3229
3829
4429
3241
3841
4441
DEVELOPMENT DIVISION
PROGRAM ROM, PARITY RAM
TYPE: AK
LOC: A27
ASSY. NO. 22939170
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 7 OF 7
PAGE 5-166


-SEL 0-2, +SEL 3 (-SEL 3)
-ENABLE XMIT
+BUSOUT
+BUSOUT
+BUSOUT
+BUSOUT
CODER 10161 3217
CODER 10161 2617
BUS
BUSIN / BUSOUT TO DRIVE
P2A32
P2B32
P2A25
P2B25
P2A15
P2B15
P2A08
P2B08
P1A32
P1B32
P1A25
P1B25
P1A15
P1B15
P1A08
P1B08
P1A43
X/Y 10192 6641
X/Y 10192 5529
X/Y 10192 4929
X/Y 10192 3841
X/Y 10192 3241
X/Y 10192 2129
X/Y 10192 1029
X/Y 10192 0441
10114 6653
10114 5553
10114 4453
10114 3853
10114 3253
10114 2153
10114 1053
10114 0453
+BUSIN
NC
BUS
BUSIN / BUSOUT TO DRIVE
P2A33
P2B33
P2A26
P2B26
P2A16
P2B16
P2A09
P2B09
P1A33
P1B33
P1A26
P1B26
P1A16
P1B16
P1A09
P1B09
P1A43
X/Y 10192 6029
X/Y 10192 5541
X/Y 10192 4941
X/Y 10192 3841
X/Y 10192 2629
X/Y 10192 2141
X/Y 10192 1029
X/Y 10192 0441
10114 6041
10114 5553
10114 4441
10114 3853
10114 2641
10114 2153
10114 1041
10114 0453
+BUSIN
NC
NOTES:
I/O LINES ARE TERMINATED AS SHOWN BELOW. THESE LINES ARE BI-DIRECTIONAL.
X/Y 10192
51 Ω
1.5 kΩ
51 Ω
-5.2 V
REFER TO SUPPLEMENTARY CHART FOR ORIGIN/DESTINATION INFORMATION.
DRIVE INTERFACE BUS
DEVELOPMENT DIVISION
TYPE: AL
LOC: B01, B02, B03 (B14, B15, B16)
ASSY. NO. 22939189
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 1 OF 5
PAGE 5-167


-SEL 0-2, +SEL 3 (-SEL 3)
P2A21
-ENABLE XMIT
+BUSOUT
+BUSOUT
BUS
X→Y CODER 10161 3817
X→Y CODER 10161 4417
BUSIN/BUSOUT TO DRIVE
P2A34
P2B34
P2A27
P2B27
P2A17
P2B17
P2A10
P2B10
P1A34
P1B34
P1A27
P1B27
P1A17
P1B17
P1A10
P1B10
P2B22
+BUSIN
NC
TO DRIVE
P2A35
P2B35
P2A28
P2B28
P2A18
P2B18
P2A11
P2B11
P1A35
P1B35
P1A28
P1B28
P1A18
P1B18
P1A11
P1B11
P2B24
NOTES:
1. SEE SHEET 1.
2. FV670 only.
3. REFER TO SUPPLEMENTARY CHART FOR ORIGIN/DESTINATION INFORMATION.
DRIVE INTERFACE BUS
DEVELOPMENT DIVISION
TYPE: AL
LOC: B01, B02, B03 (B14, B15, B16)
ASSY. NO. 22939189
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 5
PAGE 5-168



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

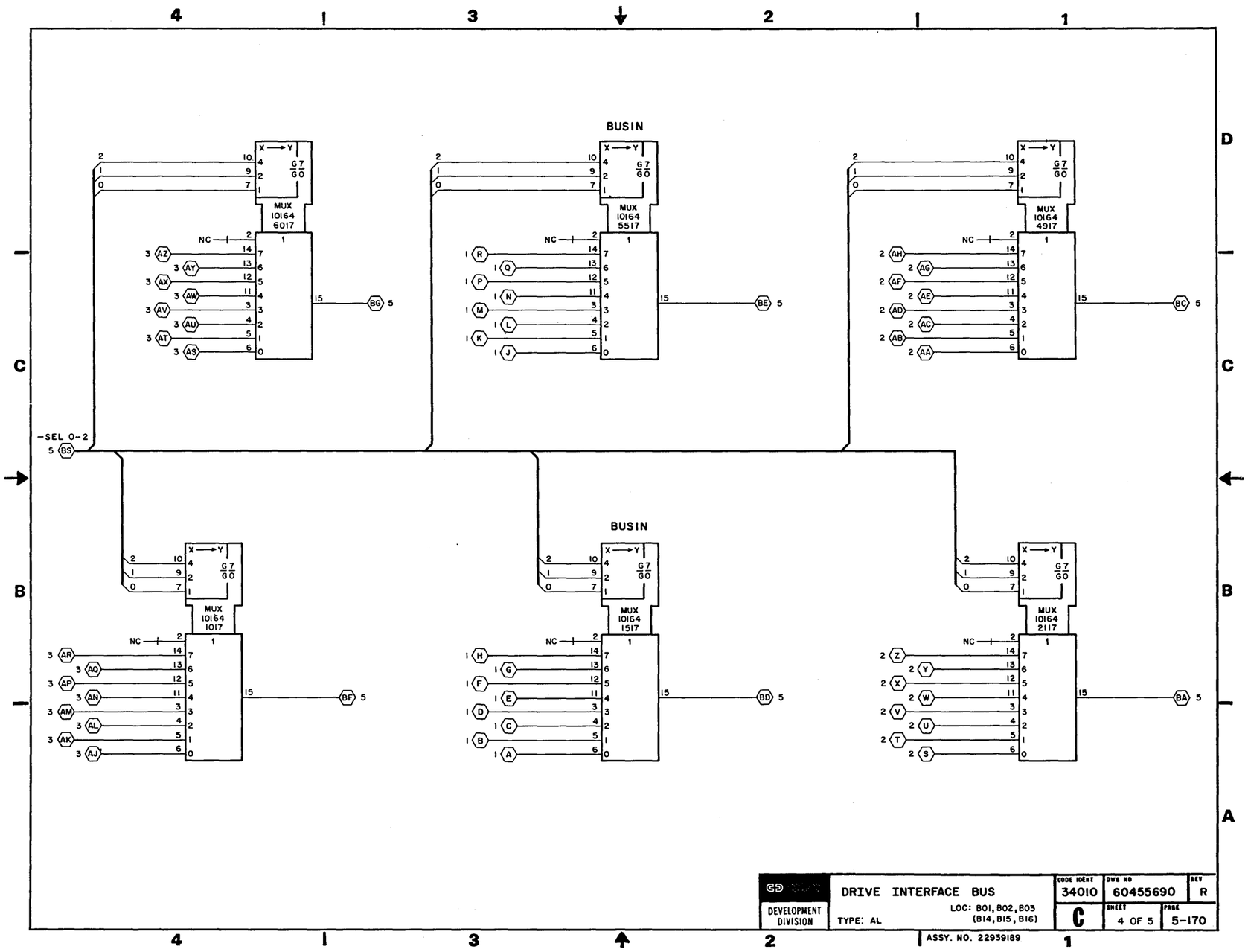
DRIVE INTERFACE BUS

TYPE: AL

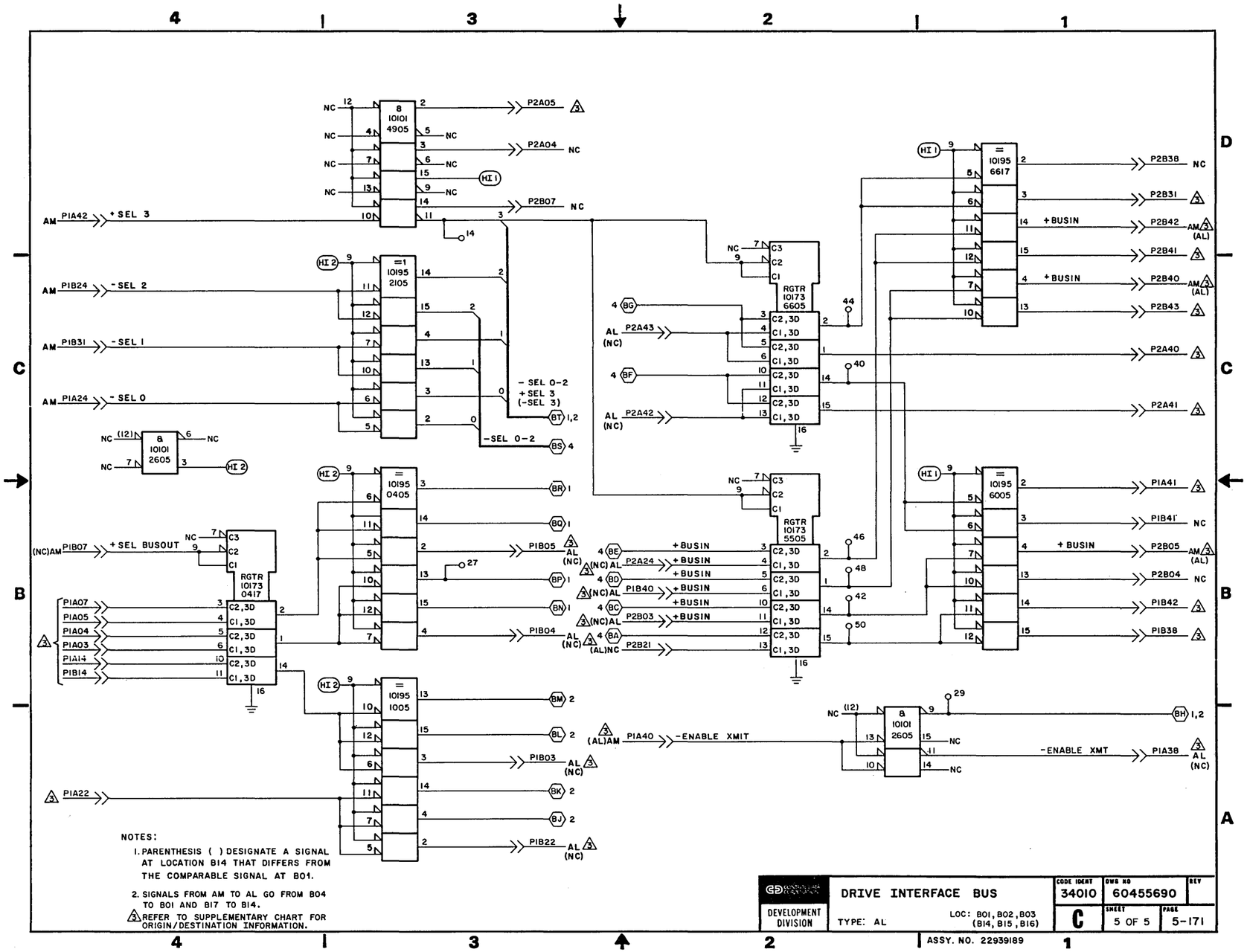
LOC: B01,B02,B03 (B14,B15,B16)

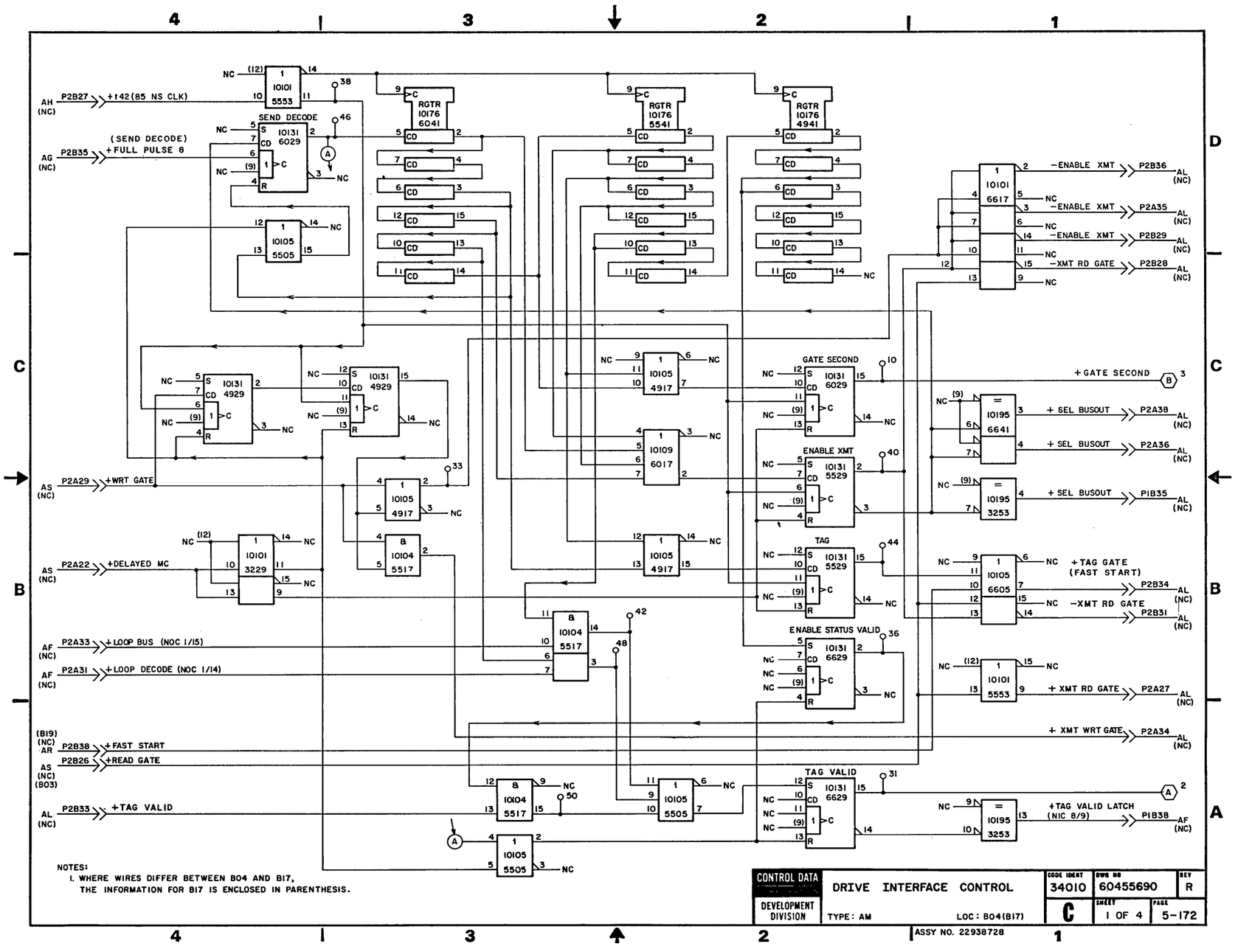
ASSY. NO. 22939189

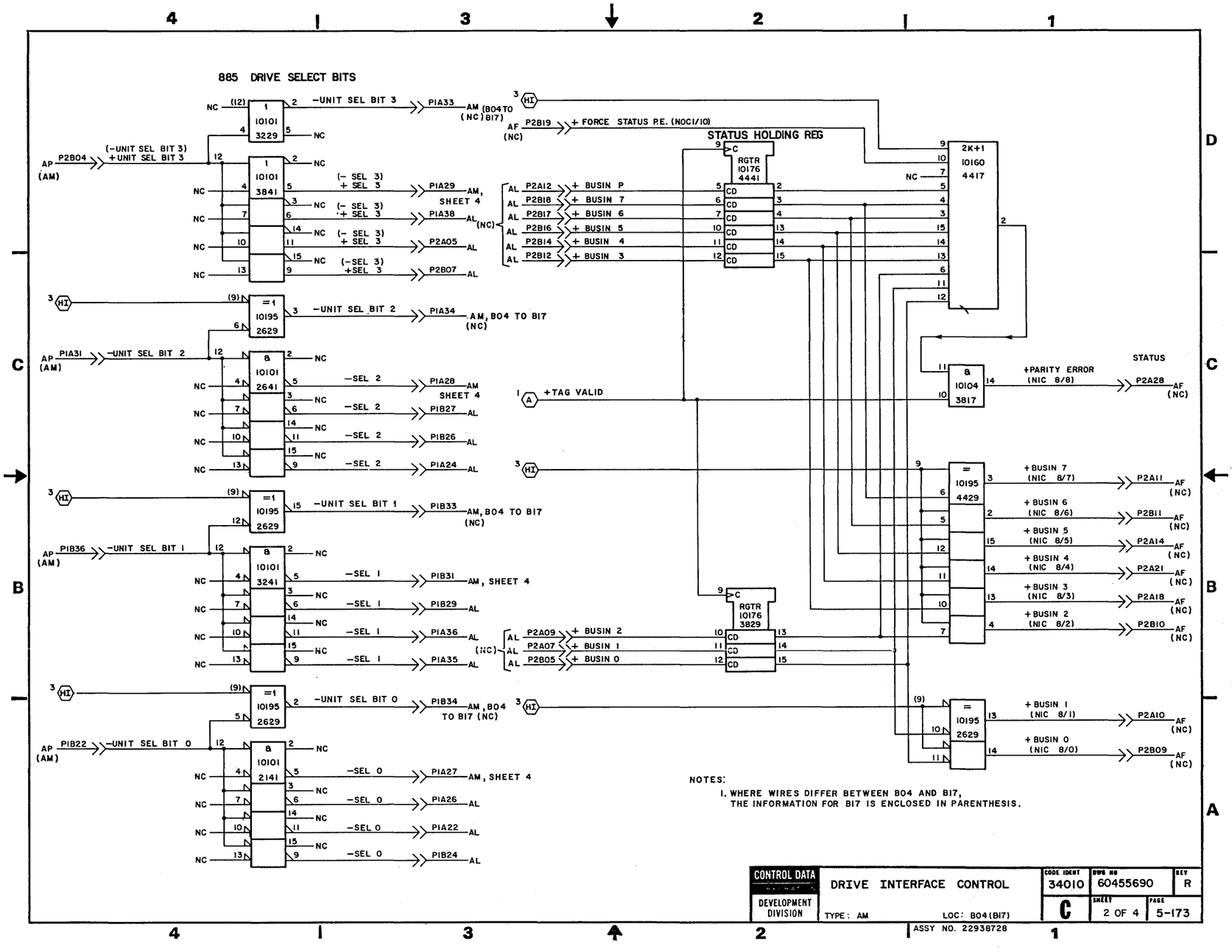
CODE IDENT	DWG NO	REV
34010	60455690	R
C	SHEET 3 OF 5	PAGE 5-169

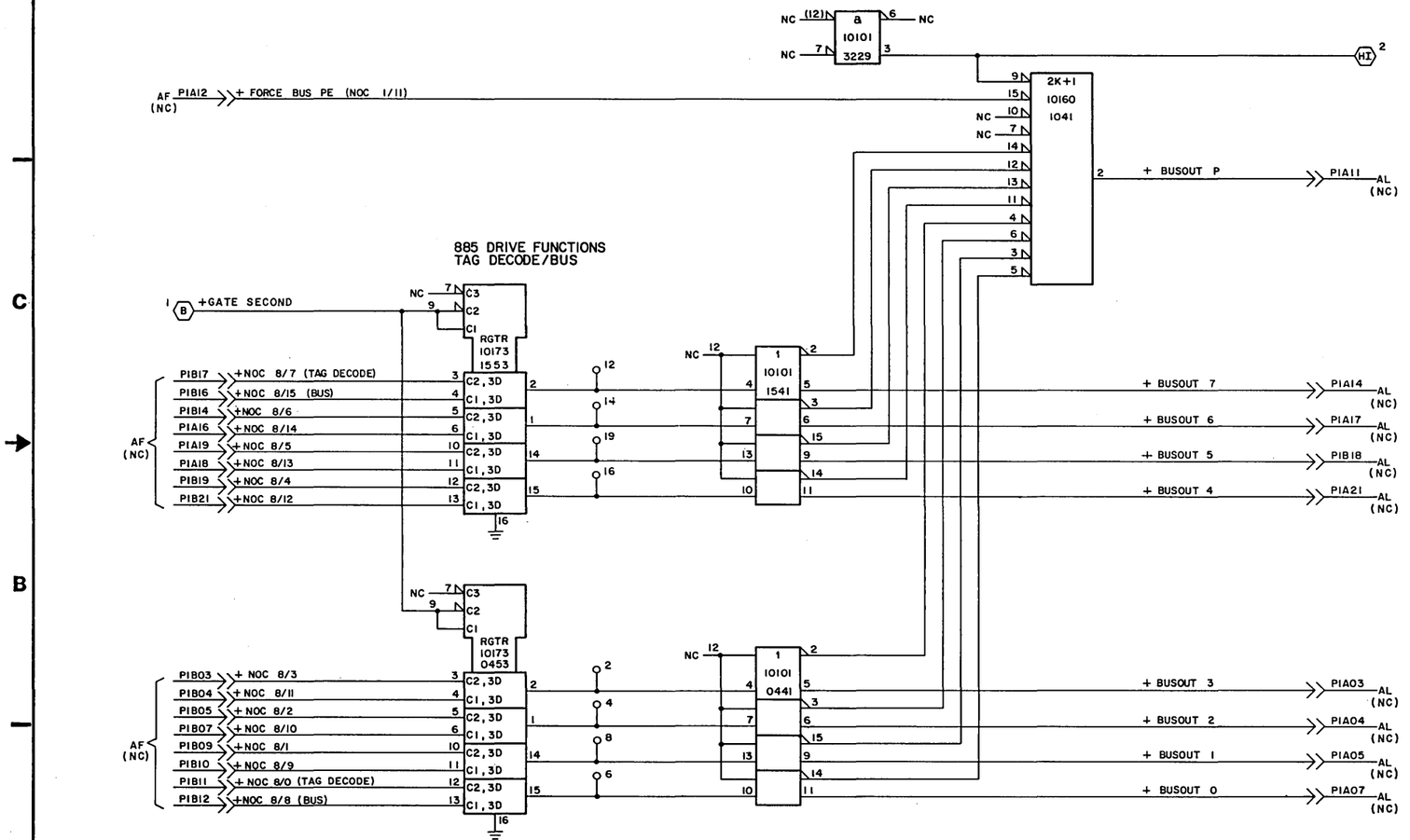


GD DEVELOPMENT DIVISION	DRIVE INTERFACE BUS TYPE: AL LOC: B01, B02, B03 (B14, B15, B16)	CODE IDENT 34010	DWG NO 60455690	REV R
	ASSY. NO. 22939189	C	SHEET 4 OF 5	PAGE 5-170


4
3
2
1
D
C
B
A
8 10101 4905
=1 10195 2105
8 10101 2605
=1 10195 0405
=1 10195 1005
RGTR 10173 0417
RGTR 10173 6605
RGTR 10173 5505
= 10195 6617
= 10195 6005
AM P1A42 + SEL 3
AM P1B24 - SEL 2
AM P1B31 - SEL 1
AM P1A24 - SEL 0
(NC)AM P1B07 + SEL BUSOUT
P2A05
P2A04
P2B07
- SEL 0-2 + SEL 3 (-SEL 3)
-SEL 0-2
AL P2A43 (NC)
AL P2A42 (NC)
+BUSIN
AM (AL)
P2B38
P2B31
P2B42
P2B41
P2B43
P2A40
P2A41
P1A41
P1B41
P2B05
P2B04
P1B42
P1B38
P1A22
P1B03
P1B04
P1B05
(AL)AM P1A40 -ENABLE XMIT
-ENABLE XMT
P1A38
NOTES:
1. PARENTHESIS ( ) DESIGNATE A SIGNAL AT LOCATION B14 THAT DIFFERS FROM THE COMPARABLE SIGNAL AT B01.
2. SIGNALS FROM AM TO AL GO FROM B04 TO B01 AND B17 TO B14.
3 REFER TO SUPPLEMENTARY CHART FOR ORIGIN/DESTINATION INFORMATION.
DEVELOPMENT DIVISION
DRIVE INTERFACE BUS
TYPE: AL
LOC: B01, B02, B03 (B14, B15, B16)
CODE IDENT 34010
DWG NO 60455690
REV
C
SHEET 5 OF 5
PAGE 5-171
ASSY. NO. 22939189


AH (NC) P2B27 +f42(85 NS CLK)
AG (NC) P2B35 (SEND DECODE) +FULL PULSE 8
AS (NC) P2A29 +WRT GATE
AS (NC) P2A22 +DELAYED MC
AF (NC) P2A33 +LOOP BUS (NOC 1/15)
AF (NC) P2A31 +LOOP DECODE (NOC 1/14)
(B19) (NC) AR P2B38 +FAST START
AS (NC) (B03) P2B26 +READ GATE
AL (NC) P2B33 +TAG VALID
SEND DECODE
GATE SECOND
ENABLE XMT
TAG
ENABLE STATUS VALID
TAG VALID
-ENABLE XMT P2B36
-ENABLE XMT P2A35
-ENABLE XMT P2B29
-XMT RD GATE P2B28
+GATE SECOND
+SEL BUSOUT P2A38
+SEL BUSOUT P2A36
+SEL BUSOUT P1B35
+TAG GATE (FAST START) P2B34
-XMT RD GATE P2B31
+XMT RD GATE P2A27
+XMT WRT GATE P2A34
+TAG VALID LATCH (NIC 8/9) P1B38
RGTR 10176 6041
RGTR 10176 5541
RGTR 10176 4941
10101 5553
10105 5505
10131 4929
10105 4917
10109 6017
10131 6029
10131 5529
10131 6629
10101 6617
10195 6641
10195 3253
10101 3229
10104 5517
10105 6605
NOTES:
1. WHERE WIRES DIFFER BETWEEN B04 AND B17, THE INFORMATION FOR B17 IS ENCLOSED IN PARENTHESIS.
CONTROL DATA
DEVELOPMENT DIVISION
DRIVE INTERFACE CONTROL
TYPE: AM
LOC: B04(B17)
ASSY NO. 22938728
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
SHEET 1 OF 4
PAGE 5-172

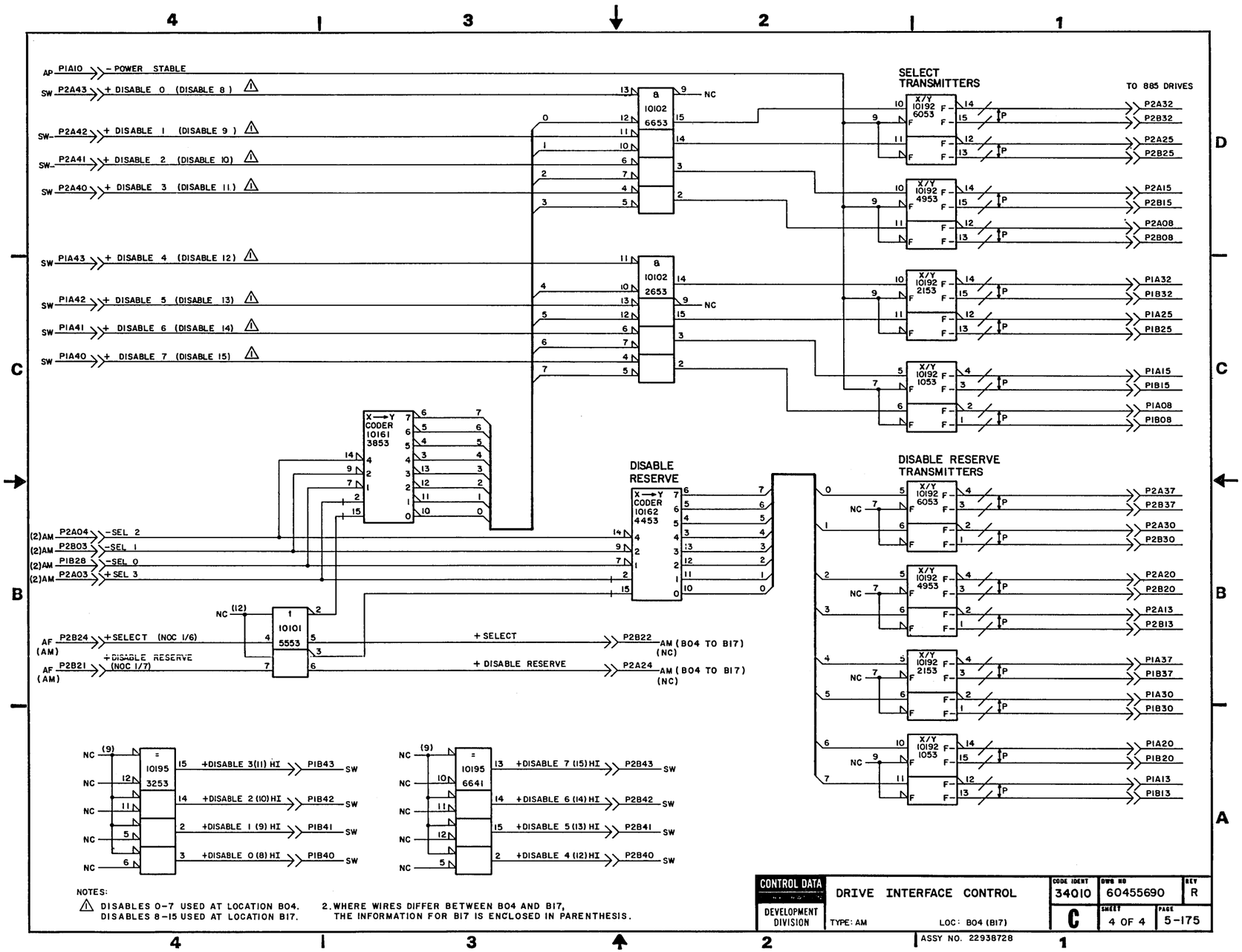

885 DRIVE SELECT BITS
STATUS HOLDING REG
-UNIT SEL BIT 3
-UNIT SEL BIT 2
-UNIT SEL BIT 1
-UNIT SEL BIT 0
+FORCE STATUS P.E. (NOC1/10)
+TAG VALID
+PARITY ERROR (NIC 8/8)
+BUSIN 7 (NIC 8/7)
+BUSIN 6 (NIC 8/6)
+BUSIN 5 (NIC 8/5)
+BUSIN 4 (NIC 8/4)
+BUSIN 3 (NIC 8/3)
+BUSIN 2 (NIC 8/2)
+BUSIN 1 (NIC 8/1)
+BUSIN 0 (NIC 8/0)
STATUS
NOTES:
1. WHERE WIRES DIFFER BETWEEN B04 AND B17, THE INFORMATION FOR B17 IS ENCLOSED IN PARENTHESIS.
CONTROL DATA
DEVELOPMENT DIVISION
DRIVE INTERFACE CONTROL
TYPE: AM
LOC: B04(B17)
ASSY NO. 22938728
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
SHEET 2 OF 4
PAGE 5-173



NOTES:

1. WHERE WIRES DIFFER BETWEEN B04 AND B17, THE INFORMATION FOR B17 IS ENCLOSED IN PARENTHESIS.

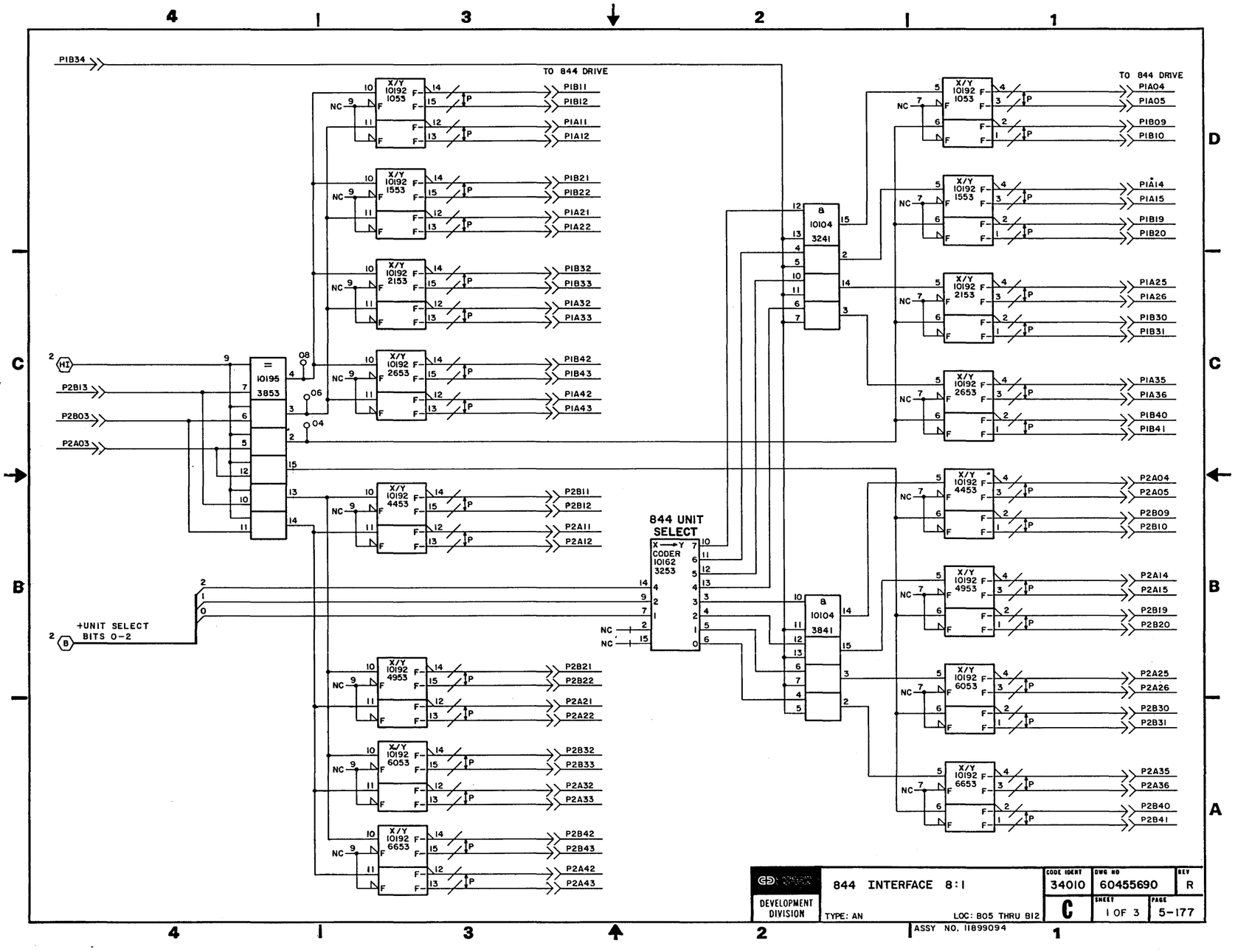
CONTROL DATA DEVELOPMENT DIVISION	DRIVE INTERFACE CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AM LOC: B04 (B17)	C	SHEET 3 OF 4	PAGE 5-174
	ASSY NO. 22938728			

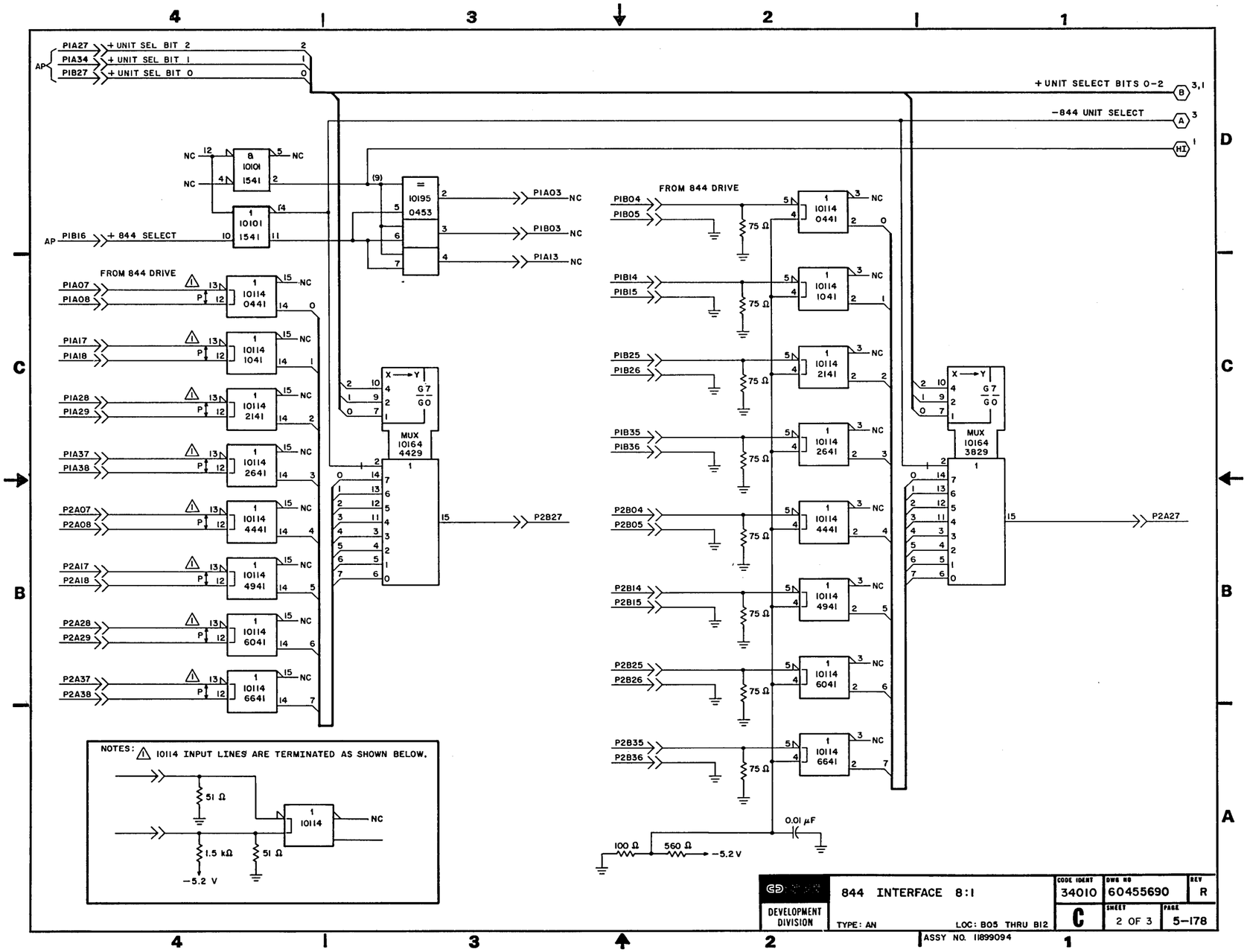

SELECT TRANSMITTERS
TO 885 DRIVES
DISABLE RESERVE
DISABLE RESERVE TRANSMITTERS
AP P1A10 - POWER STABLE
SW P2A43 + DISABLE 0 (DISABLE 8)
SW P2A42 + DISABLE 1 (DISABLE 9)
SW P2A41 + DISABLE 2 (DISABLE 10)
SW P2A40 + DISABLE 3 (DISABLE 11)
SW P1A43 + DISABLE 4 (DISABLE 12)
SW P1A42 + DISABLE 5 (DISABLE 13)
SW P1A41 + DISABLE 6 (DISABLE 14)
SW P1A40 + DISABLE 7 (DISABLE 15)
(2)AM P2A04 -SEL 2
(2)AM P2B03 -SEL 1
(2)AM P1B28 -SEL 0
(2)AM P2A03 +SEL 3
AF (AM) P2B24 +SELECT (NOC 1/6)
AF (AM) P2B21 +DISABLE RESERVE (NOC 1/7)
+SELECT
+DISABLE RESERVE
P2B22 AM (B04 TO B17) (NC)
P2A24 AM (B04 TO B17) (NC)
8 10102 6653
8 10102 2653
X→Y CODER 10161 3853
X→Y CODER 10162 4453
10101 5553
= 10195 3253
= 10195 6641
X/Y 10192 6053
X/Y 10192 4953
X/Y 10192 2153
X/Y 10192 1053
P2A32 P2B32 P2A25 P2B25
P2A15 P2B15 P2A08 P2B08
P1A32 P1B32 P1A25 P1B25
P1A15 P1B15 P1A08 P1B08
P2A37 P2B37 P2A30 P2B30
P2A20 P2B20 P2A13 P2B13
P1A37 P1B37 P1A30 P1B30
P1A20 P1B20 P1A13 P1B13
+DISABLE 3(11) HI P1B43 SW
+DISABLE 2 (10) HI P1B42 SW
+DISABLE 1 (9) HI P1B41 SW
+DISABLE 0 (8) HI P1B40 SW
+DISABLE 7 (15) HI P2B43 SW
+DISABLE 6 (14) HI P2B42 SW
+DISABLE 5 (13) HI P2B41 SW
+DISABLE 4 (12) HI P2B40 SW
NOTES:
1. DISABLES 0-7 USED AT LOCATION B04. DISABLES 8-15 USED AT LOCATION B17.
2. WHERE WIRES DIFFER BETWEEN B04 AND B17, THE INFORMATION FOR B17 IS ENCLOSED IN PARENTHESIS.
CONTROL DATA
DEVELOPMENT DIVISION
DRIVE INTERFACE CONTROL
TYPE: AM
LOC: B04 (B17)
ASSY NO. 22938728
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET C
4 OF 4
PAGE 5-175

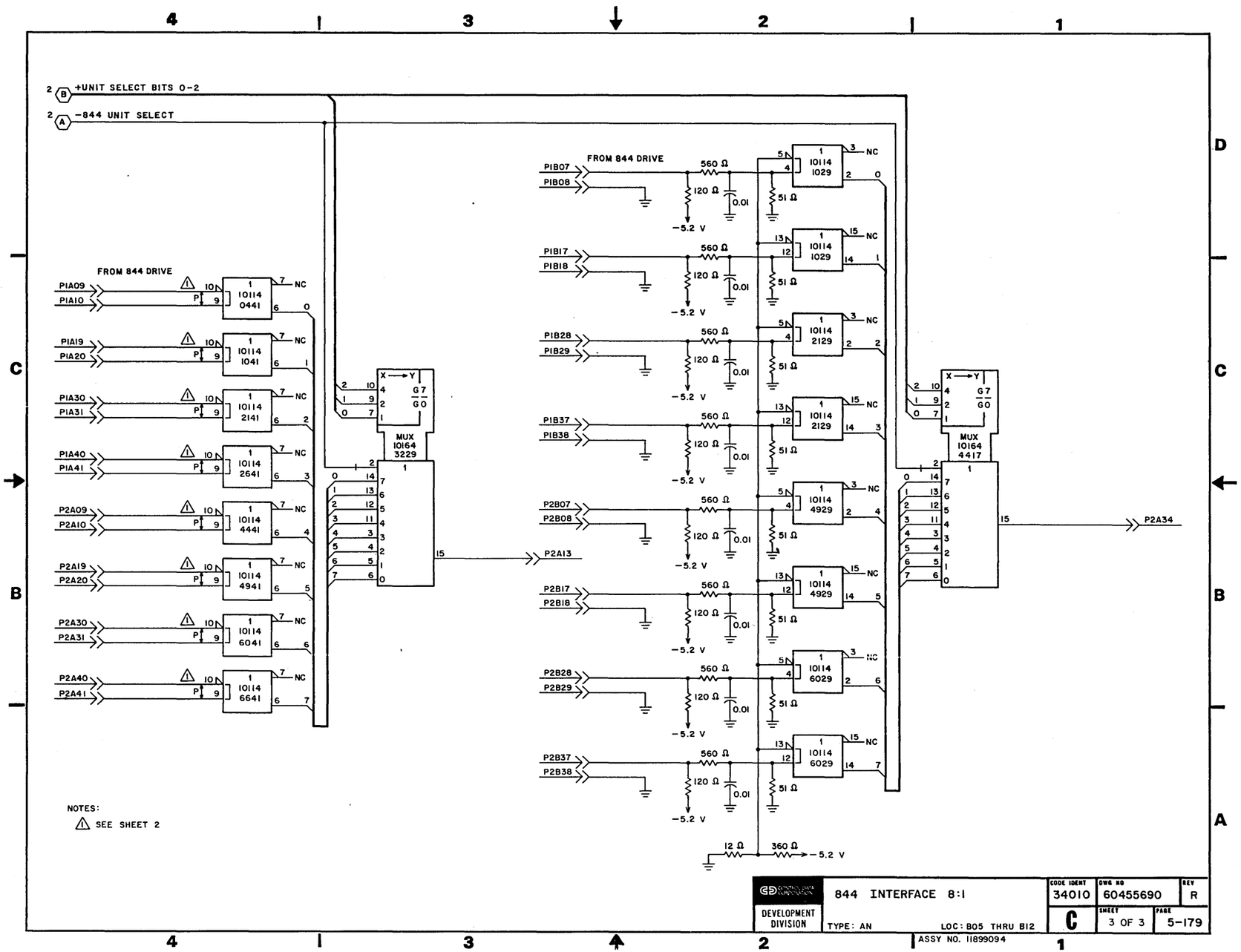
844 INTERFACE 8:1
SIGNAL NAME CHART (ALL SIGNALS ARE POSITIVE POLARITY)

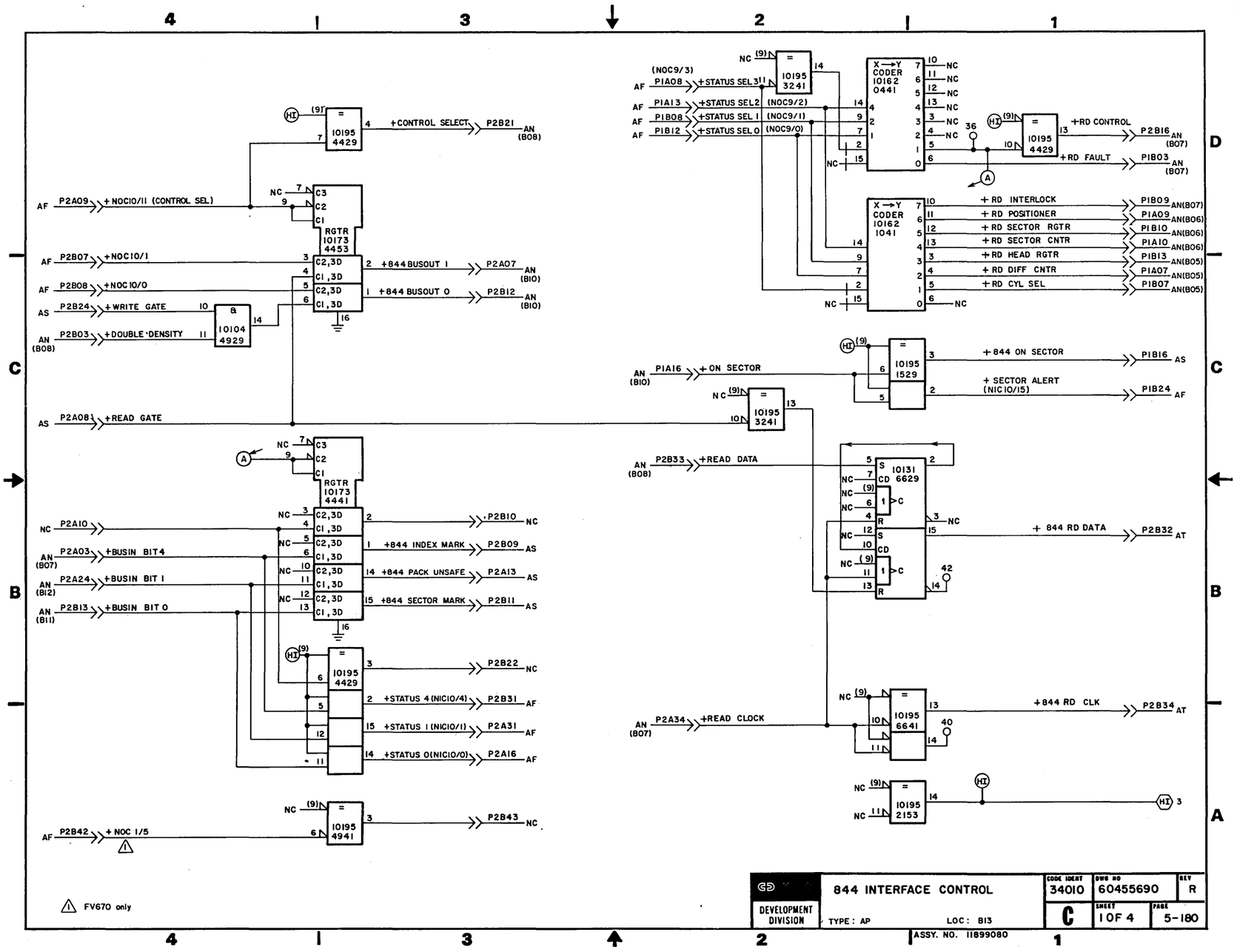
	CONNECTOR PIN	LOCATION B05 SIGNAL NAME	ORIGIN	LOCATION B06 SIGNAL NAME	ORIGIN	LOCATION B07 SIGNAL NAME	ORIGIN	LOCATION B08 SIGNAL NAME	ORIGIN	LOCATION B09 SIGNAL NAME	ORIGIN	LOCATION B10 SIGNAL NAME	ORIGIN	LOCATION B11 SIGNAL NAME	ORIGIN	LOCATION B12 SIGNAL NAME	
Sheet 1	P1B34	NC		WRITE CLOCK OUT	AT	DATA OUT 0-7	AT	CLEAR OPPOSITE CHANNEL RESERVE 0-7 (NOC 9/4)	AF	RELEASE 0-7 (NOC 9/5)	AF	CLEAR FAULT 0-7 (NOC 9/6)	AF	EQUIP. SEL 0-7 (NOC 10/10)	AF	BUSOUT BIT 9 0-7 (NOC 10/9)	AF
	P2B13	RD. DIFF. CNTR. 0-7	AP	RD. SECTOR RGTR	AP	RD. FAULT	AP	CONTROL SELECT 0-7	AP	CYLINDER SELECT 0-7 (NOC 10/14)	AF	844 BUSOUT BIT 1 0-7		BUSOUT BIT 4 0-7 (NOC 10/4)	AF	BUSOUT BIT 7 0-7 (NOC 10/7)	AF
	P2B03	RD. CYL SELECT	AP	RD. SECTOR CNTR. 0-7	AP	RD. INTERLOCK 0-7	AP	NC		HEAD SELECT 0-7 (NOC 10/13)	AF	844 BUSOUT BIT 0 0-7	AP	BUSOUT BIT 3 0-7 (NOC 10/3)	AF	BUSOUT BIT 6 0-7 (NOC 10/6)	
	P2A03	RD. HEAD RGTR 0-7	AP	RD. POSITIONER 0-7	AP	RD. CONTROL 0-7	AP	UNIT SELECTED 0-7 (NOC 10/12)	AF	DIFFERENCE SELECT 0-7 (NOC 10/15)	AF	BUSOUT BIT 2 0-7 (NOC 10/2)	AF	BUSOUT BIT 5 0-7 (NOC 10/5)	AF	BUSOUT BIT 8 0-7 (NOC 10/8)	AF
Sheet 2	P2B27	NC		UNIT SELECTED 0-7 (NIC 10/12)	AF	UNIT BUSY 0-7 (NIC 10/13)	AF	UNIT READY 0-7 (NIC 10/11)	AF	SEEK ERROR 0-7 (NIC 10/14)	AF	ON SECTOR 0-7	AP	BUSIN BIT 0 0-7	AP	BUSIN BIT 1 0-7	AP
	P2A27	NC		844 WRT CLOCK 0-7	AT	READ CLOCK 0-7	AP	READ DATA 0-7	AP	NC		NC		NC		NC	
Sheet 3	P2A13	BUSIN BIT 2 0-7 (NIC 10/2)	AF	BUSIN BIT 3 0-7 (NIC 10/3)	AF	BUSIN BIT 4 0-7	AP	BUSIN BIT 5 0-7 (NIC 10/5)	AF	BUSIN BIT 6 0-7 (NIC 10/6)	AF	BUSIN BIT 7 0-7 (NIC 10/7)	AF	BUSIN BIT 8 0-7 (NIC 10/8)	AF	BUSIN BIT 9 0-7 (N/C 10/9)	AF
	P2A34	NC		NC		ON LINE 0-7 (NIC 10/10)	AF	DOUBLE DENSITY 0-7	AP	NC		NC		NC		NC	

NOTE: SEE DRIVE INTERFACE CABLE ASSEMBLY IN SECTION 8 TO SEE CONNECTOR BLOCK PIN ASSIGNMENTS.

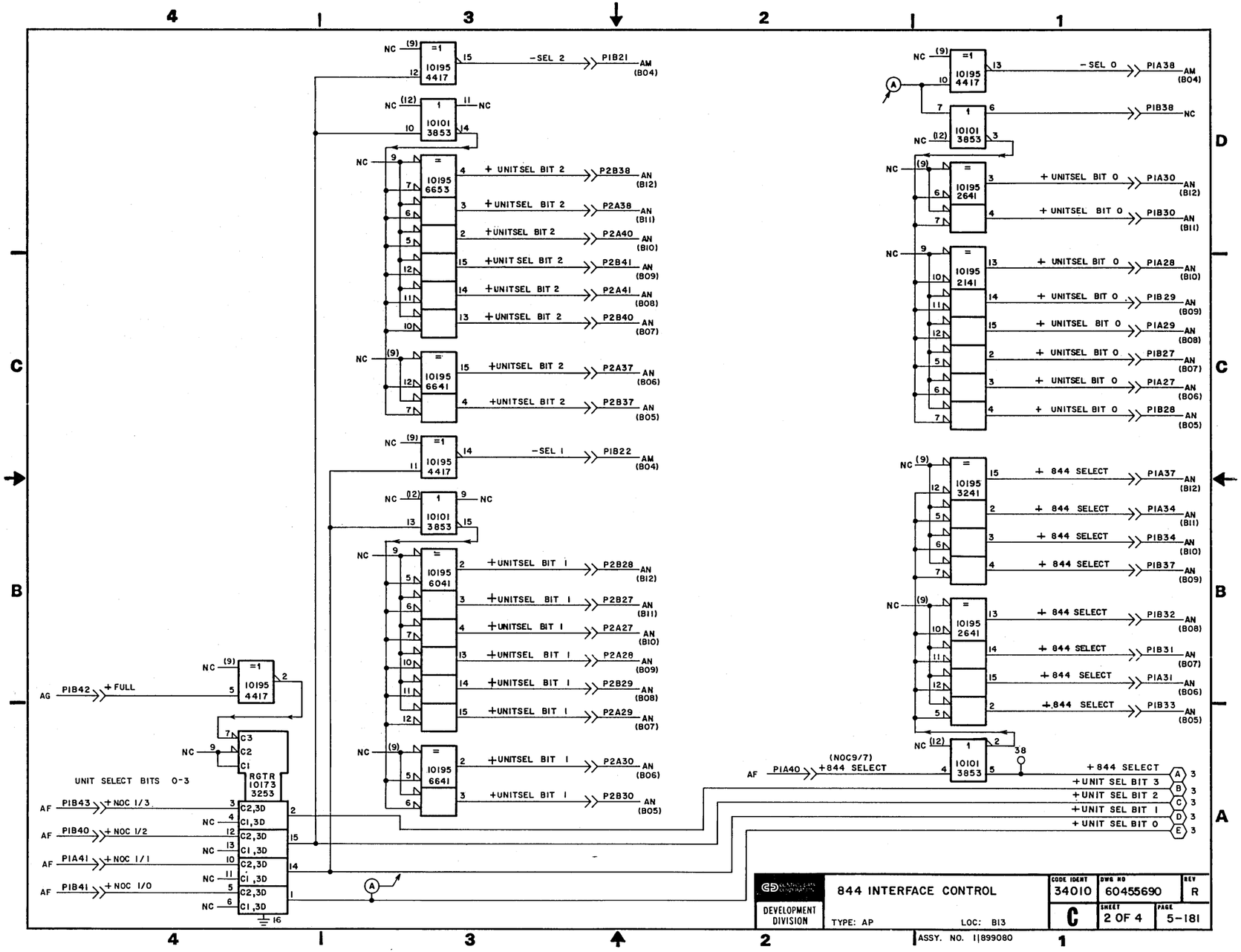

TO 844 DRIVE
PIB34
X/Y 10192 1053
PIB11
PIB12
PIA11
PIA12
X/Y 10192 1553
PIB21
PIB22
PIA21
PIA22
X/Y 10192 2153
PIB32
PIB33
PIA32
PIA33
X/Y 10192 2653
PIB42
PIB43
PIA42
PIA43
= 10195 3853
P2B13
P2B03
P2A03
X/Y 10192 4453
P2B11
P2B12
P2A11
P2A12
X/Y 10192 4953
P2B21
P2B22
P2A21
P2A22
X/Y 10192 6053
P2B32
P2B33
P2A32
P2A33
X/Y 10192 6653
P2B42
P2B43
P2A42
P2A43
+UNIT SELECT BITS 0-2
844 UNIT SELECT
X→Y CODER 10162 3253
8 10104 3241
8 10104 3841
TO 844 DRIVE
X/Y 10192 1053
PIA04
PIA05
PIB09
PIB10
X/Y 10192 1553
PIA14
PIA15
PIB19
PIB20
X/Y 10192 2153
PIA25
PIA26
PIB30
PIB31
X/Y 10192 2653
PIA35
PIA36
PIB40
PIB41
X/Y 10192 4453
P2A04
P2A05
P2B09
P2B10
X/Y 10192 4953
P2A14
P2A15
P2B19
P2B20
X/Y 10192 6053
P2A25
P2A26
P2B30
P2B31
X/Y 10192 6653
P2A35
P2A36
P2B40
P2B41
DEVELOPMENT DIVISION
844 INTERFACE 8:1
TYPE: AN
LOC: B05 THRU B12
ASSY NO. 11899094
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 3
PAGE 5-177

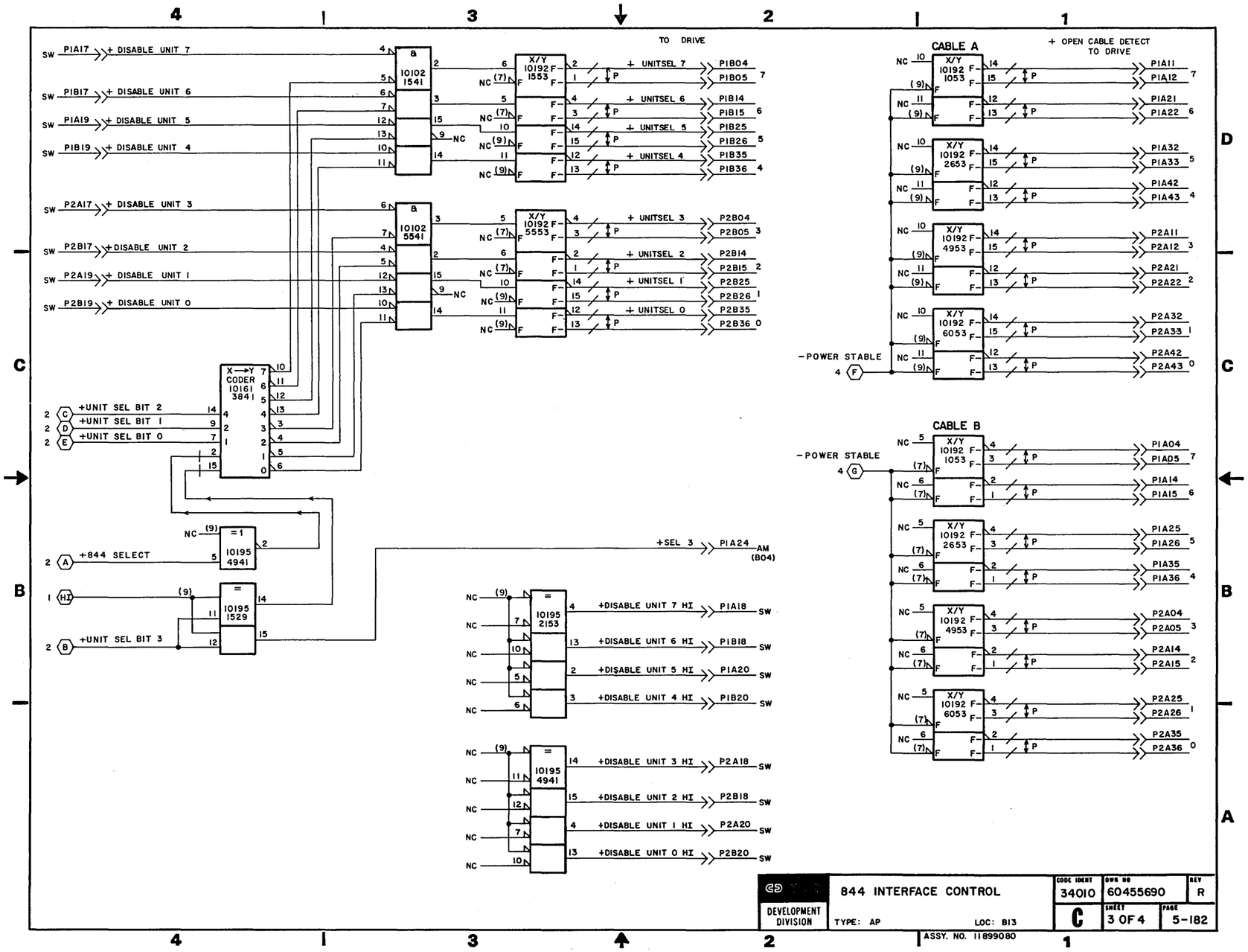

+ UNIT SEL BIT 2
+ UNIT SEL BIT 1
+ UNIT SEL BIT 0
+ UNIT SELECT BITS 0-2
-844 UNIT SELECT
+ 844 SELECT
FROM 844 DRIVE
MUX 10164 4429
MUX 10164 3829
75 Ω
0.01 μF
100 Ω
560 Ω
-5.2 V
NOTES: ⚠ 10114 INPUT LINES ARE TERMINATED AS SHOWN BELOW.
51 Ω
1.5 kΩ
844 INTERFACE 8:1
TYPE: AN
LOC: B05 THRU B12
ASSY NO. 11899094
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 3
PAGE 5-178

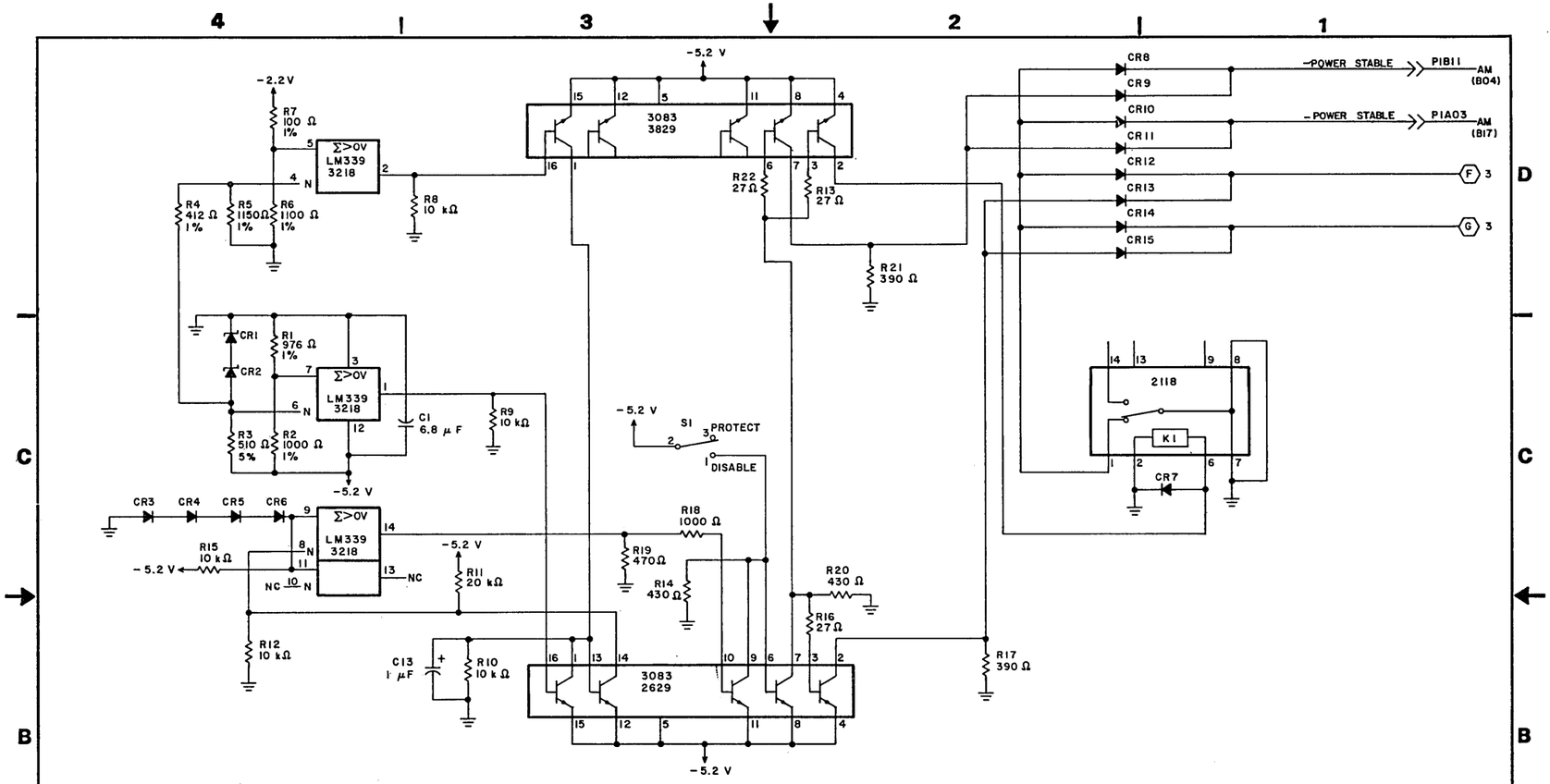

+UNIT SELECT BITS 0-2
-844 UNIT SELECT
FROM 844 DRIVE
PIA09
PIA10
PIA19
PIA20
PIA30
PIA31
PIA40
PIA41
P2A09
P2A10
P2A19
P2A20
P2A30
P2A31
P2A40
P2A41
10114 0441
10114 1041
10114 2141
10114 2641
10114 4441
10114 4941
10114 6041
10114 6641
MUX 10164 3229
P2A13
FROM 844 DRIVE
PIB07
PIB08
PIB17
PIB18
PIB28
PIB29
PIB37
PIB38
P2B07
P2B08
P2B17
P2B18
P2B28
P2B29
P2B37
P2B38
560 Ω
120 Ω
0.01
51 Ω
-5.2 V
10114 1029
10114 2129
10114 4929
10114 6029
12 Ω
360 Ω
MUX 10164 4417
P2A34
NOTES:
SEE SHEET 2
844 INTERFACE 8:1
TYPE: AN
LOC: B05 THRU B12
ASSY NO. 11899094
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 3
PAGE 5-179



DEVELOPMENT DIVISION	844 INTERFACE CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AP	LOC: B13	C	SHEET 1 OF 4	PAGE 5-180
ASSY. NO. 11899080				


4
3
2
1
D
C
B
A
NC (9) =1 10195 4417 15 -SEL 2 P1B21 AM (B04)
NC (12) 1 10101 3853 11 NC
10 4
NC (9) = 10195 6653 4 +UNITSEL BIT 2 P2B38 AN (B12)
3 +UNITSEL BIT 2 P2A38 AN (B11)
2 +UNITSEL BIT 2 P2A40 AN (B10)
15 +UNIT SEL BIT 2 P2B41 AN (B09)
14 +UNITSEL BIT 2 P2A41 AN (B08)
13 +UNITSEL BIT 2 P2B40 AN (B07)
NC (9) = 10195 6641 15 +UNITSEL BIT 2 P2A37 AN (B06)
4 +UNITSEL BIT 2 P2B37 AN (B05)
NC (9) =1 10195 4417 14 -SEL 1 P1B22 AM (B04)
NC (12) 1 10101 3853 9 NC
13 15
NC (9) = 10195 6041 2 +UNITSEL BIT 1 P2B28 AN (B12)
3 +UNITSEL BIT 1 P2B27 AN (B11)
4 +UNITSEL BIT 1 P2A27 AN (B10)
13 +UNITSEL BIT 1 P2A28 AN (B09)
14 +UNITSEL BIT 1 P2B29 AN (B08)
15 +UNITSEL BIT 1 P2A29 AN (B07)
NC (9) = 10195 6641 2 +UNITSEL BIT 1 P2A30 AN (B06)
3 +UNITSEL BIT 1 P2B30 AN (B05)
NC (9) =1 10195 4417 13 -SEL 0 P1A38 AM (B04)
A
7 6
NC (12) 1 10101 3853 3 P1B38 NC
NC (9) = 10195 2641 3 +UNITSEL BIT 0 P1A30 AN (B12)
6 4 +UNITSEL BIT 0 P1B30 AN (B11)
7
NC (9) = 10195 2141 13 +UNITSEL BIT 0 P1A28 AN (B10)
10 14 +UNITSEL BIT 0 P1B29 AN (B09)
11 15 +UNITSEL BIT 0 P1A29 AN (B08)
12 2 +UNITSEL BIT 0 P1B27 AN (B07)
5 3 +UNITSEL BIT 0 P1A27 AN (B06)
6 4 +UNITSEL BIT 0 P1B28 AN (B05)
7
NC (9) = 10195 3241 15 +844 SELECT P1A37 AN (B12)
12 2 +844 SELECT P1A34 AN (B11)
5 3 +844 SELECT P1B34 AN (B10)
6 4 +844 SELECT P1B37 AN (B09)
7
NC (9) = 10195 2641 13 +844 SELECT P1B32 AN (B08)
10 14 +844 SELECT P1B31 AN (B07)
11 15 +844 SELECT P1A31 AN (B06)
12 2 +844 SELECT P1B33 AN (B05)
5
NC (12) 1 10101 3853 2 38
AF P1A40 (NOC9/7) +844 SELECT 4 5 +844 SELECT
+UNIT SEL BIT 3 A 3
+UNIT SEL BIT 2 B 3
+UNIT SEL BIT 1 C 3
+UNIT SEL BIT 0 D 3
E 3
AG P1B42 +FULL NC (9) =1 10195 4417 5 2
7 C3 C2 C1 RGTR 10173 3253
NC 9
UNIT SELECT BITS 0-3
AF P1B43 +NOC 1/3 3 C2,3D 2
NC 4 C1,3D
AF P1B40 +NOC 1/2 12 C2,3D 15
NC 13 C1,3D
AF P1A41 +NOC 1/1 10 C2,3D 14
NC 11 C1,3D
AF P1B41 +NOC 1/0 5 C2,3D 1
NC 6 C1,3D
16
A
GD DEVELOPMENT DIVISION
844 INTERFACE CONTROL
TYPE: AP
LOC: B13
ASSY. NO. 11899080
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 2 OF 4
PAGE 5-181

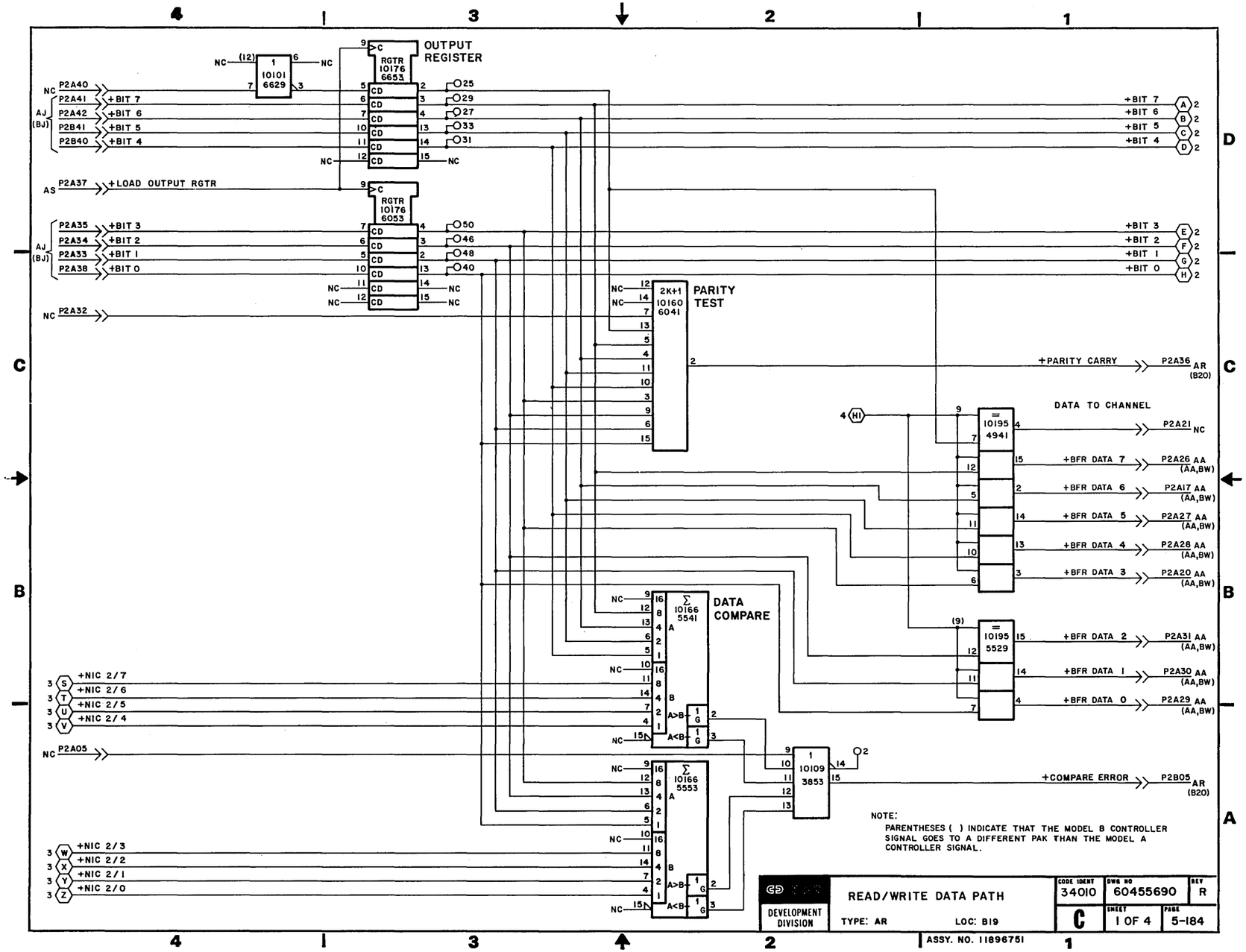

TO DRIVE
+ OPEN CABLE DETECT TO DRIVE
CABLE A
CABLE B
SW P1A17 + DISABLE UNIT 7
SW P1B17 + DISABLE UNIT 6
SW P1A19 + DISABLE UNIT 5
SW P1B19 + DISABLE UNIT 4
SW P2A17 + DISABLE UNIT 3
SW P2B17 + DISABLE UNIT 2
SW P2A19 + DISABLE UNIT 1
SW P2B19 + DISABLE UNIT 0
10102 1541
10102 5541
X/Y 10192 1553
X/Y 10192 5553
+ UNITSEL 7
+ UNITSEL 6
+ UNITSEL 5
+ UNITSEL 4
+ UNITSEL 3
+ UNITSEL 2
+ UNITSEL 1
+ UNITSEL 0
P1B04
P1B05
P1B14
P1B15
P1B25
P1B26
P1B35
P1B36
P2B04
P2B05
P2B14
P2B15
P2B25
P2B26
P2B35
P2B36
X→Y CODER 10161 3841
+UNIT SEL BIT 2
+UNIT SEL BIT 1
+UNIT SEL BIT 0
+844 SELECT
+UNIT SEL BIT 3
10195 4941
10195 1529
+SEL 3
P1A24 AM (B04)
10195 2153
+DISABLE UNIT 7 HI
+DISABLE UNIT 6 HI
+DISABLE UNIT 5 HI
+DISABLE UNIT 4 HI
+DISABLE UNIT 3 HI
+DISABLE UNIT 2 HI
+DISABLE UNIT 1 HI
+DISABLE UNIT 0 HI
P1A18
P1B18
P1A20
P1B20
P2A18
P2B18
P2A20
P2B20
X/Y 10192 1053
X/Y 10192 2653
X/Y 10192 4953
X/Y 10192 6053
P1A11
P1A12
P1A21
P1A22
P1A32
P1A33
P1A42
P1A43
P2A11
P2A12
P2A21
P2A22
P2A32
P2A33
P2A42
P2A43
P1A04
P1A05
P1A14
P1A15
P1A25
P1A26
P1A35
P1A36
P2A04
P2A05
P2A14
P2A15
P2A25
P2A26
P2A35
P2A36
-POWER STABLE
844 INTERFACE CONTROL
DEVELOPMENT DIVISION
TYPE: AP
LOC: B13
ASSY. NO. 11899080
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 4
PAGE 5-182

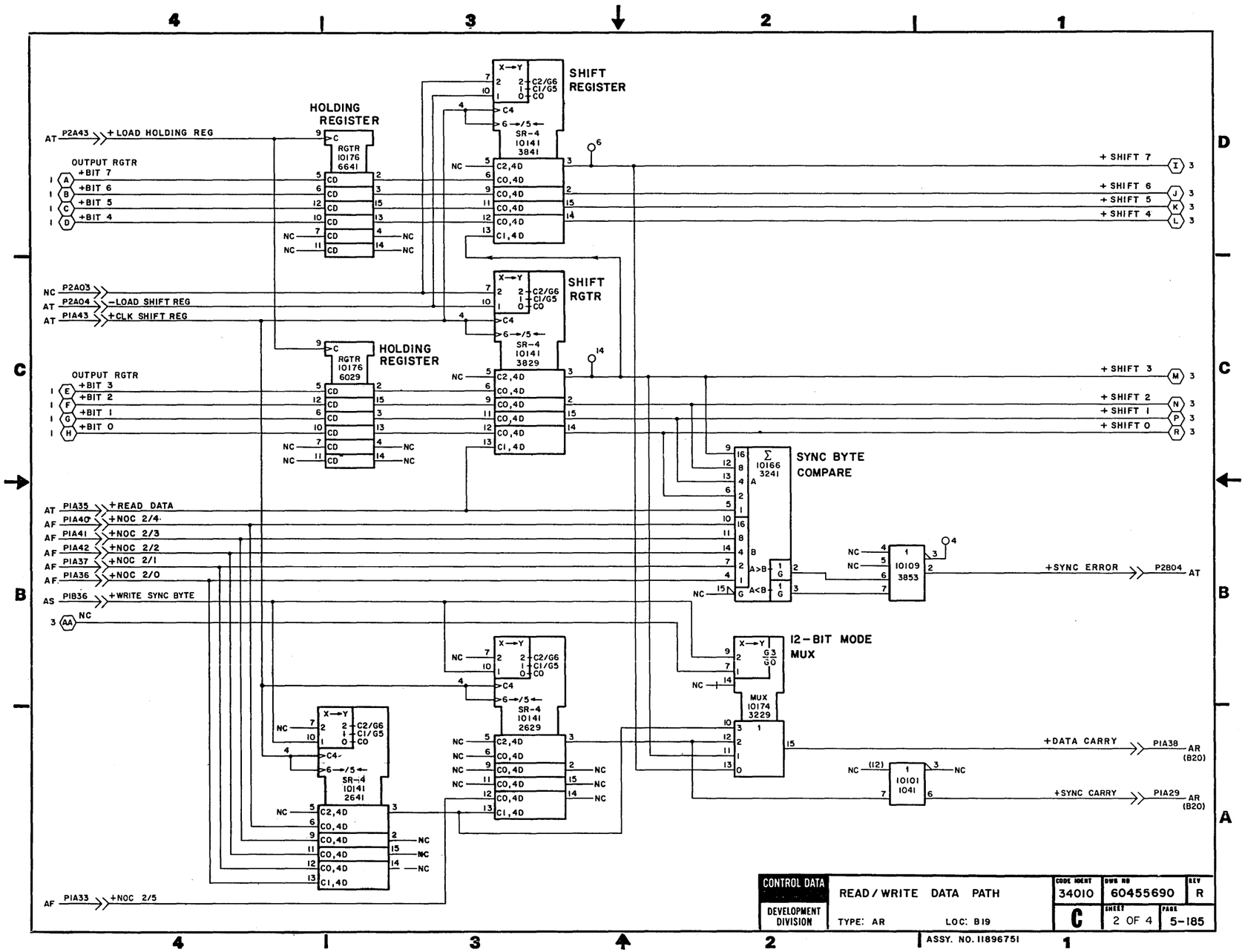


2.2 V AND 5.2 V
BUS MONITOR

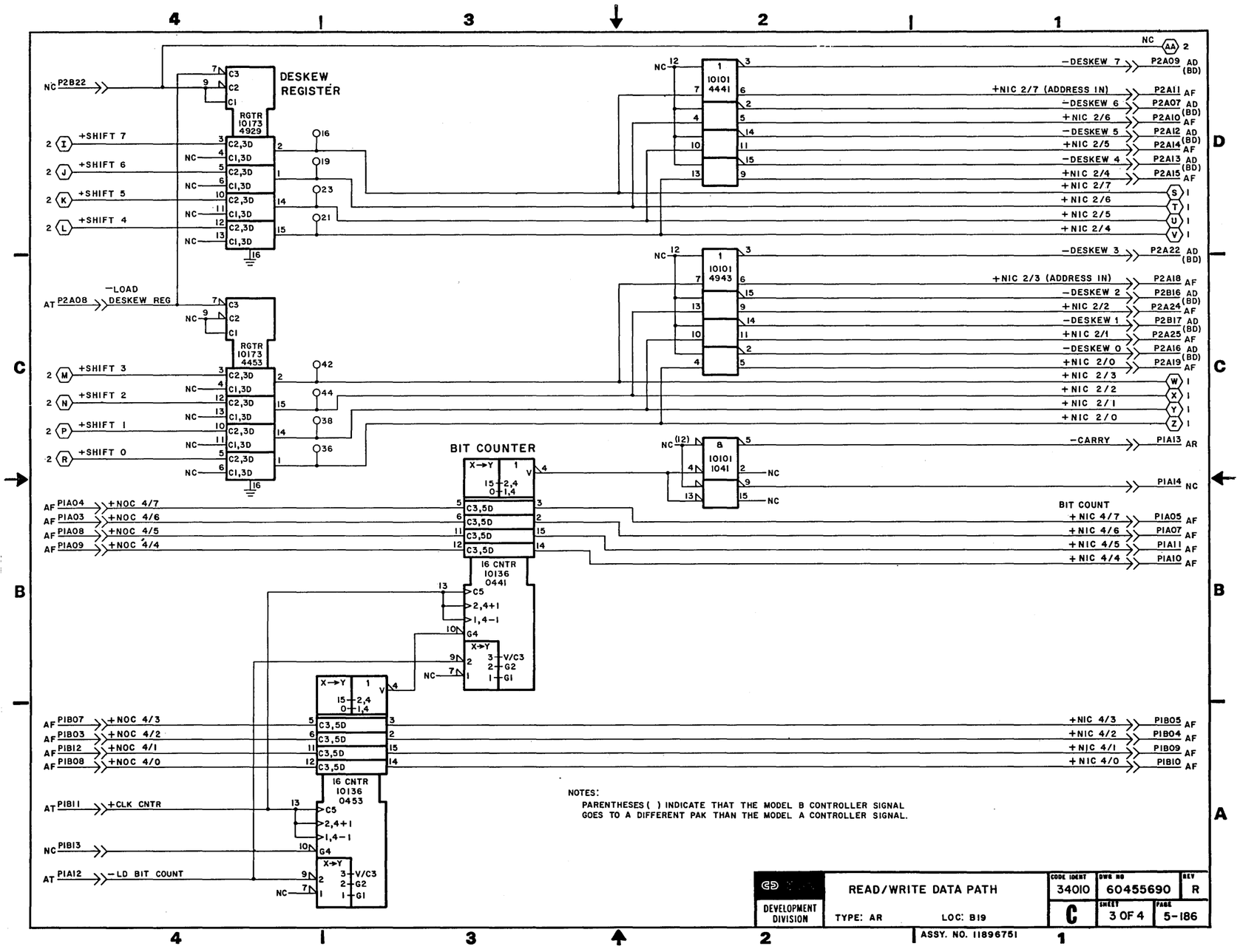
OPEN CABLE
DECTECTION CIRCUIT

DEVELOPMENT DIVISION	844 INTERFACE CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AP LOC: B13	C	SHEET 4 OF 4	PAGE 5-183
	ASSY. NO. 11899080			


OUTPUT REGISTER
RGTR 10176 6653
RGTR 10176 6053
P2A40 +BIT 7
P2A41 +BIT 6
P2A42 +BIT 5
P2B41 +BIT 4
P2B40
P2A37 +LOAD OUTPUT RGTR
P2A35 +BIT 3
P2A34 +BIT 2
P2A33 +BIT 1
P2A38 +BIT 0
P2A32
PARITY TEST
2K+1 10160 6041
+PARITY CARRY P2A36 AR (B20)
DATA TO CHANNEL
+BFR DATA 7 P2A26 AA (AA,BW)
+BFR DATA 6 P2A17 AA (AA,BW)
+BFR DATA 5 P2A27 AA (AA,BW)
+BFR DATA 4 P2A28 AA (AA,BW)
+BFR DATA 3 P2A20 AA (AA,BW)
+BFR DATA 2 P2A31 AA (AA,BW)
+BFR DATA 1 P2A30 AA (AA,BW)
+BFR DATA 0 P2A29 AA (AA,BW)
DATA COMPARE
+NIC 2/7
+NIC 2/6
+NIC 2/5
+NIC 2/4
P2A05
+NIC 2/3
+NIC 2/2
+NIC 2/1
+NIC 2/0
+COMPARE ERROR P2B05 AR (B20)
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
DEVELOPMENT DIVISION
READ/WRITE DATA PATH
TYPE: AR LOC: B19
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 4
PAGE 5-184
ASSY. NO. 11896751

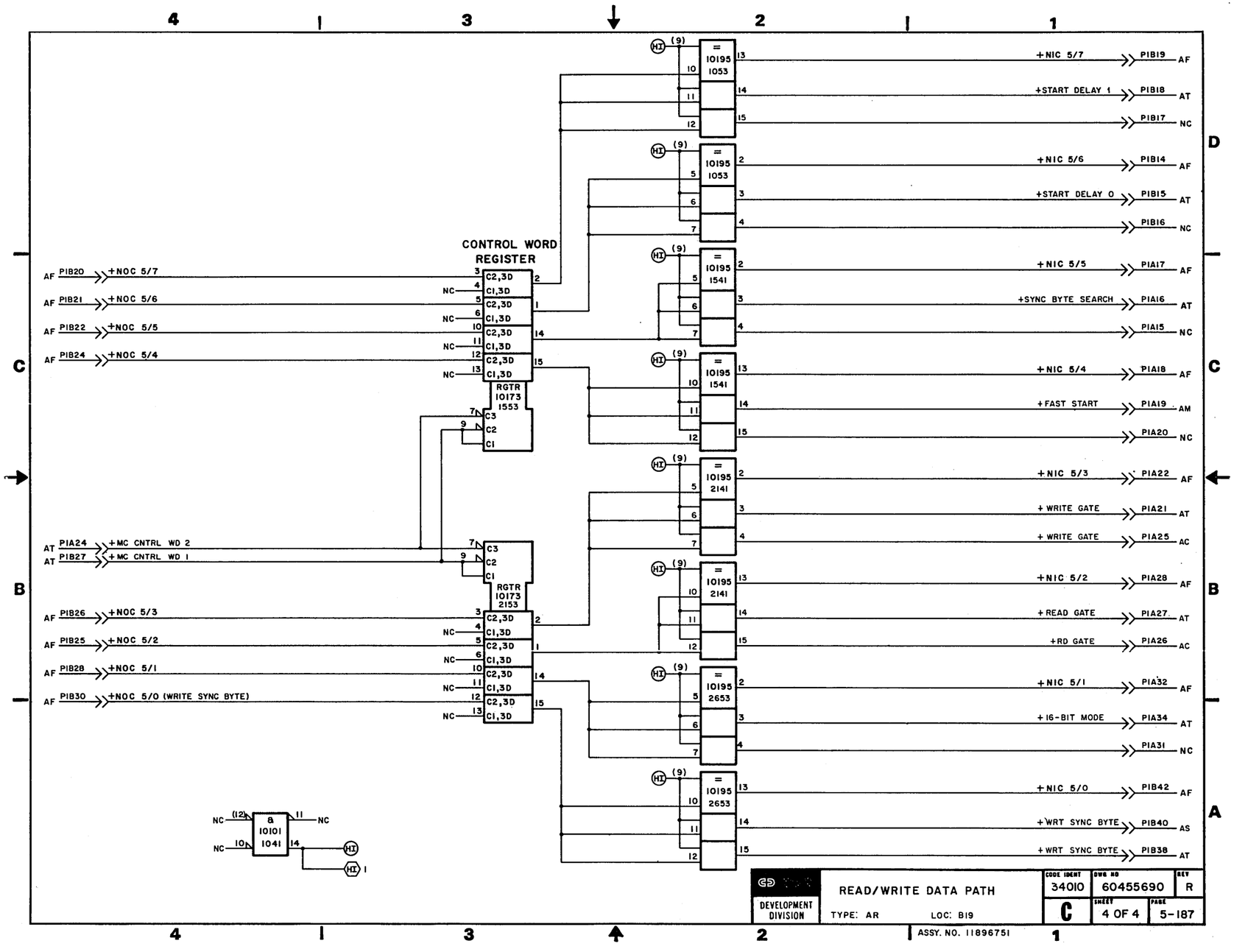


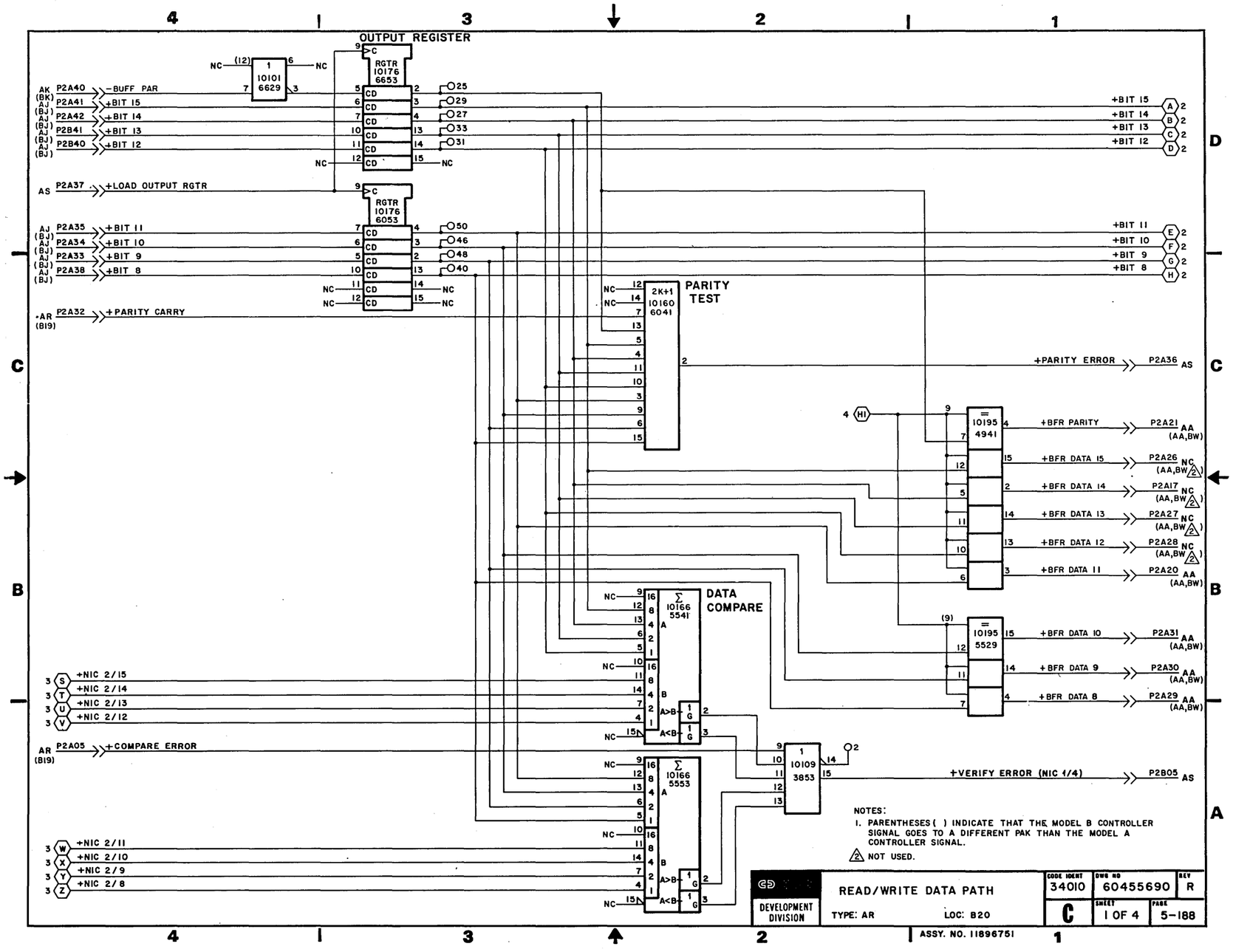
CONTROL DATA	READ / WRITE DATA PATH	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	TYPE: AR LOC: B19	34010	60455690	R
	ASSY. NO. 11896751	C	SHEET 2 OF 4	PAGE 5-185

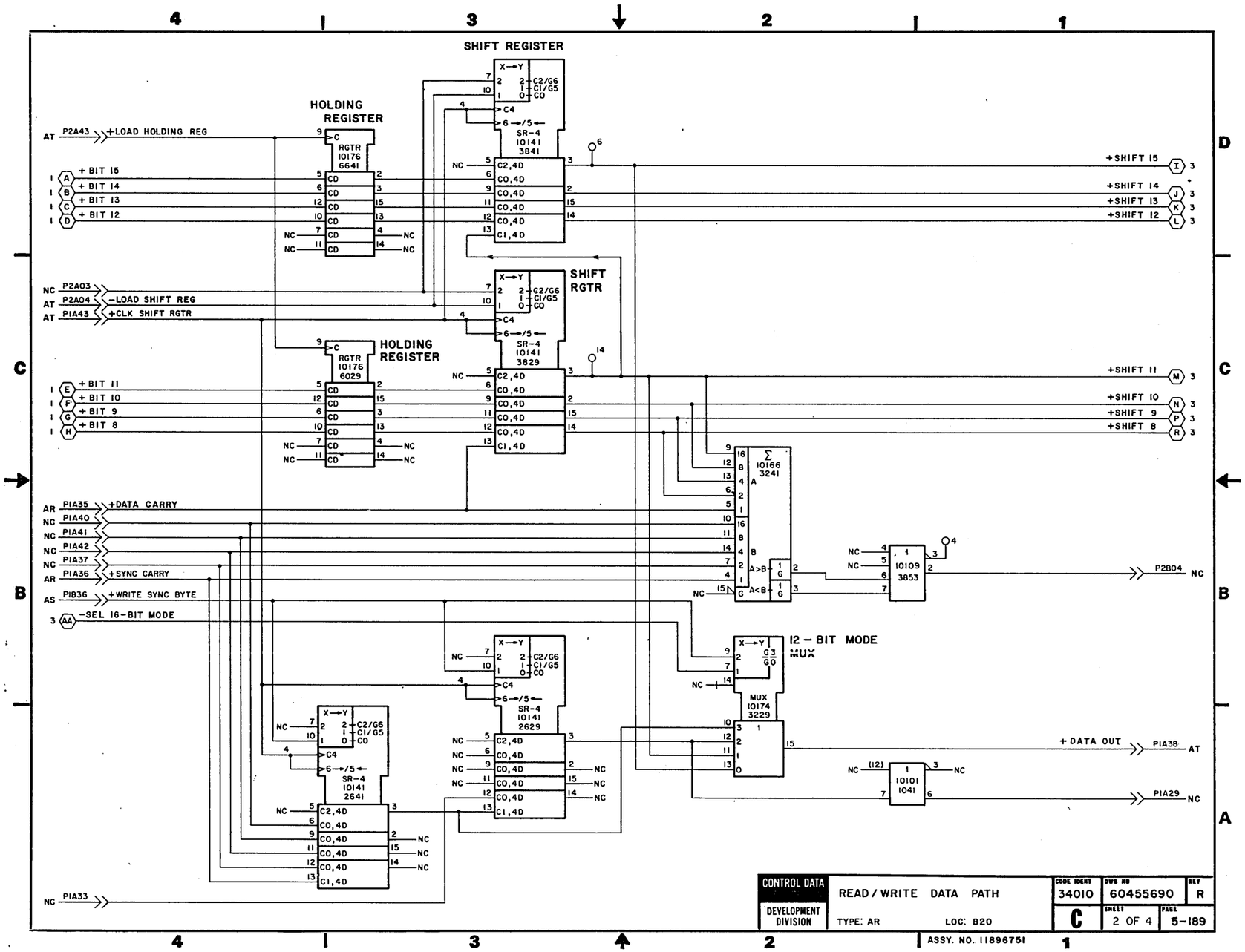


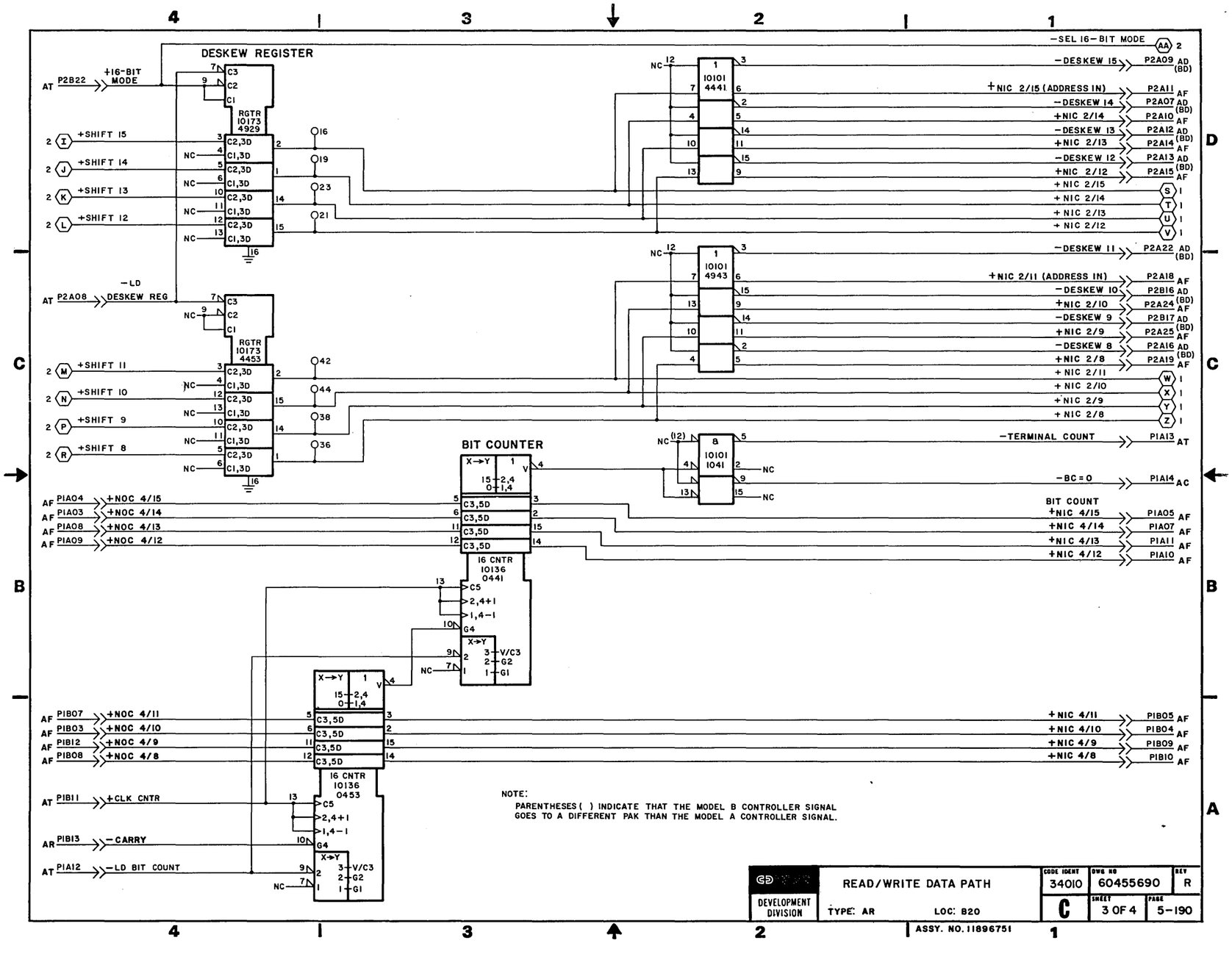
NOTES:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

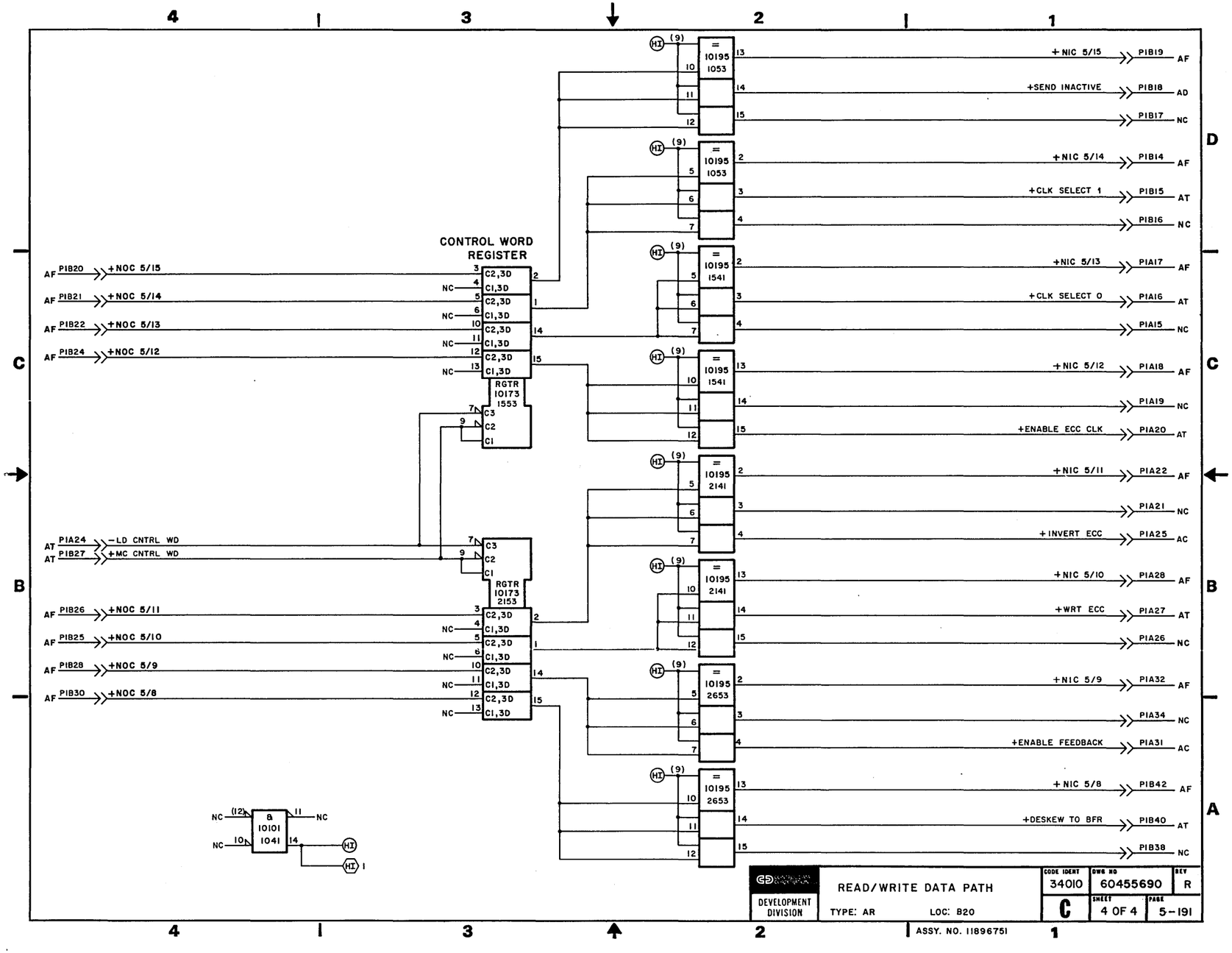
DEVELOPMENT DIVISION	READ/WRITE DATA PATH	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AR LOC: B19	C	SHEET 3 OF 4	PAGE 5-186
	ASSY. NO. 11896751			

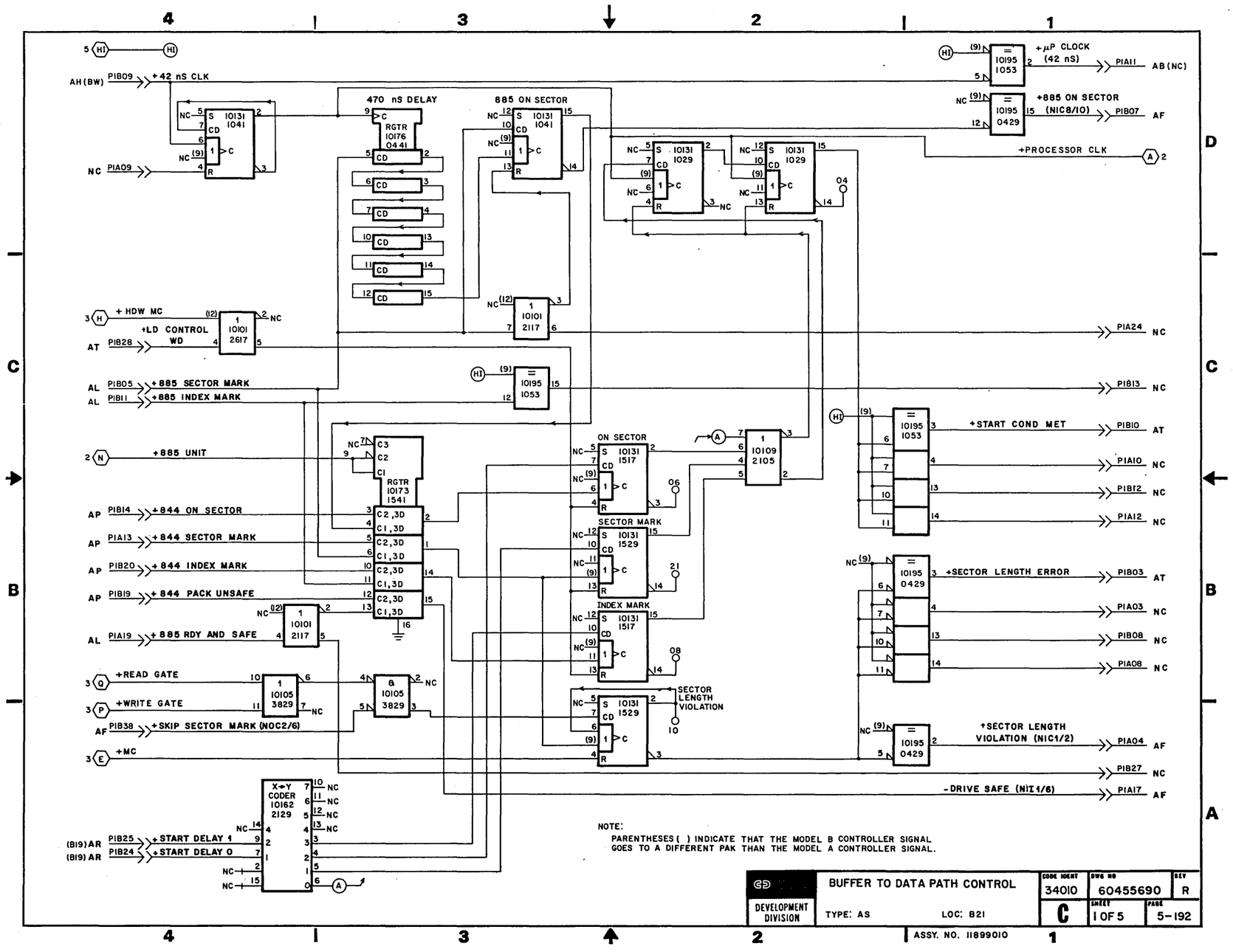

CONTROL WORD REGISTER
AF PIB20 +NOC 5/7
AF PIB21 +NOC 5/6
AF PIB22 +NOC 5/5
AF PIB24 +NOC 5/4
AT PIA24 +MC CNTRL WD 2
AT PIB27 +MC CNTRL WD 1
AF PIB26 +NOC 5/3
AF PIB25 +NOC 5/2
AF PIB28 +NOC 5/1
AF PIB30 +NOC 5/0 (WRITE SYNC BYTE)
C2,3D
C1,3D
RGTR 10173 1553
RGTR 10173 2153
8 10101 1041
= 10195 1053
= 10195 1541
= 10195 2141
= 10195 2653
+NIC 5/7 PIB19 AF
+START DELAY 1 PIB18 AT
PIB17 NC
+NIC 5/6 PIB14 AF
+START DELAY 0 PIB15 AT
PIB16 NC
+NIC 5/5 PIA17 AF
+SYNC BYTE SEARCH PIA16 AT
PIA15 NC
+NIC 5/4 PIA18 AF
+FAST START PIA19 AM
PIA20 NC
+NIC 5/3 PIA22 AF
+WRITE GATE PIA21 AT
+WRITE GATE PIA25 AC
+NIC 5/2 PIA28 AF
+READ GATE PIA27 AT
+RD GATE PIA26 AC
+NIC 5/1 PIA32 AF
+16-BIT MODE PIA34 AT
PIA31 NC
+NIC 5/0 PIB42 AF
+WRT SYNC BYTE PIB40 AS
+WRT SYNC BYTE PIB38 AT
DEVELOPMENT DIVISION
READ/WRITE DATA PATH
TYPE: AR LOC: B19
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 4 OF 4
PAGE 5-187
ASSY. NO. 11896751


OUTPUT REGISTER
RGTR 10176 6653
RGTR 10176 6053
P2A40 -BUFF PAR
P2A41 +BIT 15
P2A42 +BIT 14
P2B41 +BIT 13
P2B40 +BIT 12
P2A37 +LOAD OUTPUT RGTR
P2A35 +BIT 11
P2A34 +BIT 10
P2A33 +BIT 9
P2A38 +BIT 8
P2A32 +PARITY CARRY
PARITY TEST
2K+1 10160 6041
+PARITY ERROR P2A36
DATA COMPARE
Σ 10166 5541
Σ 10166 5553
P2A05 +COMPARE ERROR
+NIC 2/15
+NIC 2/14
+NIC 2/13
+NIC 2/12
+NIC 2/11
+NIC 2/10
+NIC 2/9
+NIC 2/8
= 10195 4941
= 10195 5529
+BFR PARITY P2A21
+BFR DATA 15 P2A26
+BFR DATA 14 P2A17
+BFR DATA 13 P2A27
+BFR DATA 12 P2A28
+BFR DATA 11 P2A20
+BFR DATA 10 P2A31
+BFR DATA 9 P2A30
+BFR DATA 8 P2A29
+VERIFY ERROR (NIC 1/4) P2B05
NOTES:
1. PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
2 NOT USED.
DEVELOPMENT DIVISION
READ/WRITE DATA PATH
TYPE: AR LOC: B20
ASSY. NO. 11896751
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 4
PAGE 5-188


SHIFT REGISTER
HOLDING REGISTER
SHIFT RGTR
HOLDING REGISTER
12 – BIT MODE MUX
AT P2A43 +LOAD HOLDING REG
+ BIT 15
+ BIT 14
+ BIT 13
+ BIT 12
NC P2A03
AT P2A04 -LOAD SHIFT REG
AT P1A43 +CLK SHIFT RGTR
+ BIT 11
+ BIT 10
+ BIT 9
+ BIT 8
AR P1A35 +DATA CARRY
NC P1A40
NC P1A41
NC P1A42
NC P1A37
AR P1A36 +SYNC CARRY
AS P1B36 +WRITE SYNC BYTE
3 AA -SEL 16-BIT MODE
NC P1A33
+SHIFT 15
+SHIFT 14
+SHIFT 13
+SHIFT 12
+SHIFT 11
+SHIFT 10
+SHIFT 9
+SHIFT 8
P2B04 NC
+ DATA OUT
PIA38 AT
PIA29 NC
RGTR 10176 6641
SR-4 10141 3841
RGTR 10176 6029
SR-4 10141 3829
SR-4 10141 2629
SR-4 10141 2641
Σ 10166 3241
10109 3853
MUX 10174 3229
10101 1041
CONTROL DATA
DEVELOPMENT DIVISION
READ / WRITE DATA PATH
TYPE: AR
LOC: B20
ASSY. NO. 11896751
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 4
PAGE 5-189

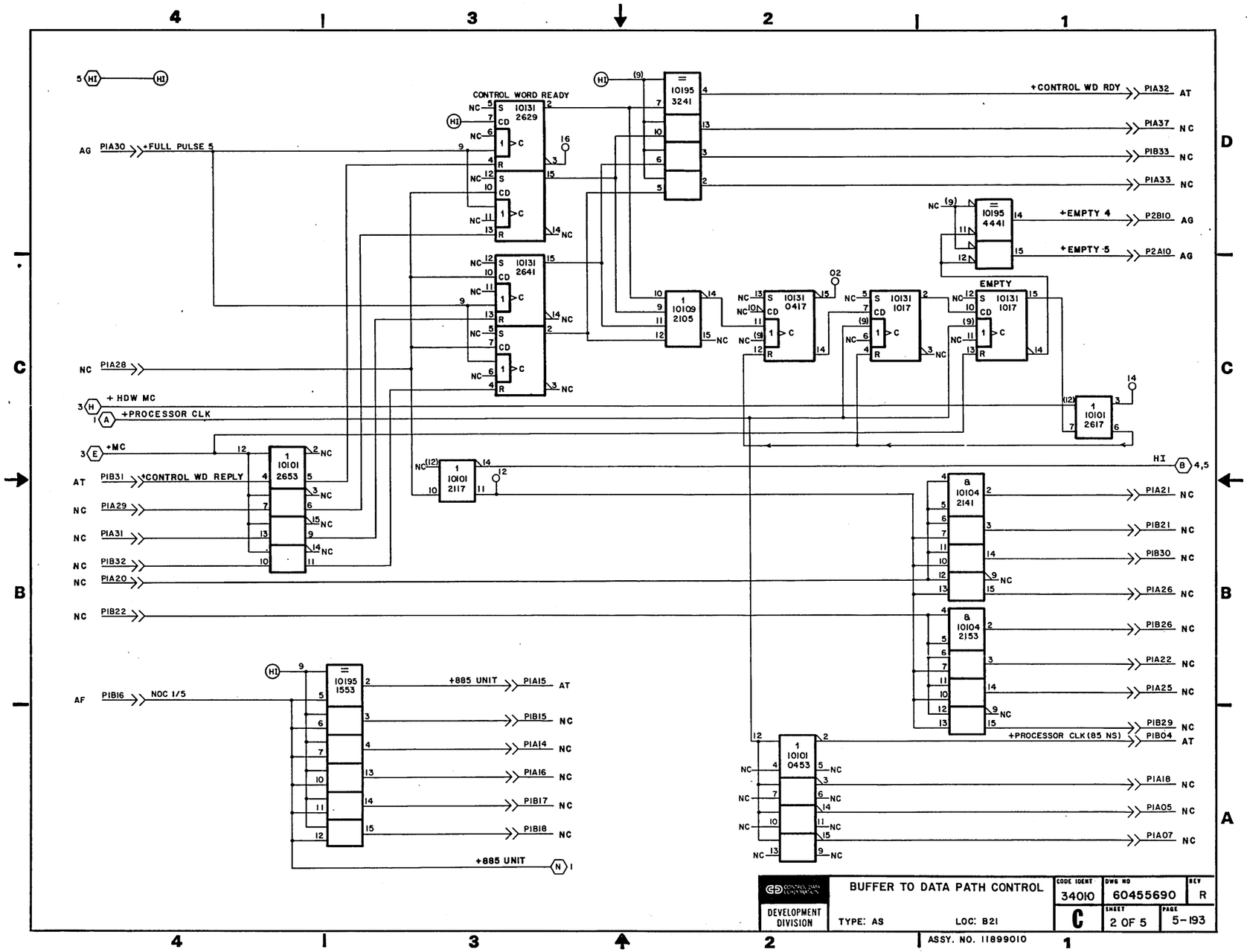

DESKEW REGISTER
AT P2B22 +16-BIT MODE
RGTR 10173 4929
2 I +SHIFT 15
2 J +SHIFT 14
2 K +SHIFT 13
2 L +SHIFT 12
16
19
23
21
AT P2A08 −LD DESKEW REG
RGTR 10173 4453
2 M +SHIFT 11
2 N +SHIFT 10
2 P +SHIFT 9
2 R +SHIFT 8
42
44
38
36
BIT COUNTER
X→Y 1 V
15−2,4
0−1,4
AF PIA04 +NOC 4/15
AF PIA03 +NOC 4/14
AF PIA08 +NOC 4/13
AF PIA09 +NOC 4/12
C3,5D
16 CNTR 10136 0441
C5
2,4+1
1,4−1
G4
X→Y
3−V/C3
2−G2
1−G1
AF PIB07 +NOC 4/11
AF PIB03 +NOC 4/10
AF PIB12 +NOC 4/9
AF PIB08 +NOC 4/8
16 CNTR 10136 0453
AT PIB11 +CLK CNTR
AR PIB13 −CARRY
AT PIA12 −LD BIT COUNT
10101 4441
10101 4943
10101 1041
−SEL 16−BIT MODE
−DESKEW 15
+NIC 2/15 (ADDRESS IN)
−DESKEW 14
+NIC 2/14
−DESKEW 13
+NIC 2/13
−DESKEW 12
+NIC 2/12
+NIC 2/15
+NIC 2/14
+NIC 2/13
+NIC 2/12
−DESKEW 11
+NIC 2/11 (ADDRESS IN)
−DESKEW 10
+NIC 2/10
−DESKEW 9
+NIC 2/9
−DESKEW 8
+NIC 2/8
+NIC 2/11
+NIC 2/10
+NIC 2/9
+NIC 2/8
−TERMINAL COUNT
−BC=0
BIT COUNT
+NIC 4/15
+NIC 4/14
+NIC 4/13
+NIC 4/12
+NIC 4/11
+NIC 4/10
+NIC 4/9
+NIC 4/8
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
DEVELOPMENT DIVISION
READ/WRITE DATA PATH
TYPE: AR LOC: B20
ASSY. NO. 11896751
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 4
PAGE 5-190
C

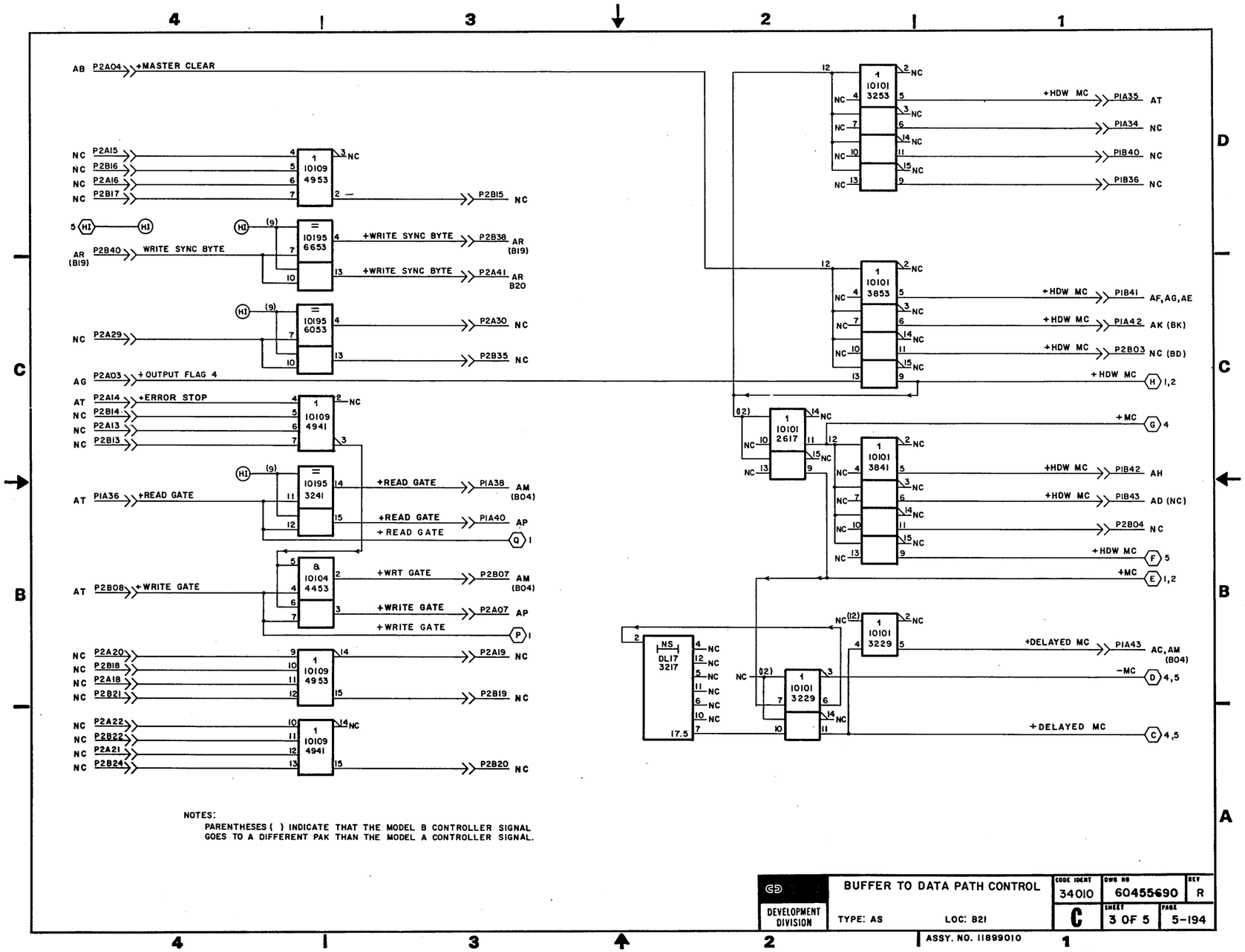

CONTROL WORD REGISTER
AF PIB20 +NOC 5/15
AF PIB21 +NOC 5/14
AF PIB22 +NOC 5/13
AF PIB24 +NOC 5/12
AT PIA24 -LD CNTRL WD
AT PIB27 +MC CNTRL WD
AF PIB26 +NOC 5/11
AF PIB25 +NOC 5/10
AF PIB28 +NOC 5/9
AF PIB30 +NOC 5/8
C2,3D
C1,3D
RGTR 10173 1553
RGTR 10173 2153
= 10195 1053
= 10195 1541
= 10195 2141
= 10195 2653
+NIC 5/15 PIB19 AF
+SEND INACTIVE PIB18 AD
PIB17 NC
+NIC 5/14 PIB14 AF
+CLK SELECT 1 PIB15 AT
PIB16 NC
+NIC 5/13 PIA17 AF
+CLK SELECT 0 PIA16 AT
PIA15 NC
+NIC 5/12 PIA18 AF
PIA19 NC
+ENABLE ECC CLK PIA20 AT
+NIC 5/11 PIA22 AF
PIA21 NC
+INVERT ECC PIA25 AC
+NIC 5/10 PIA28 AF
+WRT ECC PIA27 AT
PIA26 NC
+NIC 5/9 PIA32 AF
PIA34 NC
+ENABLE FEEDBACK PIA31 AC
+NIC 5/8 PIB42 AF
+DESKEW TO BFR PIB40 AT
PIB38 NC
8 10101 1041
READ/WRITE DATA PATH
TYPE: AR LOC: 820
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 4 OF 4
PAGE 5-191
ASSY. NO. 11896751



NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

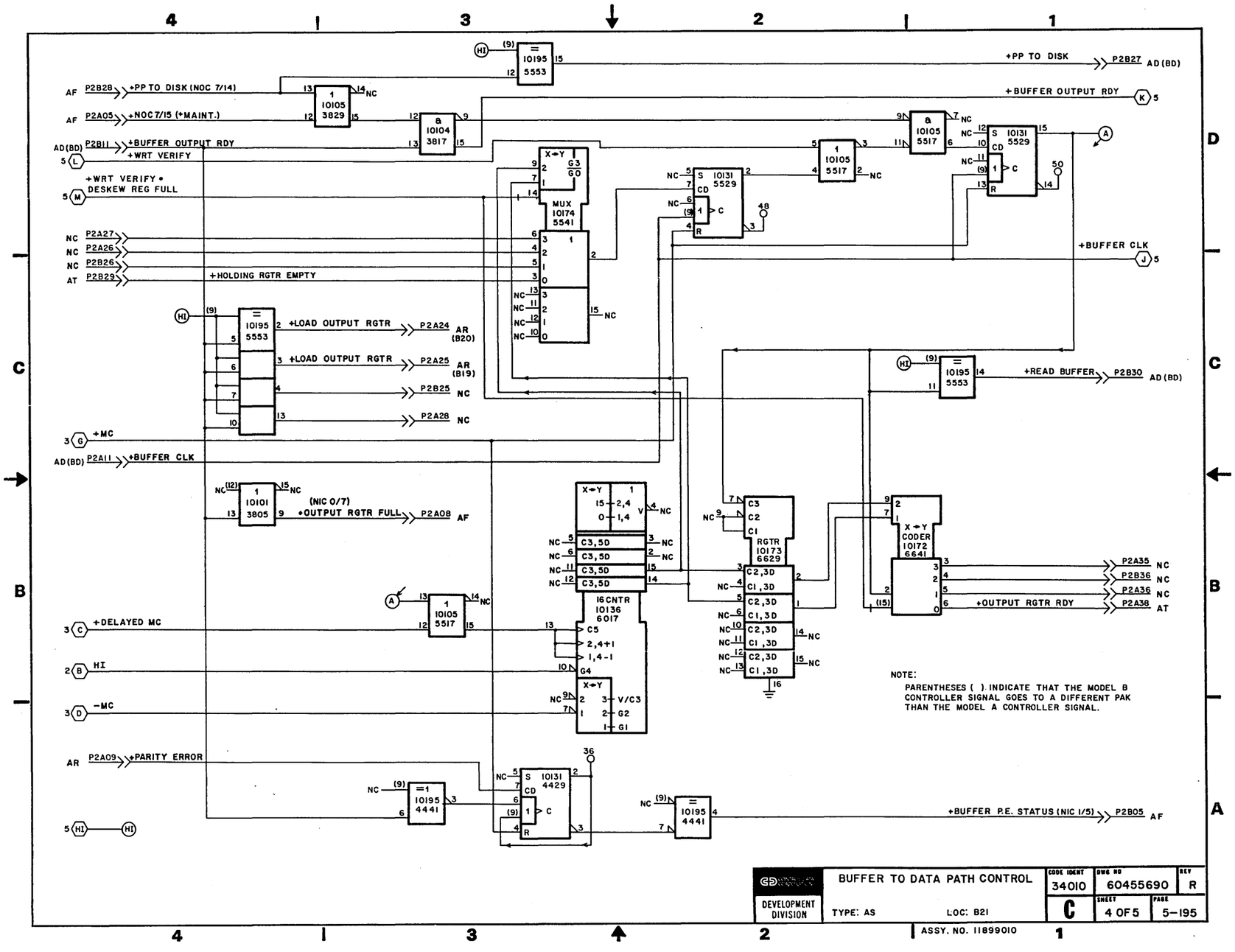
CD DEVELOPMENT DIVISION	BUFFER TO DATA PATH CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
	TYPE: AS LOC: B21	C	SHEET 1 OF 5	PAGE 5-192
	ASSY. NO. 1189010			

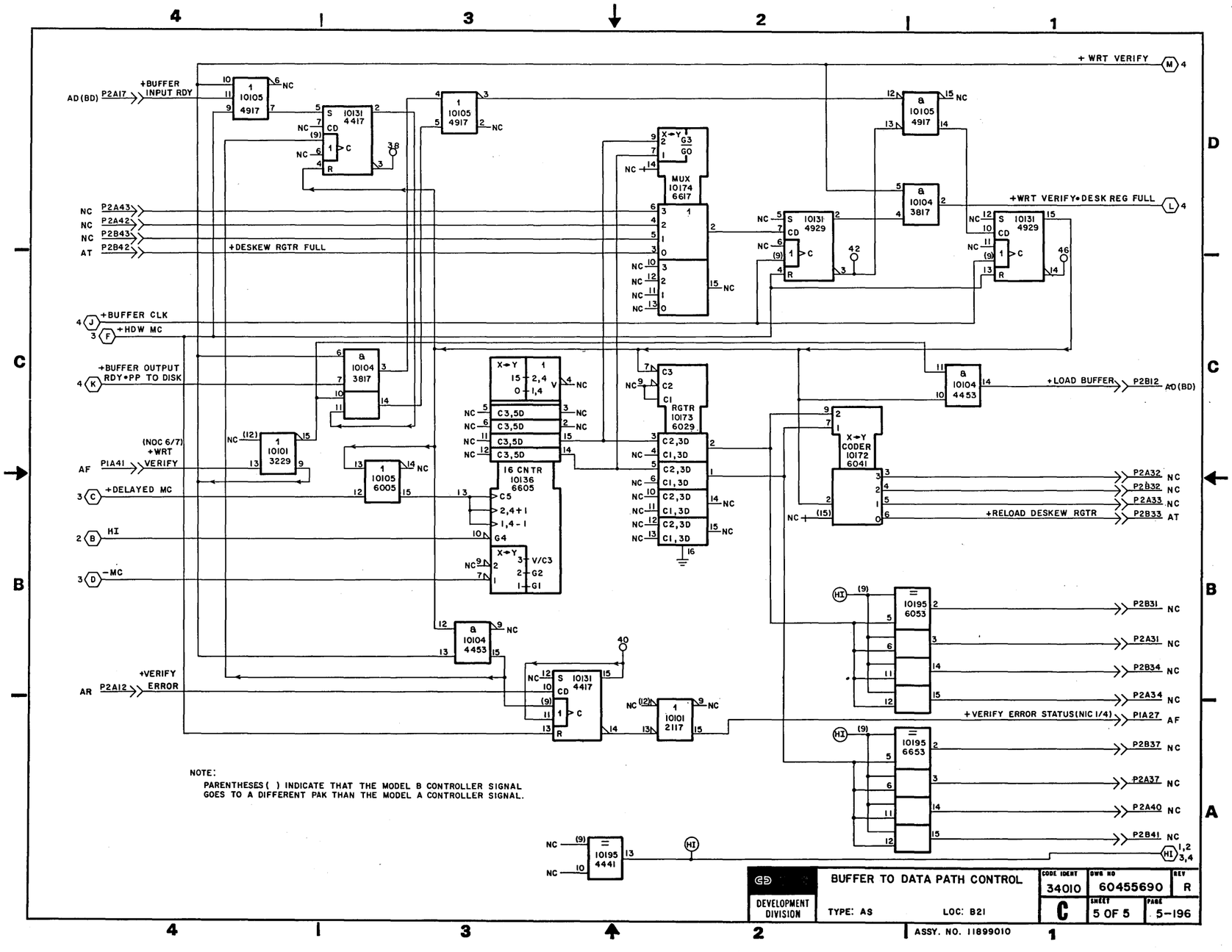

CONTROL WORD READY
10131 2629
10131 2641
10131 2653
10195 3241
10109 2105
10131 0417
10131 1017
10131 1017
10195 4441
10101 2617
10101 2117
10195 1553
10104 2141
10104 2153
10101 0453
AG PIA30 +FULL PULSE 5
NC PIA28
+ HDW MC
+PROCESSOR CLK
+MC
AT PIB31 *CONTROL WD REPLY
NC PIA29
NC PIA31
NC PIB32
NC PIA20
NC PIB22
AF PIB16 NOC 1/5
+CONTROL WD RDY PIA32 AT
PIA37 NC
PIB33 NC
PIA33 NC
+EMPTY 4 P2B10 AG
+EMPTY 5 P2A10 AG
EMPTY
HI B 4,5
PIA21 NC
PIB21 NC
PIB30 NC
PIA26 NC
PIB26 NC
PIA22 NC
PIA25 NC
PIB29 NC
+PROCESSOR CLK (85 NS) PIB04 AT
PIA18 NC
PIA05 NC
PIA07 NC
+885 UNIT PIA15 AT
PIB15 NC
PIA14 NC
PIA16 NC
PIB17 NC
PIB18 NC
+885 UNIT N 1
BUFFER TO DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AS
LOC: B21
ASSY. NO. 11899010
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 2 OF 5
PAGE 5-193

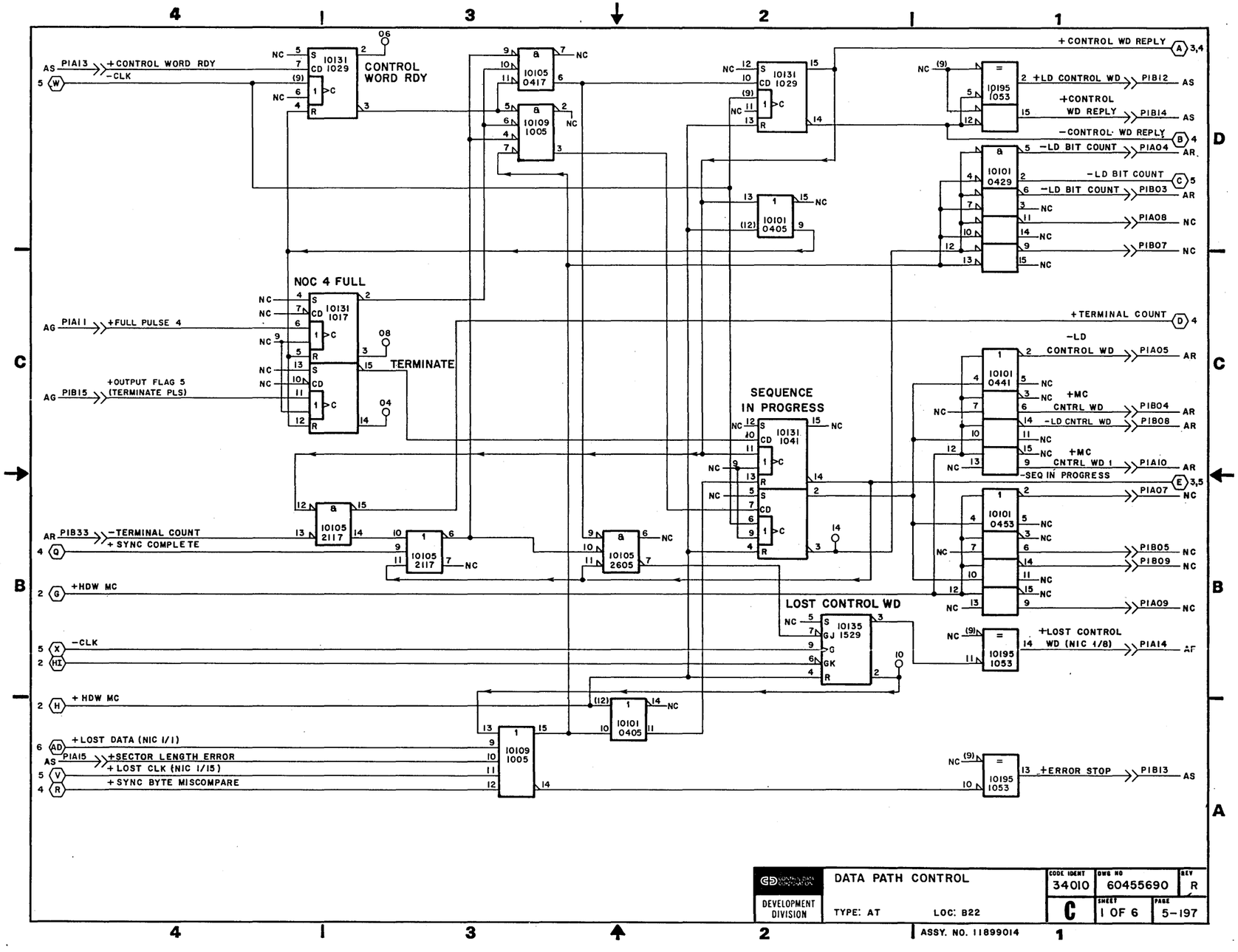


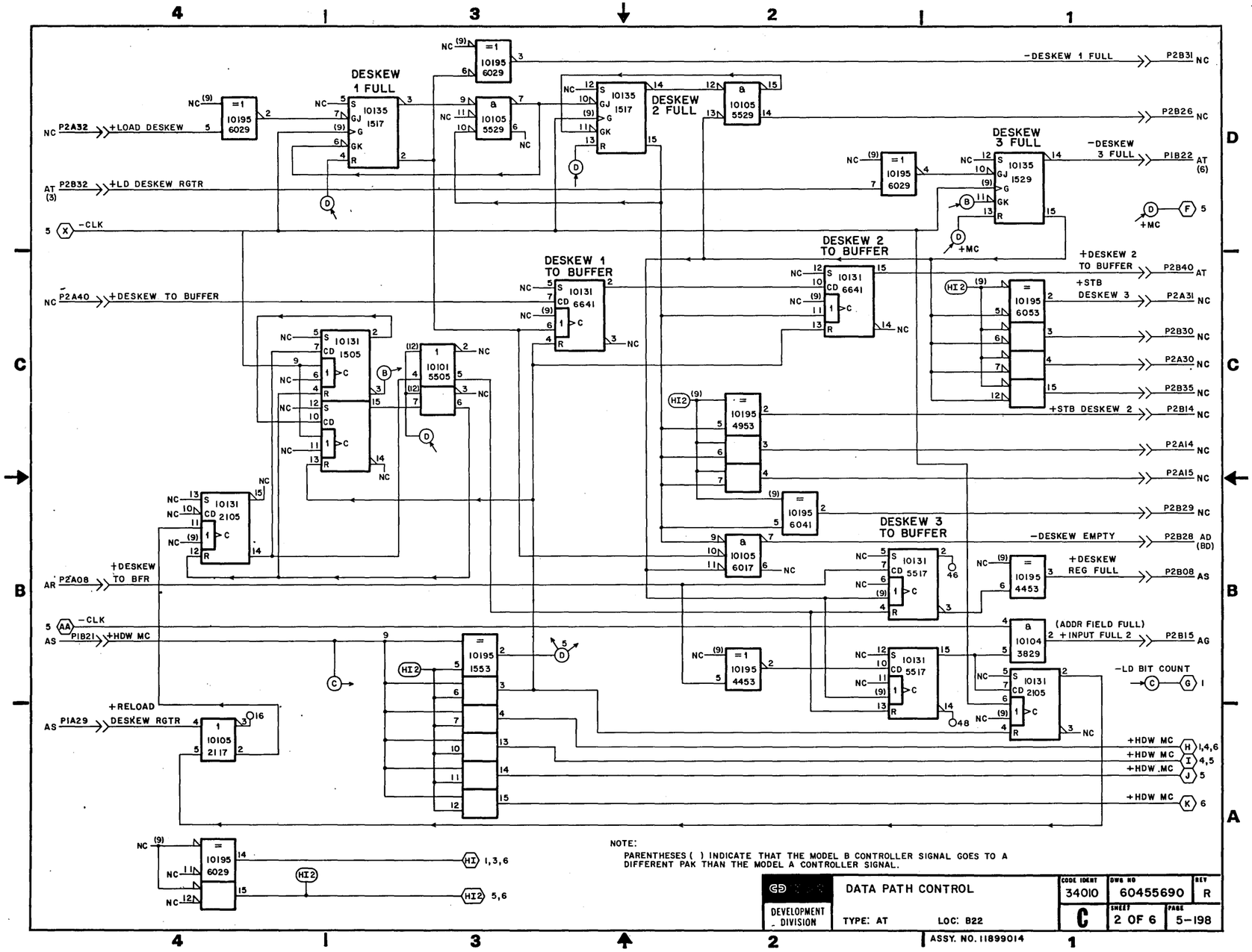
NOTES:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.

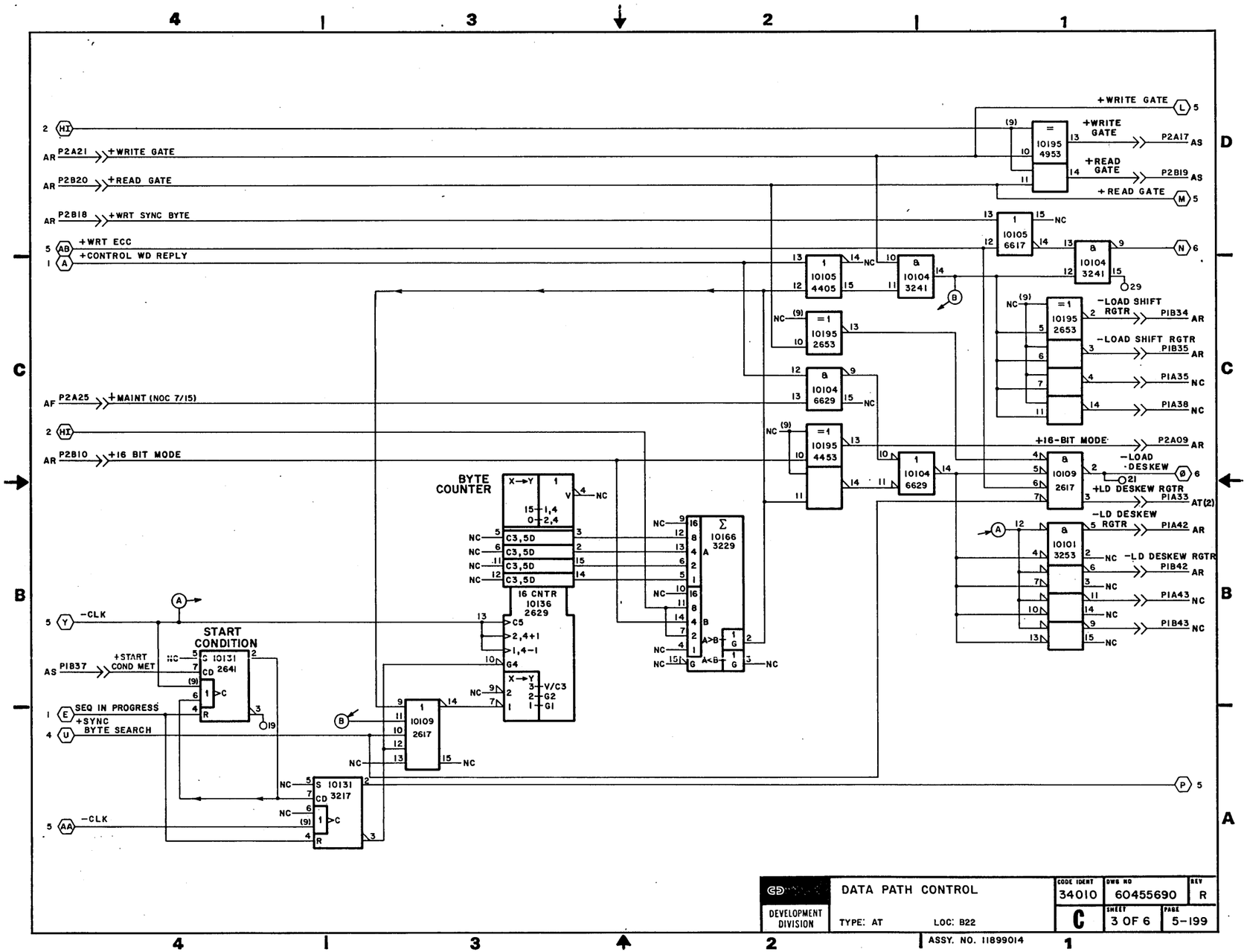
GD DEVELOPMENT DIVISION	BUFFER TO DATA PATH CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: AS LOC: B21	ASSY. NO. 11899010	C	SHEET 3 OF 5	PAGE 5-194

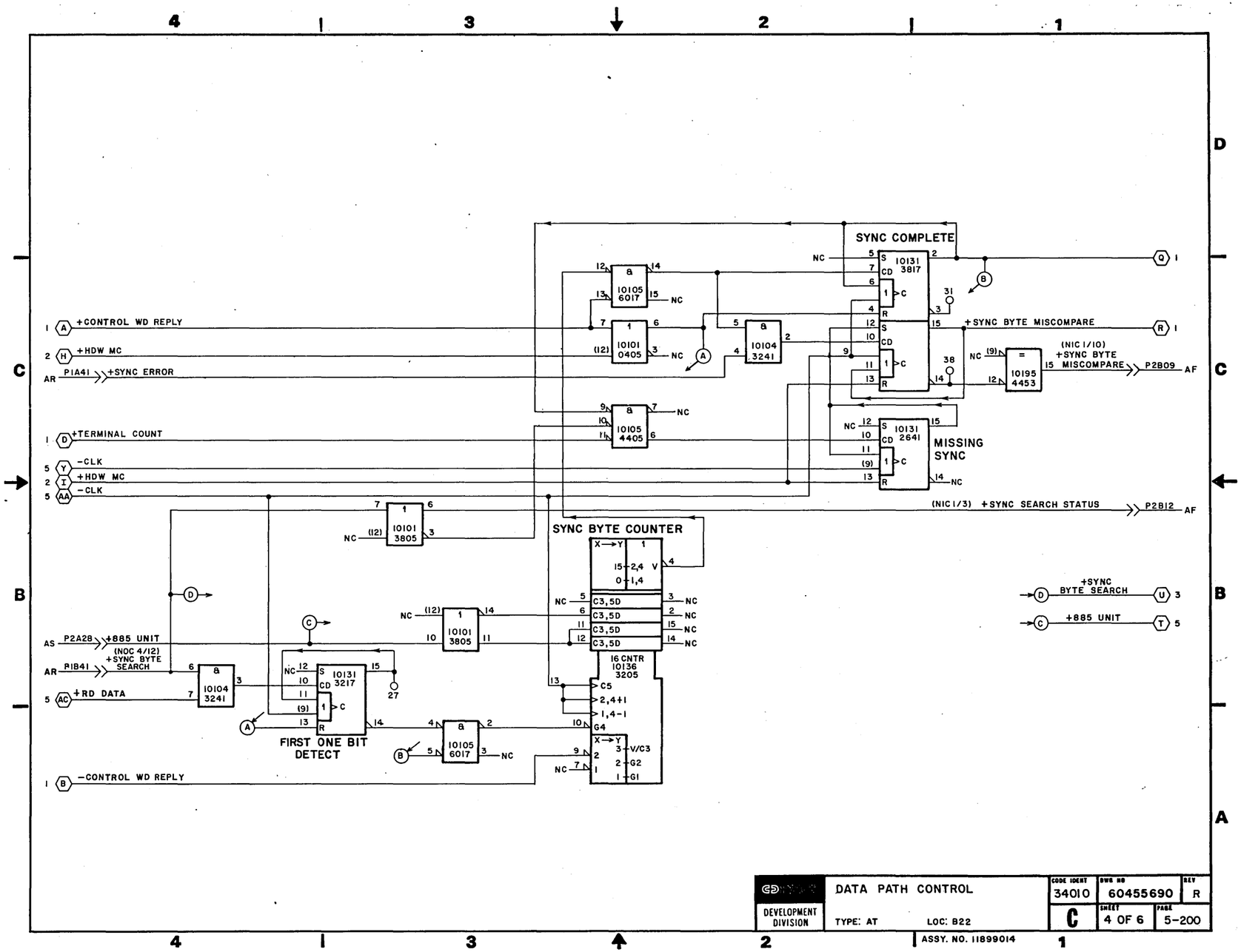

+PP TO DISK
P2B27 AD(BD)
+BUFFER OUTPUT RDY
AF P2B28 +PP TO DISK (NOC 7/14)
AF P2A05 +NOC 7/15 (+MAINT.)
AD(BD) P2B11 +BUFFER OUTPUT RDY
+WRT VERIFY
+WRT VERIFY • DESKEW REG FULL
NC P2A27
NC P2A26
NC P2B26
AT P2B29
+HOLDING RGTR EMPTY
+LOAD OUTPUT RGTR P2A24 AR (B20)
+LOAD OUTPUT RGTR P2A25 AR (B19)
P2B25 NC
P2A28 NC
+MC
AD(BD) P2A11 +BUFFER CLK
(NIC 0/7) +OUTPUT RGTR FULL P2A08 AF
+DELAYED MC
HI
-MC
AR P2A09 +PARITY ERROR
+BUFFER CLK
+READ BUFFER P2B30 AD(BD)
+BUFFER P.E. STATUS (NIC 1/5) P2B05 AF
P2A35 NC
P2B36 NC
P2A36 NC
+OUTPUT RGTR RDY P2A38 AT
MUX 10174 5541
16 CNTR 10136 6017
RGTR 10173 6629
X CODER 10172 6641
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
BUFFER TO DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AS
LOC: B21
ASSY. NO. 11899010
CODE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 4 OF 5
PAGE 5-195

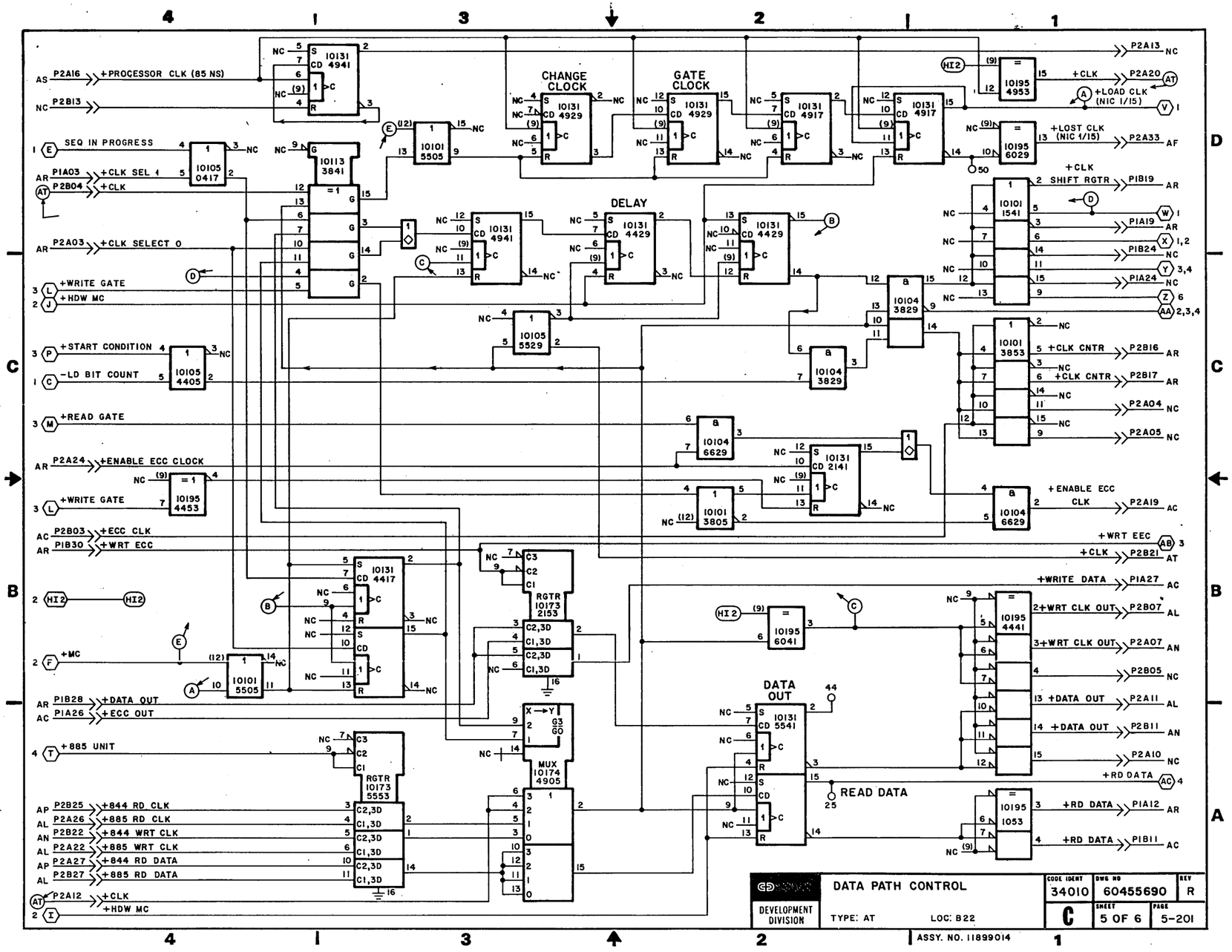

+WRT VERIFY
AD(BD) P2AI7 +BUFFER INPUT RDY
NC P2A43
NC P2A42
NC P2B43
AT P2B42
+DESKEW RGTR FULL
+WRT VERIFY•DESK REG FULL
+BUFFER CLK
+HDW MC
+BUFFER OUTPUT RDY•PP TO DISK
+LOAD BUFFER P2B12 AD(BD)
(NOC 6/7) +WRT VERIFY
AF PIA41
+DELAYED MC
HI
-MC
+RELOAD DESKEW RGTR P2B33 AT
P2A32 NC
P2B32 NC
P2A33 NC
P2B31 NC
P2A31 NC
P2B34 NC
P2A34 NC
+VERIFY ERROR STATUS(NIC 1/4) PIA27 AF
P2B37 NC
P2A37 NC
P2A40 NC
P2B41 NC
+VERIFY ERROR
AR P2AI2
MUX 10174 6617
RGTR 10173 6029
16 CNTR 10136 6605
X•Y CODER 10172 6041
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
BUFFER TO DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AS
LOC: B21
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 5 OF 5
PAGE 5-196
ASSY. NO. 11899010

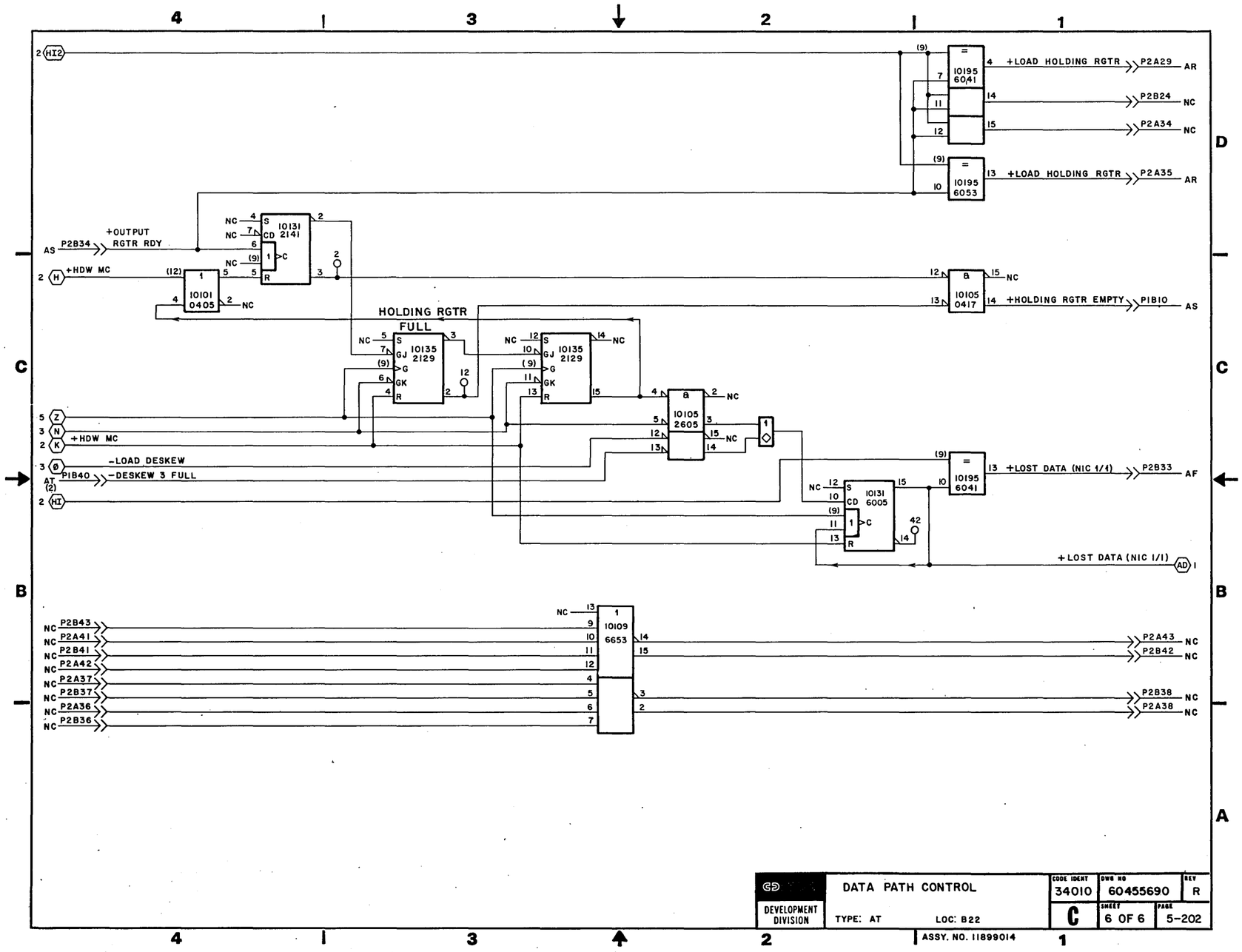

CONTROL WORD RDY
NOC 4 FULL
TERMINATE
SEQUENCE IN PROGRESS
LOST CONTROL WD
AS PIA13 +CONTROL WORD RDY
-CLK
AG PIA11 +FULL PULSE 4
AG PIB15 +OUTPUT FLAG 5 (TERMINATE PLS)
AR PIB33 -TERMINAL COUNT
+SYNC COMPLETE
+HDW MC
-CLK
+HDW MC
+LOST DATA (NIC 1/1)
AS PIA15 +SECTOR LENGTH ERROR
+LOST CLK (NIC 1/15)
+SYNC BYTE MISCOMPARE
+CONTROL WD REPLY
+LD CONTROL WD PIB12 AS
+CONTROL WD REPLY PIB14 AS
-CONTROL WD REPLY
-LD BIT COUNT PIA04 AR
-LD BIT COUNT
-LD BIT COUNT PIB03 AR
PIA08 NC
PIB07 NC
+TERMINAL COUNT
-LD CONTROL WD PIA05 AR
+MC CNTRL WD PIB04 AR
-LD CNTRL WD PIB08 AR
+MC CNTRL WD 1 PIA10 AR
-SEQ IN PROGRESS
PIA07 NC
PIB05 NC
PIB09 NC
PIA09 NC
+LOST CONTROL WD (NIC 1/8) PIA14 AF
+ERROR STOP PIB13 AS
DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AT
LOC: B22
ASSY. NO. 11899014
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 6
PAGE 5-197

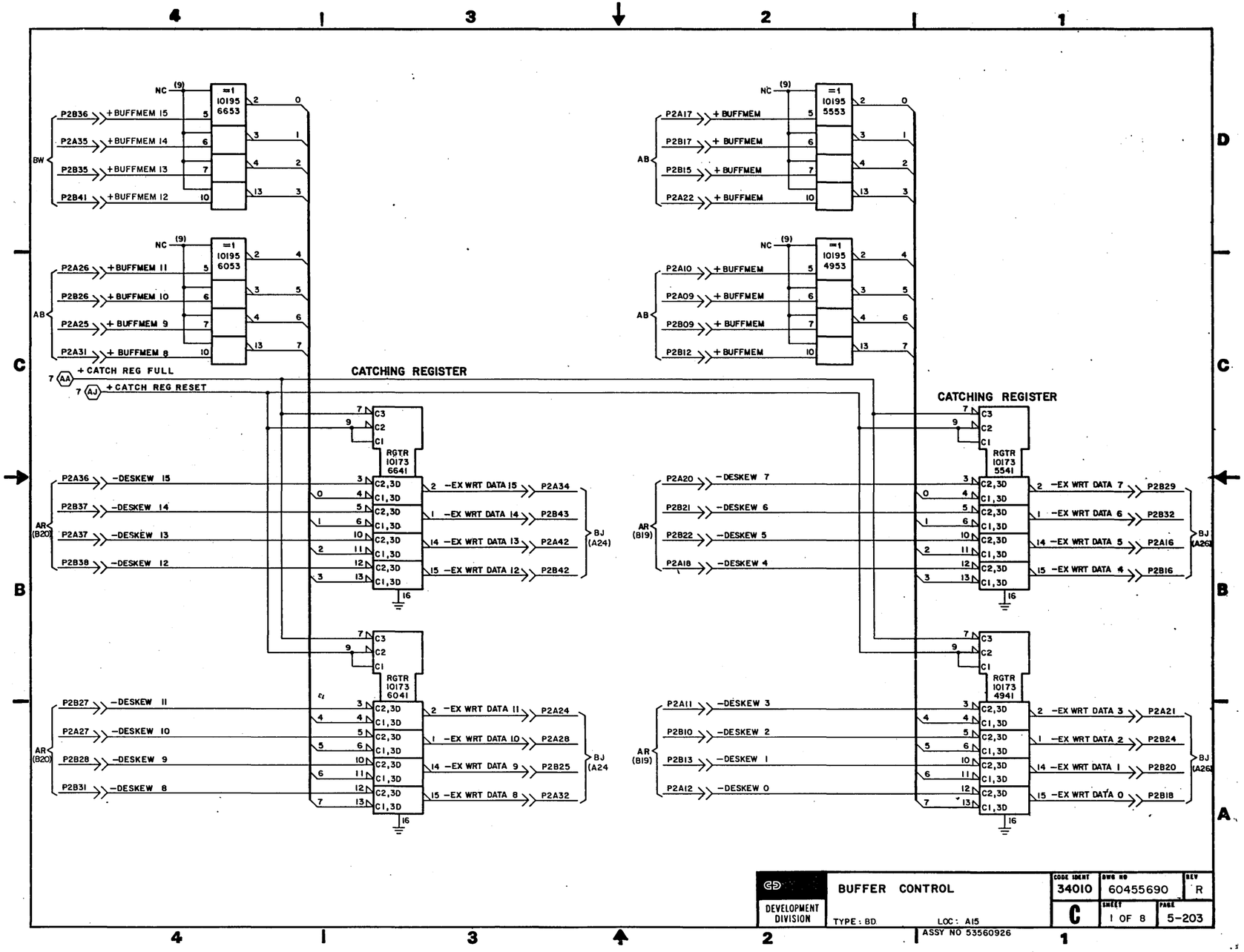

DESKEW 1 FULL
DESKEW 2 FULL
DESKEW 3 FULL
DESKEW 1 TO BUFFER
DESKEW 2 TO BUFFER
DESKEW 3 TO BUFFER
+LOAD DESKEW
+LD DESKEW RGTR
-CLK
+DESKEW TO BUFFER
+DESKEW TO BFR
+HDW MC
+RELOAD DESKEW RGTR
-DESKEW 1 FULL
-DESKEW 2 FULL
-DESKEW 3 FULL
+DESKEW 2 TO BUFFER
+STB DESKEW 3
+STB DESKEW 2
-DESKEW EMPTY
+DESKEW REG FULL
(ADDR FIELD FULL) +INPUT FULL 2
-LD BIT COUNT
NOTE:
PARENTHESES ( ) INDICATE THAT THE MODEL B CONTROLLER SIGNAL GOES TO A DIFFERENT PAK THAN THE MODEL A CONTROLLER SIGNAL.
DEVELOPMENT - DIVISION
DATA PATH CONTROL
TYPE: AT
LOC: B22
ASSY. NO. 11899014
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 2 OF 6
PAGE 5-198

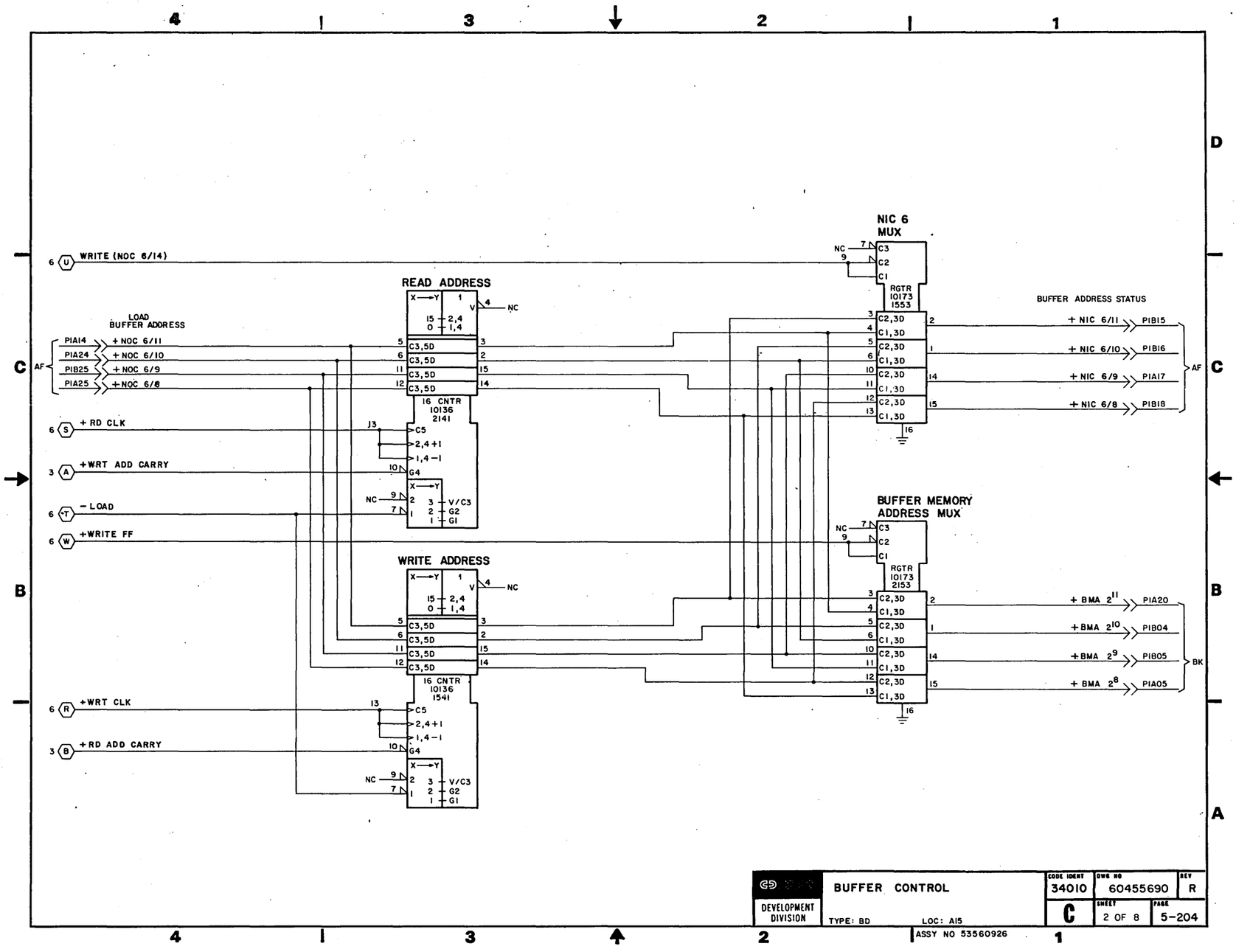

4
3
2
1
D
C
B
A
+WRITE GATE
+READ GATE
+WRT SYNC BYTE
+WRT ECC
+CONTROL WD REPLY
+MAINT (NOC 7/15)
+16 BIT MODE
-CLK
+START COND MET
SEQ IN PROGRESS
+SYNC BYTE SEARCH
BYTE COUNTER
START CONDITION
16 CNTR 10136 2629
-LOAD SHIFT RGTR
+16-BIT MODE
-LOAD DESKEW
+LD DESKEW RGTR
-LD DESKEW RGTR
DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AT
LOC: B22
ASSY. NO. 11899014
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 6
PAGE 5-199


SYNC COMPLETE
+CONTROL WD REPLY
+HDW MC
P1A41 +SYNC ERROR
+TERMINAL COUNT
-CLK
+HDW MC
-CLK
+SYNC BYTE MISCOMPARE
(NIC 1/10) +SYNC BYTE MISCOMPARE P2B09 AF
MISSING SYNC
(NIC 1/3) +SYNC SEARCH STATUS P2B12 AF
SYNC BYTE COUNTER
P2A28 +885 UNIT
(NOC 4/12) +SYNC BYTE SEARCH
P1B41
+RD DATA
FIRST ONE BIT DETECT
16 CNTR 10136 3205
-CONTROL WD REPLY
+SYNC BYTE SEARCH
+885 UNIT
DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AT
LOC: B22
ASSY. NO. 11899014
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 4 OF 6
PAGE 5-200

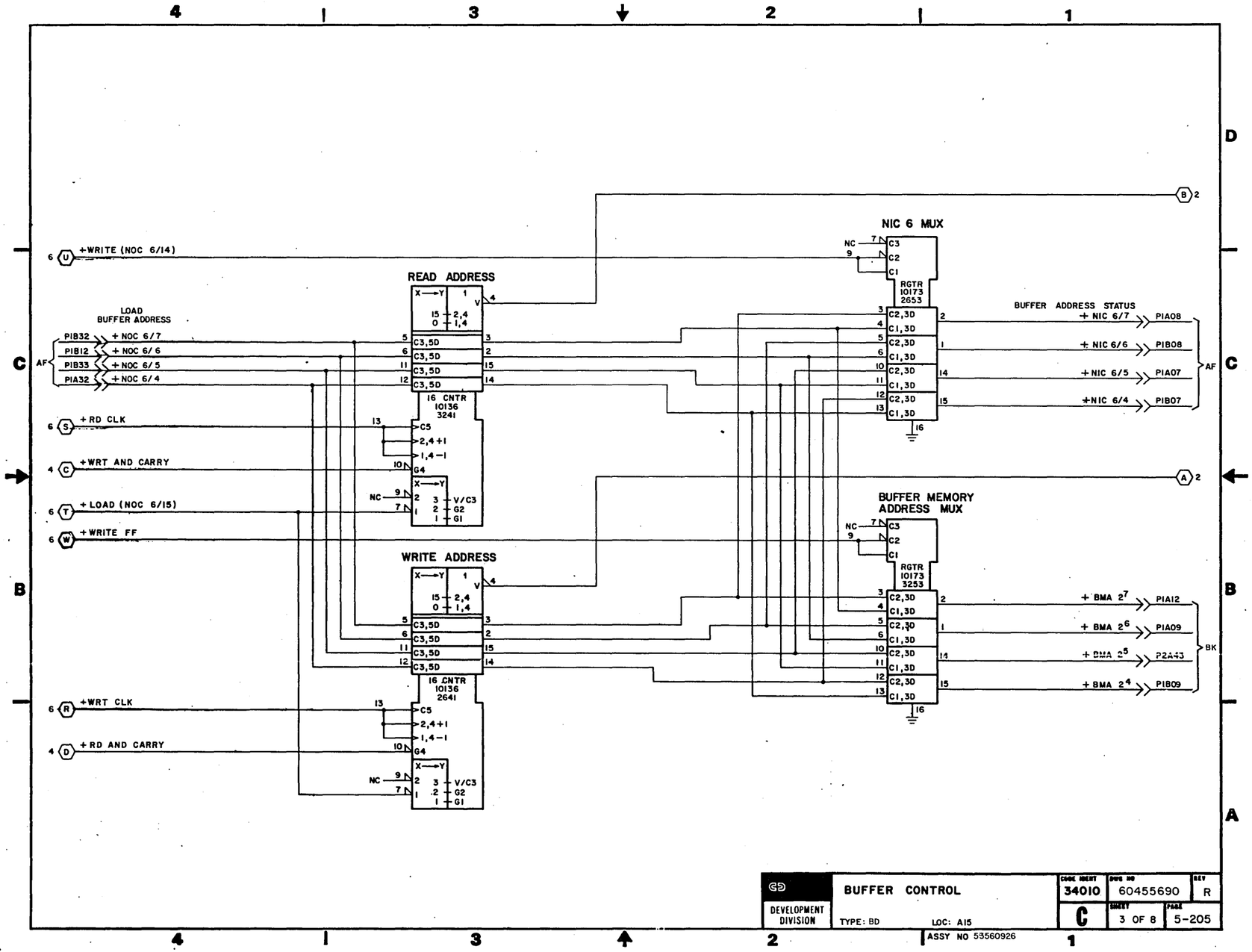

P2A16 +PROCESSOR CLK (85 NS)
P2B13
SEQ IN PROGRESS
P1A03 +CLK SEL 1
P2B04 +CLK
P2A03 +CLK SELECT 0
+WRITE GATE
+HDW MC
+START CONDITION
-LD BIT COUNT
+READ GATE
P2A24 +ENABLE ECC CLOCK
+WRITE GATE
P2B03 +ECC CLK
P1B30 +WRT ECC
+MC
P1B28 +DATA OUT
P1A26 +ECC OUT
+885 UNIT
P2B25 +844 RD CLK
P2A26 +885 RD CLK
P2B22 +844 WRT CLK
P2A22 +885 WRT CLK
P2A27 +844 RD DATA
P2B27 +885 RD DATA
P2A12 +CLK
+HDW MC
CHANGE CLOCK
GATE CLOCK
DELAY
DATA OUT
READ DATA
+CLK
+LOAD CLK (NIC 1/15)
+LOST CLK (NIC 1/15)
SHIFT RGTR
+CLK CNTR
+ENABLE ECC CLK
+WRT EEC
+WRITE DATA
+WRT CLK OUT
+DATA OUT
+RD DATA
P2A13
P2A20
P2A33
P1B19
P1A19
P1B24
P1A24
P2B16
P2B17
P2A04
P2A05
P2A19
P2B21
P1A27
P2B07
P2A07
P2B05
P2A11
P2B11
P2A10
P1A12
P1B11
10131 CD 4941
10131 CD 4929
10131 CD 4917
10131 CD 4429
10131 CD 4417
10131 CD 5541
10131 CD 2141
10195 4953
10195 6029
10195 4441
10195 6041
10195 1053
10104 3829
10104 6629
10101 5505
10101 1541
10101 3853
10101 3805
10105 0417
10105 4405
10105 5529
10113 3841
10173 2153
10173 5553
10174 4905
DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AT
LOC: B22
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 5 OF 6
PAGE 5-201
ASSY. NO. 11899014

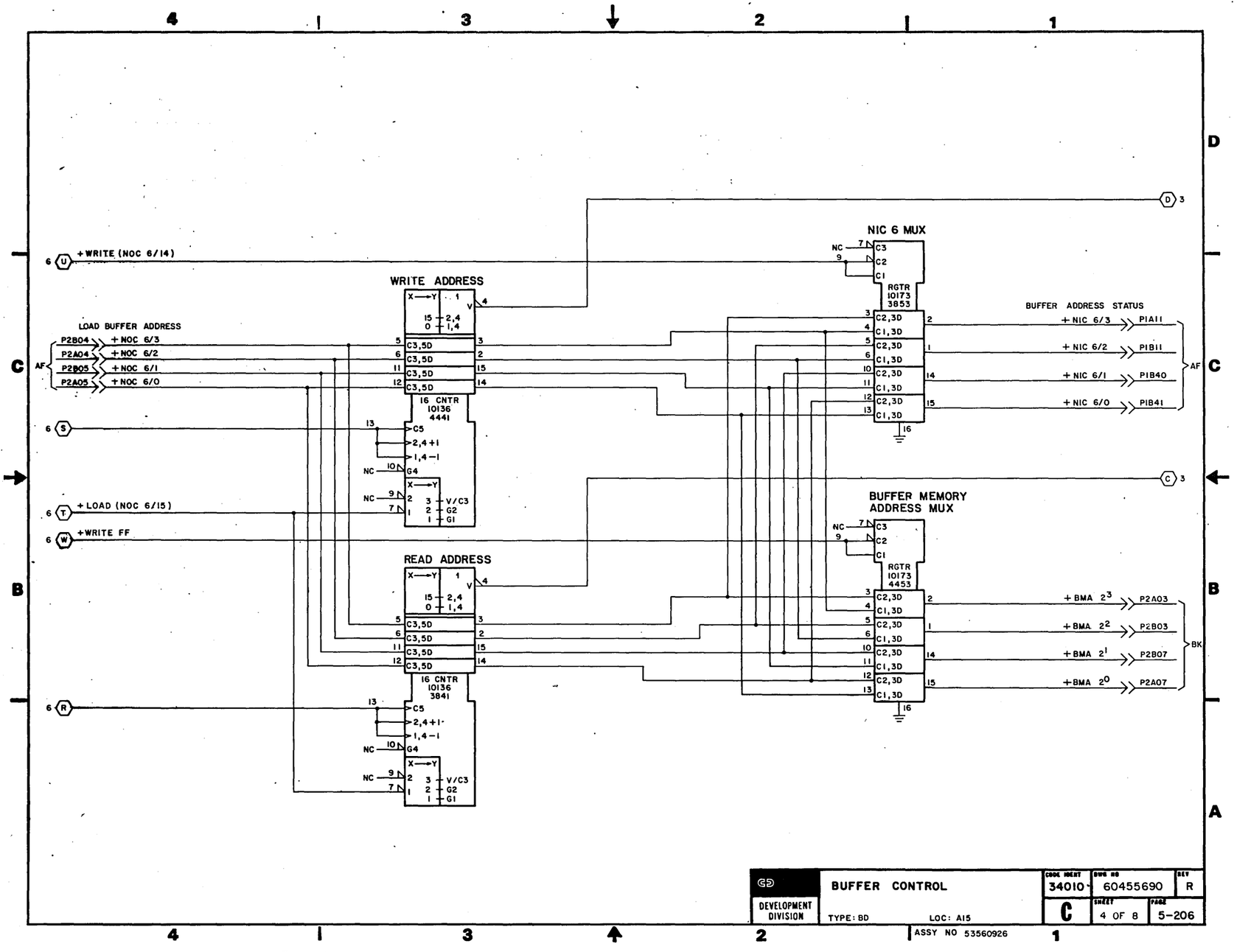

+LOAD HOLDING RGTR
P2A29
AR
P2B24
NC
P2A34
NC
+LOAD HOLDING RGTR
P2A35
AR
+OUTPUT RGTR RDY
P2B34
AS
+HDW MC
HOLDING RGTR FULL
+HOLDING RGTR EMPTY
PIB10
AS
+HDW MC
-LOAD DESKEW
-DESKEW 3 FULL
PIB40
AT (2)
+LOST DATA (NIC 1/1)
P2B33
AF
+LOST DATA (NIC 1/1)
AD 1
P2B43
P2A41
P2B41
P2A42
P2A37
P2B37
P2A36
P2B36
P2A43
P2B42
P2B38
P2A38
10101 0405
10131 CD 2141
10135 2129
10105 2605
10105 0417
10195 6041
10195 6053
10131 CD 6005
10109 6653
DATA PATH CONTROL
DEVELOPMENT DIVISION
TYPE: AT
LOC: B22
ASSY. NO. 11899014
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 6 OF 6
PAGE 5-202

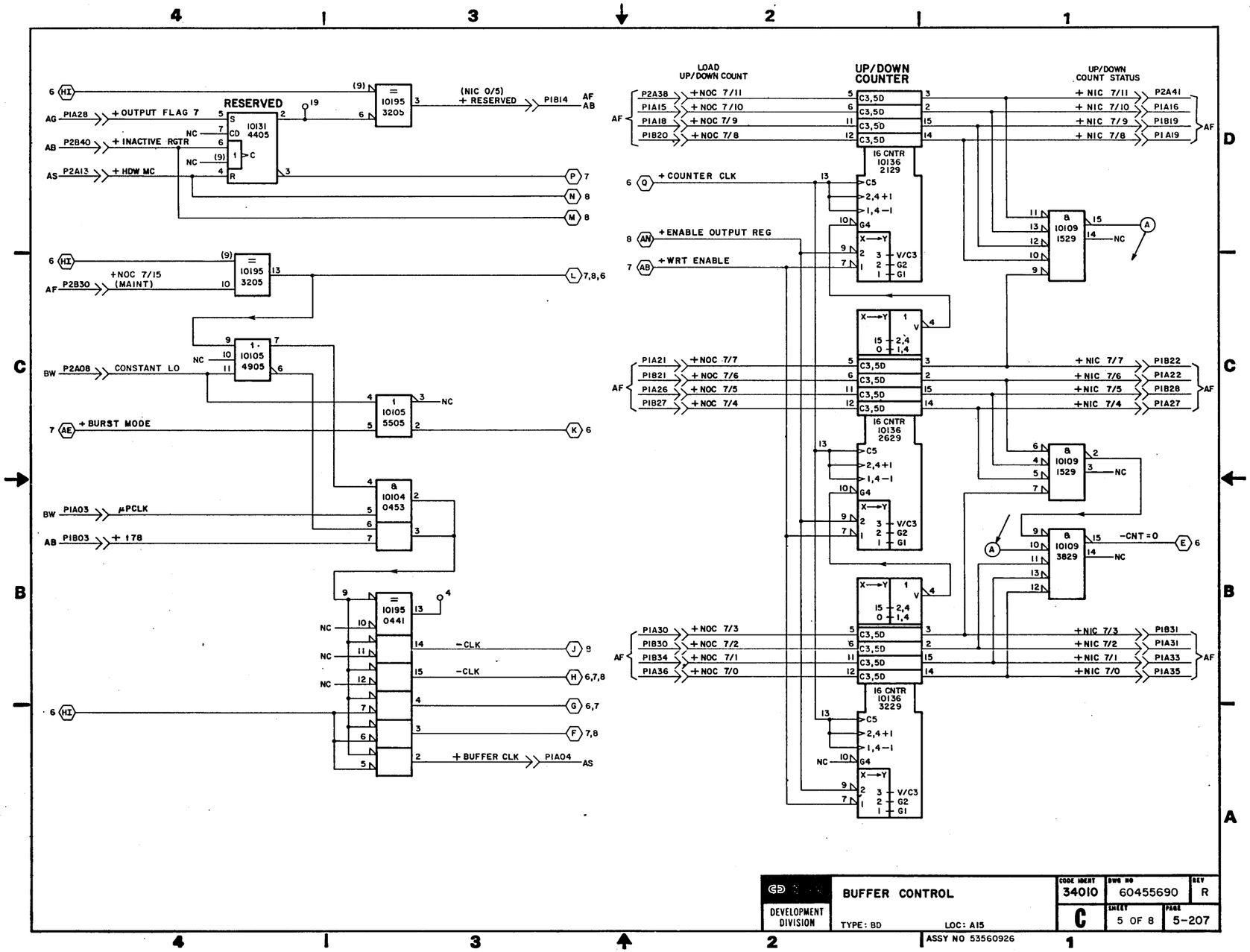

4
3
2
1
D
C
B
A
NC (9)
=1
10195
6653
P2B36 +BUFFMEM 15
P2A35 +BUFFMEM 14
P2B35 +BUFFMEM 13
P2B41 +BUFFMEM 12
BW
NC (9)
=1
10195
5553
P2A17 +BUFFMEM
P2B17 +BUFFMEM
P2B15 +BUFFMEM
P2A22 +BUFFMEM
AB
NC (9)
=1
10195
6053
P2A26 +BUFFMEM 11
P2B26 +BUFFMEM 10
P2A25 +BUFFMEM 9
P2A31 +BUFFMEM 8
AB
NC (9)
=1
10195
4953
P2A10 +BUFFMEM
P2A09 +BUFFMEM
P2B09 +BUFFMEM
P2B12 +BUFFMEM
AB
7 (AA) +CATCH REG FULL
7 (AJ) +CATCH REG RESET
CATCHING REGISTER
CATCHING REGISTER
RGTR
10173
6641
RGTR
10173
5541
RGTR
10173
6041
RGTR
10173
4941
C3
C2
C1
C2,3D
C1,3D
16
P2A36 -DESKEW 15
P2B37 -DESKEW 14
P2A37 -DESKEW 13
P2B38 -DESKEW 12
AR (B20)
-EX WRT DATA 15 P2A34
-EX WRT DATA 14 P2B43
-EX WRT DATA 13 P2A42
-EX WRT DATA 12 P2B42
BJ (A24)
P2A20 -DESKEW 7
P2B21 -DESKEW 6
P2B22 -DESKEW 5
P2A18 -DESKEW 4
AR (B19)
-EX WRT DATA 7 P2B29
-EX WRT DATA 6 P2B32
-EX WRT DATA 5 P2A16
-EX WRT DATA 4 P2B16
BJ (A26)
P2B27 -DESKEW 11
P2A27 -DESKEW 10
P2B28 -DESKEW 9
P2B31 -DESKEW 8
AR (B20)
-EX WRT DATA 11 P2A24
-EX WRT DATA 10 P2A28
-EX WRT DATA 9 P2B25
-EX WRT DATA 8 P2A32
BJ (A24)
P2A11 -DESKEW 3
P2B10 -DESKEW 2
P2B13 -DESKEW 1
P2A12 -DESKEW 0
AR (B19)
-EX WRT DATA 3 P2A21
-EX WRT DATA 2 P2B24
-EX WRT DATA 1 P2B20
-EX WRT DATA 0 P2B18
BJ (A26)
GD
DEVELOPMENT DIVISION
BUFFER CONTROL
TYPE: BD
LOC: A15
ASSY NO 53560926
CODE IDENT 34010
DWG NO 60455690
REV R
C
SHEET 1 OF 8
PAGE 5-203

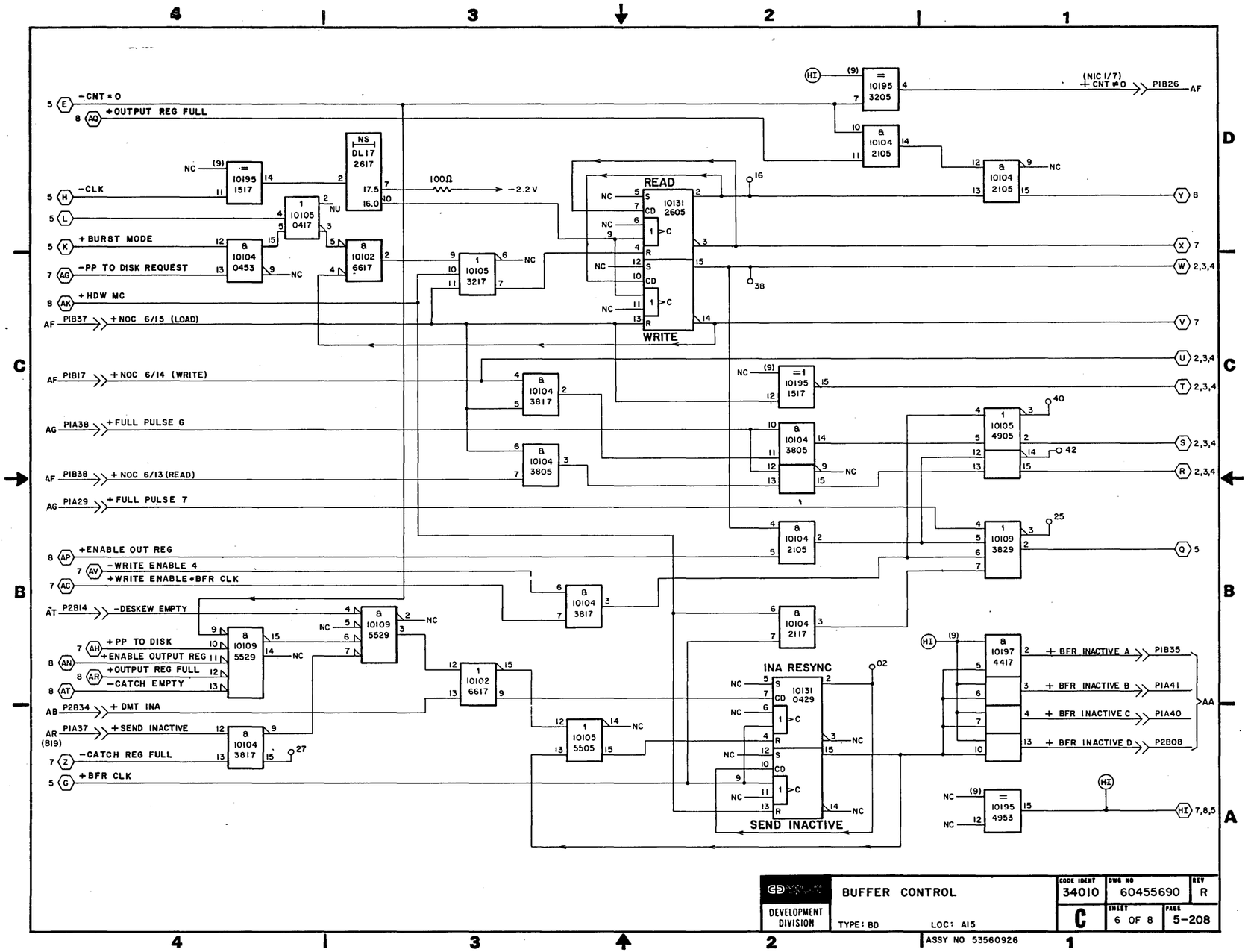


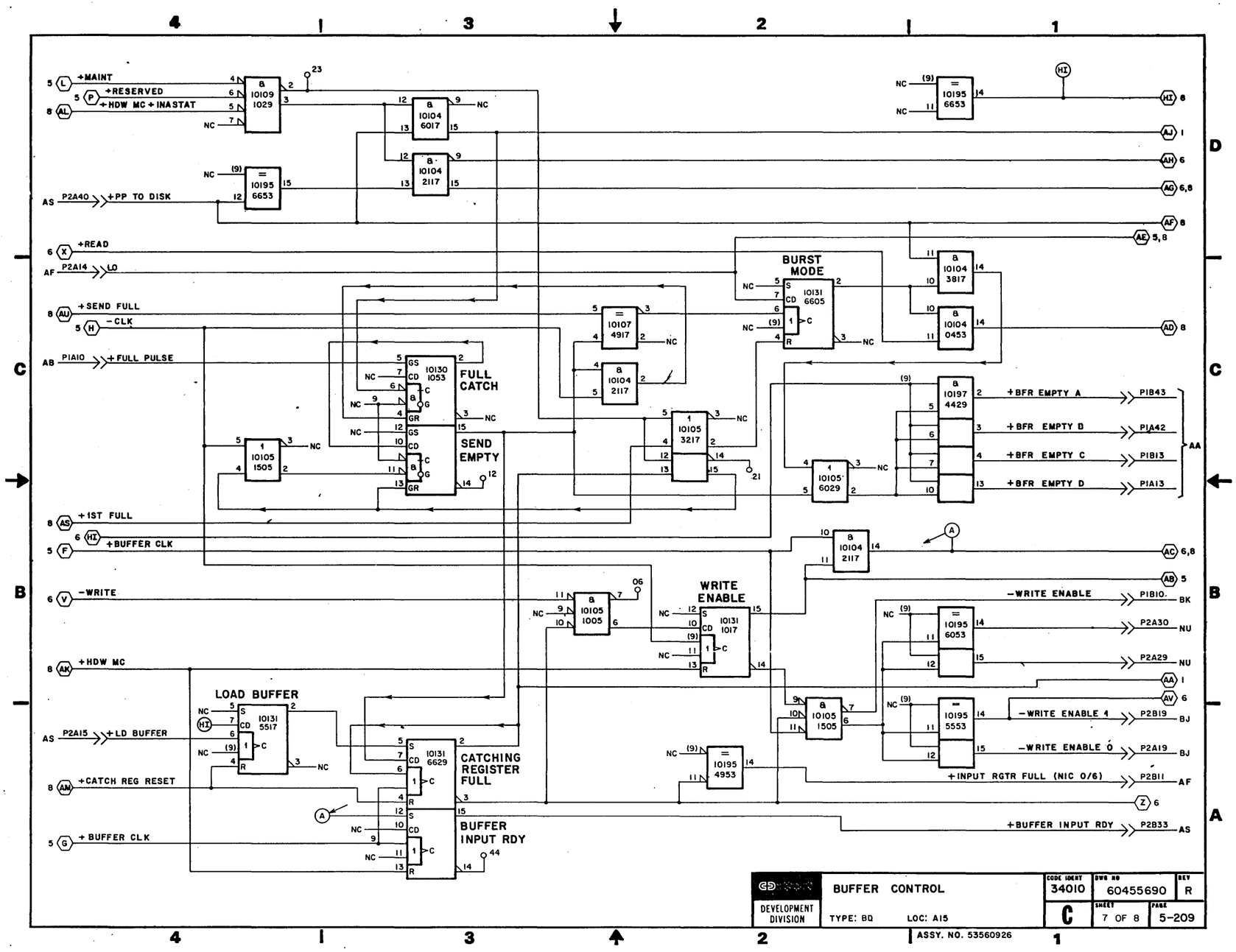
DEVELOPMENT DIVISION	BUFFER CONTROL	CODE IDENT 34010	DWG NO 60455690	REV R
TYPE: BD LOC: A15 ASSY NO 53560926		C	SHEET 2 OF 8	PAGE 5-204

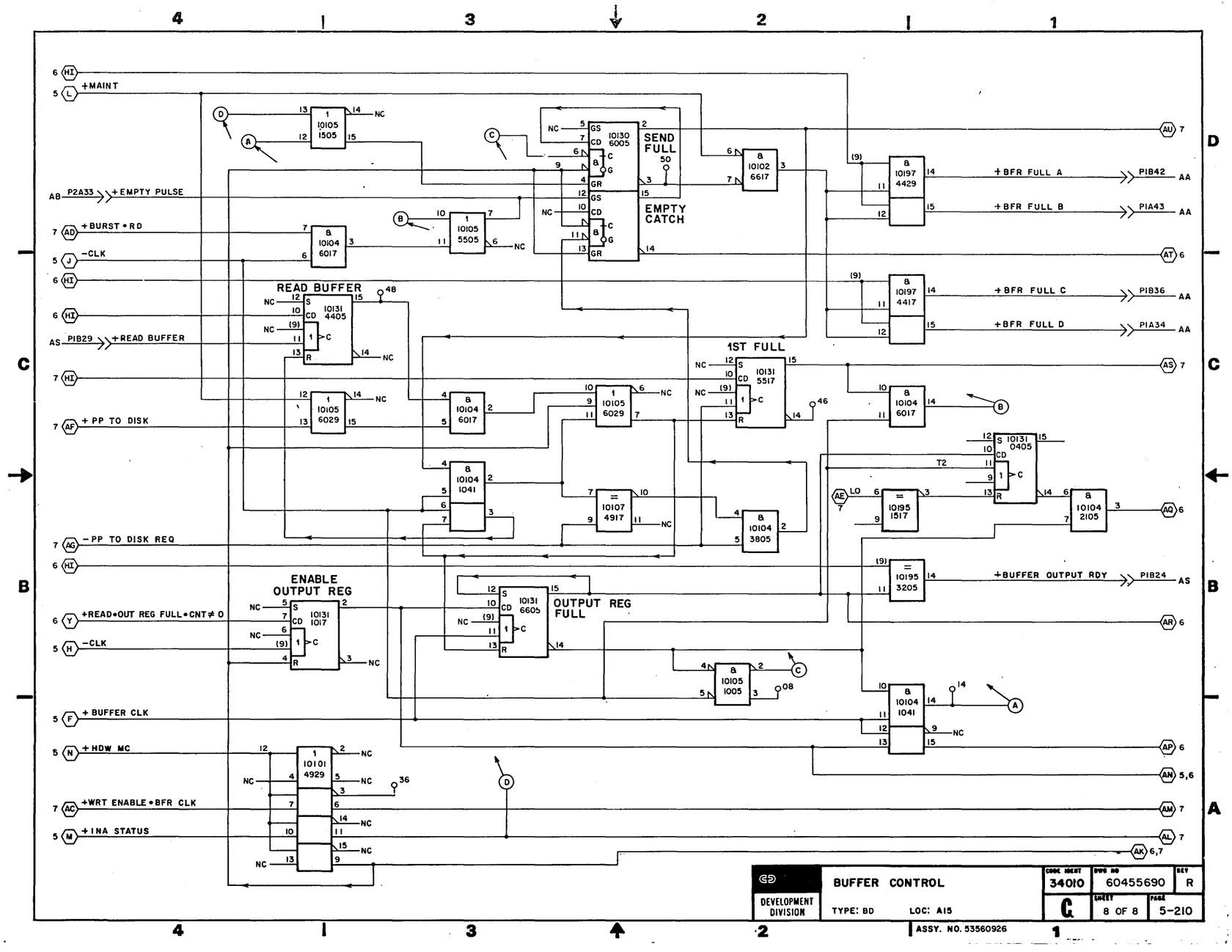

4
3
2
1
D
C
B
A
NIC 6 MUX
BUFFER MEMORY ADDRESS MUX
READ ADDRESS
WRITE ADDRESS
LOAD BUFFER ADDRESS
+WRITE (NOC 6/14)
+RD CLK
+WRT AND CARRY
+LOAD (NOC 6/15)
+WRITE FF
+WRT CLK
+RD AND CARRY
PIB32 + NOC 6/7
PIB12 + NOC 6/6
PIB33 + NOC 6/5
PIA32 + NOC 6/4
BUFFER ADDRESS STATUS
+ NIC 6/7 PIA08
+ NIC 6/6 PIB08
+ NIC 6/5 PIA07
+NIC 6/4 PIB07
+ BMA 2^7 PIA12
+ BMA 2^6 PIA09
+ BMA 2^5 P2A43
+ BMA 2^4 PIB09
RGTR 10173 2653
16 CNTR 10136 3241
16 CNTR 10136 2641
C3,5D
C2,3D
C1,3D
C5
2,4+1
1,4-1
G4
V/C3
G2
G1
AF
BK
GD
DEVELOPMENT DIVISION
BUFFER CONTROL
TYPE: BD
LOC: A15
ASSY NO 53560926
CAGE IDENT 34010
DWG NO 60455690
REV R
SIZE C
SHEET 3 OF 8
PAGE 5-205

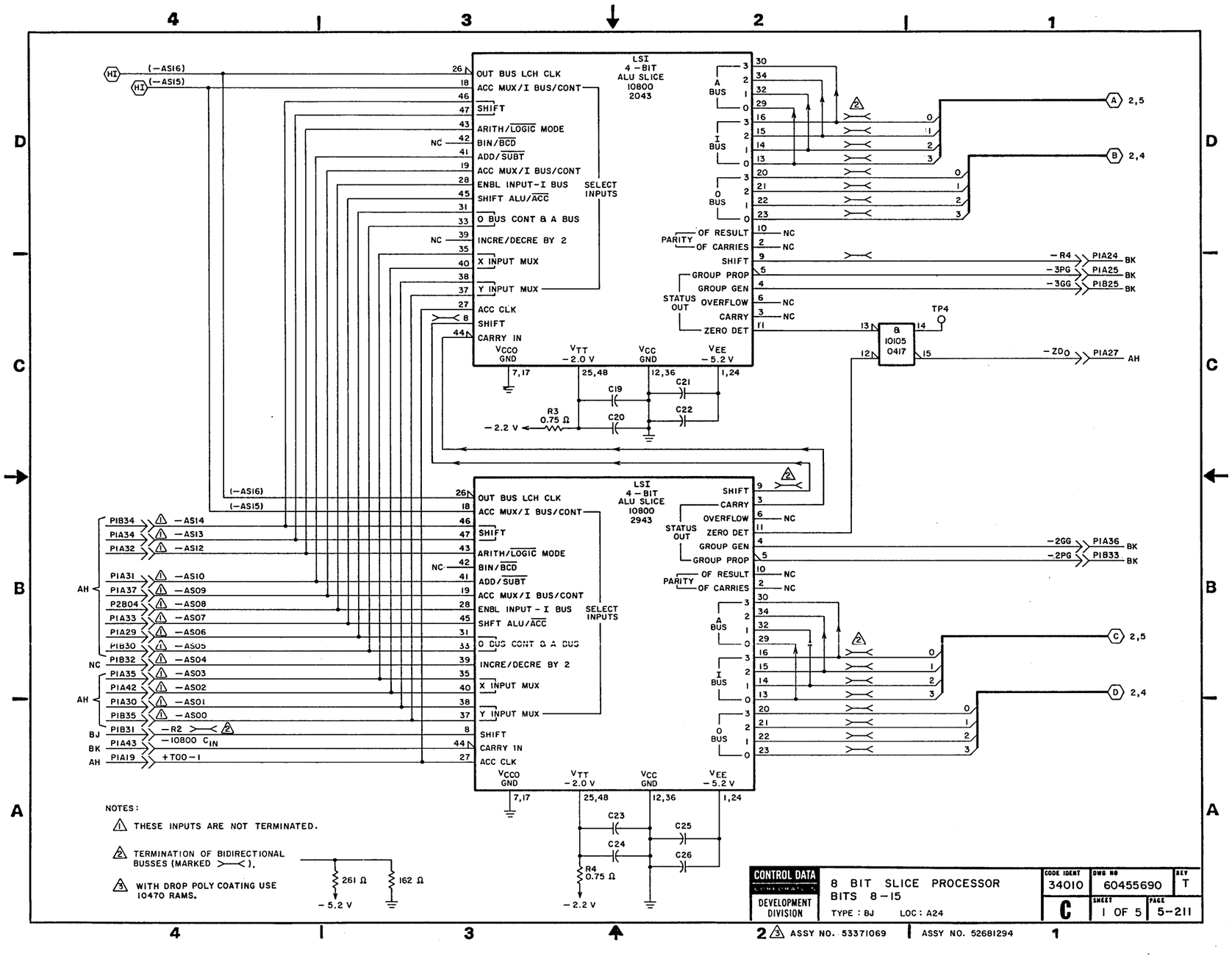

+WRITE (NOC 6/14)
WRITE ADDRESS
LOAD BUFFER ADDRESS
P2B04 +NOC 6/3
P2A04 +NOC 6/2
P2B05 +NOC 6/1
P2A05 +NOC 6/0
AF
C3,5D
16 CNTR 10136 4441
C5
2,4+1
1,4-1
G4
V/C3
G2
G1
+LOAD (NOC 6/15)
+WRITE FF
READ ADDRESS
16 CNTR 10136 3841
NIC 6 MUX
RGTR 10173 3853
C3
C2
C1
C2,3D
C1,3D
BUFFER ADDRESS STATUS
+NIC 6/3 PIA11
+NIC 6/2 PIB11
+NIC 6/1 PIB40
+NIC 6/0 PIB41
BUFFER MEMORY ADDRESS MUX
RGTR 10173 4453
+BMA 2^3 P2A03
+BMA 2^2 P2B03
+BMA 2^1 P2B07
+BMA 2^0 P2A07
BK
BUFFER CONTROL
DEVELOPMENT DIVISION
TYPE: BD
LOC: A15
ASSY NO 53560926
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 4 OF 8
PAGE 5-206

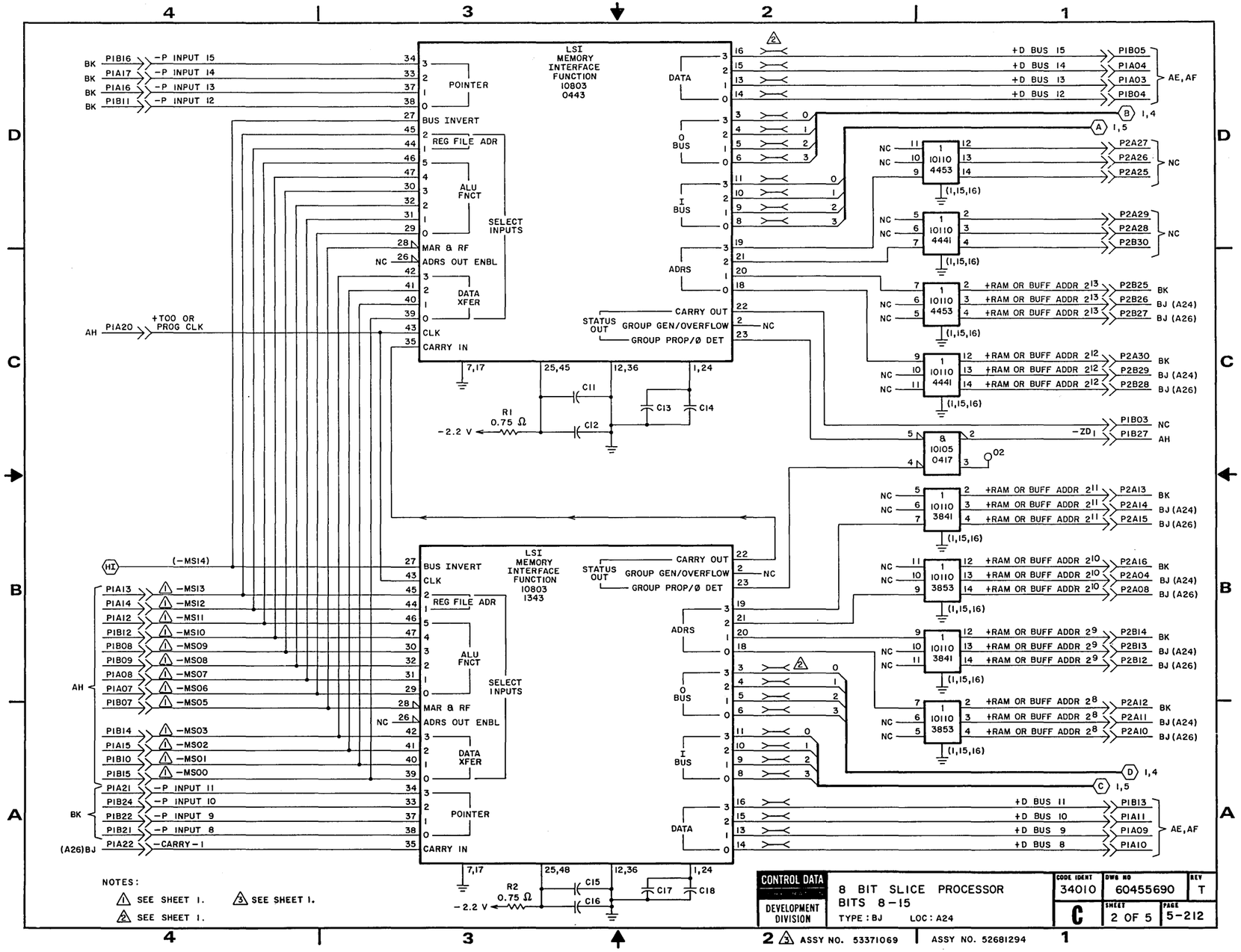

RESERVED
10131 4405
10195 3205
(NIC 0/5) + RESERVED
P1B14
AF
AB
+OUTPUT FLAG 7
P1A28
+INACTIVE RGTR
P2B40
+HDW MC
P2A13
10195 3205
+NOC 7/15 (MAINT)
P2B30
7,8,6
10105 4905
CONSTANT LO
P2A08
+BURST MODE
10105 5505
10104 0453
µPCLK
P1A03
+178
P1B03
10195 0441
-CLK
-CLK
+BUFFER CLK
P1A04
LOAD UP/DOWN COUNT
UP/DOWN COUNTER
UP/DOWN COUNT STATUS
+NOC 7/11
+NOC 7/10
+NOC 7/9
+NOC 7/8
C3,5D
16 CNTR 10136 2129
+COUNTER CLK
+ENABLE OUTPUT REG
+WRT ENABLE
+NIC 7/11
+NIC 7/10
+NIC 7/9
+NIC 7/8
10109 1529
+NOC 7/7
+NOC 7/6
+NOC 7/5
+NOC 7/4
16 CNTR 10136 2629
+NIC 7/7
+NIC 7/6
+NIC 7/5
+NIC 7/4
-CNT=0
+NOC 7/3
+NOC 7/2
+NOC 7/1
+NOC 7/0
16 CNTR 10136 3229
+NIC 7/3
+NIC 7/2
+NIC 7/1
+NIC 7/0
BUFFER CONTROL
DEVELOPMENT DIVISION
TYPE: BD
LOC: A15
ASSY NO 53560926
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 5 OF 8
PAGE 5-207

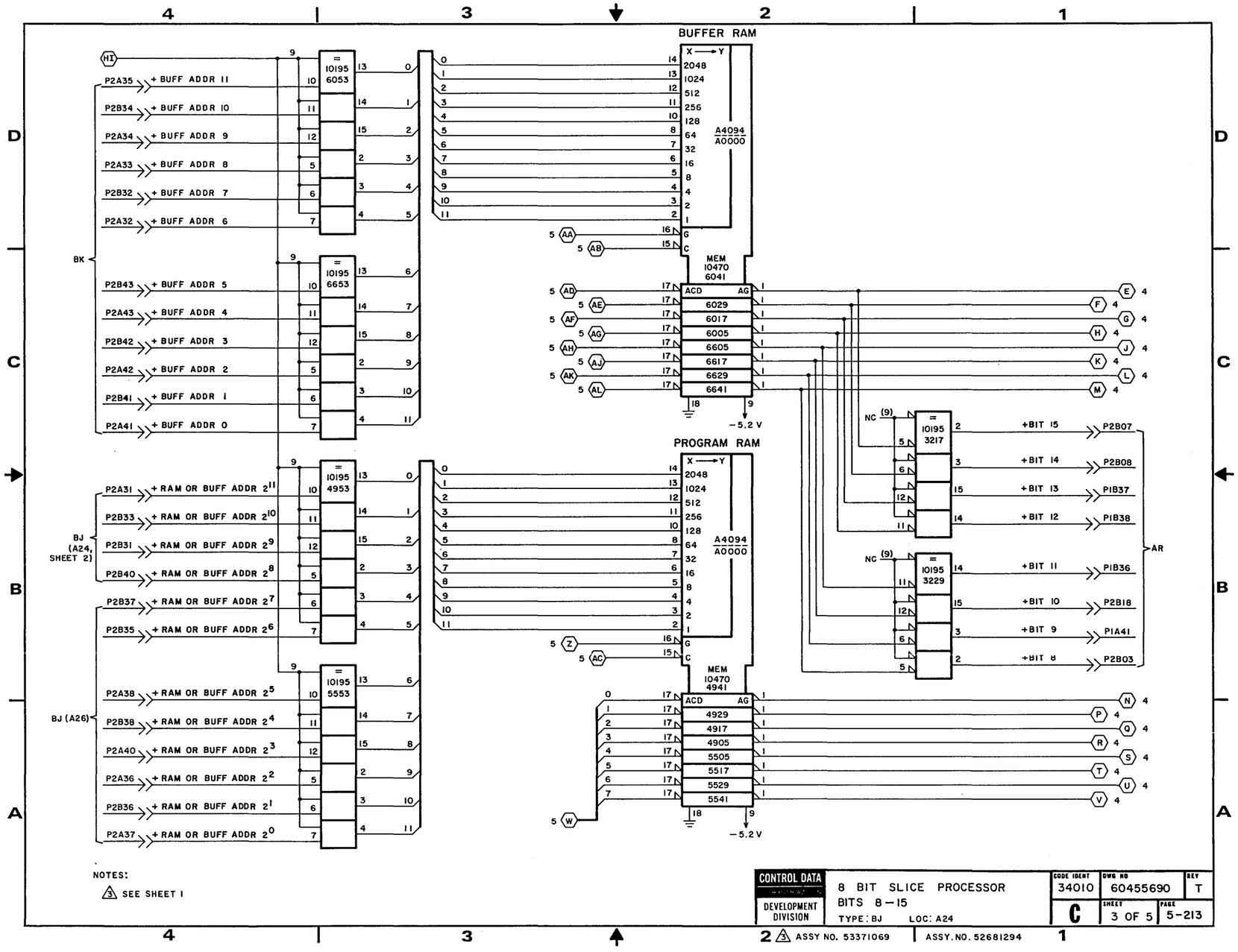

-CNT = 0
+OUTPUT REG FULL
-CLK
+BURST MODE
-PP TO DISK REQUEST
+HDW MC
PIB37 +NOC 6/15 (LOAD)
PIB17 +NOC 6/14 (WRITE)
PIA38 +FULL PULSE 6
PIB38 +NOC 6/13 (READ)
PIA29 +FULL PULSE 7
+ENABLE OUT REG
-WRITE ENABLE 4
+WRITE ENABLE•BFR CLK
P2B14 -DESKEW EMPTY
+PP TO DISK
+ENABLE OUTPUT REG
+OUTPUT REG FULL
-CATCH EMPTY
P2B34 + DMT INA
PIA37 (B19) +SEND INACTIVE
-CATCH REG FULL
+BFR CLK
100Ω
-2.2V
READ
WRITE
INA RESYNC
SEND INACTIVE
(NIC 1/7) +CNT ≠ 0 PIB26 AF
+BFR INACTIVE A PIB35
+BFR INACTIVE B PIA41
+BFR INACTIVE C PIA40
+BFR INACTIVE D P2B08
AA
BUFFER CONTROL
DEVELOPMENT DIVISION
TYPE: BD
LOC: A15
ASSY NO 53560926
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 6 OF 8
PAGE 5-208

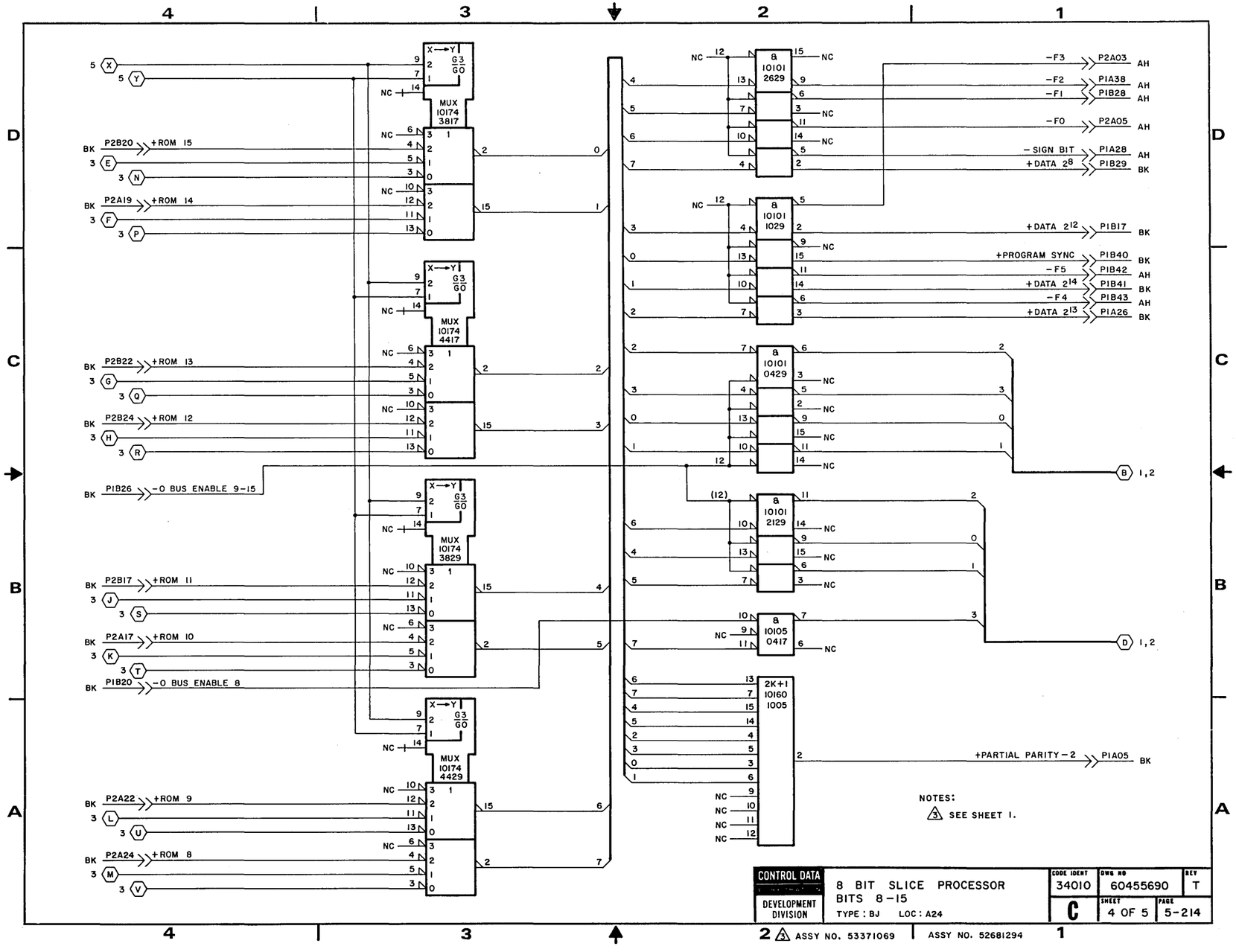

+MAINT
+RESERVED
+HDW MC + INASTAT
8 10109 1029
8 10104 6017
8 10104 2117
(9) = 10195 6653
AS P2A40 +PP TO DISK
+READ
AF P2A14 LO
+SEND FULL
-CLK
AB P1A10 +FULL PULSE
GS CD 10130 1053 FULL CATCH
SEND EMPTY
1 10105 1505
= 10107 4917
1 10105 3217
+1ST FULL
+BUFFER CLK
-WRITE
+HDW MC
LOAD BUFFER
S CD 10131 5517
AS P2A15 +LD BUFFER
+CATCH REG RESET
+BUFFER CLK
S CD 10131 6629 CATCHING REGISTER FULL
BUFFER INPUT RDY
8 10105 1005
WRITE ENABLE
S CD 10131 1017
BURST MODE
S CD 10131 6605
8 10104 3817
8 10104 0453
= 10195 6653
8 10197 4429
+BFR EMPTY A P1B43
+BFR EMPTY B P1A42
+BFR EMPTY C P1B13
+BFR EMPTY D P1A13
AA
1 10105 6029
8 10104 2117
-WRITE ENABLE P1B10. BK
= 10195 6053 P2A30 NU
P2A29 NU
= 10195 5553
-WRITE ENABLE 1 P2B19 BJ
-WRITE ENABLE 0 P2A19 BJ
= 10195 4953
+INPUT RGTR FULL (NIC 0/6) P2B11 AF
+BUFFER INPUT RDY P2B33 AS
AC 6,8
AB 5
AA 1
AV 6
Z 6
AJ 1
AH 6
AG 6,8
AF 8
AE 5,8
AD 8
HI 8
BUFFER CONTROL
DEVELOPMENT DIVISION
TYPE: BQ LOC: A15
ASSY. NO. 53560926
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 7 OF 8
PAGE 5-209

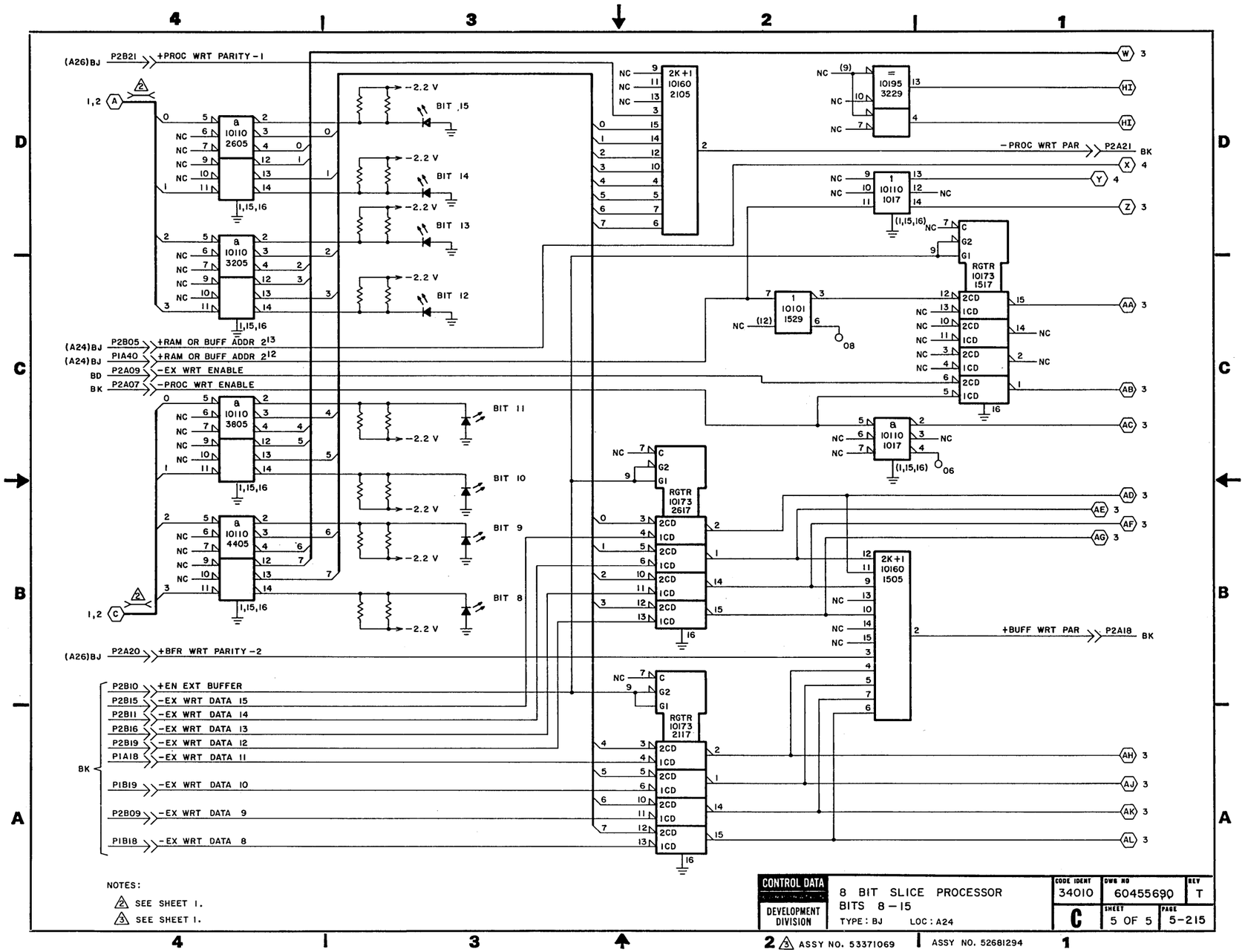

6 HI
5 L +MAINT
AB P2A33 +EMPTY PULSE
7 AD +BURST • RD
5 J -CLK
6 HI
6 HI
AS PIB29 +READ BUFFER
7 HI
7 AF + PP TO DISK
7 AG - PP TO DISK REQ
6 HI
6 Y +READ•OUT REG FULL•CNT≠ 0
5 H -CLK
5 F + BUFFER CLK
5 N + HDW MC
7 AC +WRT ENABLE • BFR CLK
5 M + INA STATUS
READ BUFFER
ENABLE OUTPUT REG
SEND FULL
EMPTY CATCH
OUTPUT REG FULL
1ST FULL
10105 1505
10105 5505
10104 6017
10131 4405
10105 6029
10104 1041
10107 4917
10130 6005
10102 6617
10131 5517
10104 3805
10131 1017
10101 4929
10131 6605
10105 1005
10197 4429
10197 4417
10131 0405
10195 1517
10104 2105
10195 3205
10104 1041
+BFR FULL A
+BFR FULL B
+BFR FULL C
+BFR FULL D
+BUFFER OUTPUT RDY
PIB42 AA
PIA43 AA
PIB36 AA
PIA34 AA
PIB24 AS
AU 7
AT 6
AS 7
AQ 6
AR 6
AP 6
AN 5,6
AM 7
AL 7
AK 6,7
BUFFER CONTROL
TYPE: BD LOC: A15
DEVELOPMENT DIVISION
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 8 OF 8
PAGE 5-210
ASSY. NO. 53560926


LSI 4-BIT ALU SLICE 10800 2043
OUT BUS LCH CLK
ACC MUX/I BUS/CONT
SHIFT
ARITH/LOGIC MODE
BIN/BCD
ADD/SUBT
ACC MUX/I BUS/CONT
ENBL INPUT-I BUS
SHIFT ALU/ACC
O BUS CONT & A BUS
INCRE/DECRE BY 2
X INPUT MUX
Y INPUT MUX
ACC CLK
SHIFT
CARRY IN
SELECT INPUTS
A BUS
I BUS
O BUS
PARITY OF RESULT
PARITY OF CARRIES
STATUS OUT SHIFT
GROUP PROP
GROUP GEN
OVERFLOW
CARRY
ZERO DET
VCCO GND
VTT -2.0 V
VCC GND
VEE -5.2 V
C19
C20
C21
C22
R3 0.75 Ω
-2.2 V
TP4
10105 0417
-R4
-3PG
-3GG
-2GG
-2PG
-ZDO
PIA24 BK
PIA25 BK
PIB25 BK
PIA36 BK
PIB33 BK
PIA27 AH
(-AS16)
(-AS15)
-AS14
-AS13
-AS12
-AS10
-AS09
-AS08
-AS07
-AS06
-AS05
-AS04
-AS03
-AS02
-AS01
-AS00
-R2
-10800 CIN
+TOO-1
C23
C24
C25
C26
R4 0.75 Ω
261 Ω
162 Ω
-5.2 V
NOTES:
1 THESE INPUTS ARE NOT TERMINATED.
2 TERMINATION OF BIDIRECTIONAL BUSSES (MARKED ><).
3 WITH DROP POLY COATING USE 10470 RAMS.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 8-15
TYPE : BJ LOC : A24
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET 1 OF 5
PAGE 5-211
ASSY NO. 53371069
ASSY NO. 52681294


LSI MEMORY INTERFACE FUNCTION 10803 0443
POINTER
REG FILE ADR
ALU FNCT
DATA XFER
SELECT INPUTS
BUS INVERT
MAR & RF
ADRS OUT ENBL
CLK
CARRY IN
DATA
O BUS
I BUS
ADRS
CARRY OUT
STATUS OUT
GROUP GEN/OVERFLOW
GROUP PROP/Ø DET
PIBI6 -P INPUT 15
PIAI7 -P INPUT 14
PIAI6 -P INPUT 13
PIBII -P INPUT 12
PIA20 +TOO OR PROG CLK
+D BUS 15
+D BUS 14
+D BUS 13
+D BUS 12
PIB05
PIA04
PIA03
PIB04
AE, AF
R1 0.75 Ω
-2.2 V
C11
C12
C13
C14
7,17
25,45
12,36
1,24
10110 4453
10110 4441
10110 3841
10110 3853
10105 0417
+RAM OR BUFF ADDR 2^13
+RAM OR BUFF ADDR 2^12
+RAM OR BUFF ADDR 2^11
+RAM OR BUFF ADDR 2^10
+RAM OR BUFF ADDR 2^9
+RAM OR BUFF ADDR 2^8
P2A27
P2A26
P2A25
P2A29
P2A28
P2B30
P2B25
P2B26
P2B27
P2B30
P2A30
P2B29
P2B28
P1B03
P1B27
-ZD1
P2A13
P2A14
P2A15
P2A16
P2A04
P2A08
P2B14
P2B13
P2B12
P2A12
P2A11
P2A10
BK
BJ (A24)
BJ (A26)
NC
(-MS14)
PIAI3 -MSI3
PIAI4 -MSI2
PIAI2 -MSI1
PIBI2 -MSI0
PIB08 -MS09
PIB09 -MS08
PIA08 -MS07
PIA07 -MS06
PIB07 -MS05
PIBI4 -MS03
PIAI5 -MS02
PIBI0 -MS01
PIBI5 -MS00
PIA21 -P INPUT 11
PIB24 -P INPUT 10
PIB22 -P INPUT 9
PIB21 -P INPUT 8
PIA22 -CARRY-1
(A26)BJ
R2 0.75 Ω
-2.2 V
C15
C16
C17
C18
+D BUS 11
+D BUS 10
+D BUS 9
+D BUS 8
PIBI3
PIAI1
PIA09
PIA10
NOTES:
1 SEE SHEET 1.
2 SEE SHEET 1.
3 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 8-15
TYPE : BJ LOC : A24
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET 2 OF 5
PAGE 5-212
ASSY NO. 53371069
ASSY NO. 52681294


BUFFER RAM
PROGRAM RAM
MEM 10470 6041
MEM 10470 4941
A4094 A0000
10195 6053
10195 6653
10195 4953
10195 5553
10195 3217
10195 3229
+ BUFF ADDR 11
+ BUFF ADDR 10
+ BUFF ADDR 9
+ BUFF ADDR 8
+ BUFF ADDR 7
+ BUFF ADDR 6
+ BUFF ADDR 5
+ BUFF ADDR 4
+ BUFF ADDR 3
+ BUFF ADDR 2
+ BUFF ADDR 1
+ BUFF ADDR 0
+ RAM OR BUFF ADDR 2^11
+ RAM OR BUFF ADDR 2^10
+ RAM OR BUFF ADDR 2^9
+ RAM OR BUFF ADDR 2^8
+ RAM OR BUFF ADDR 2^7
+ RAM OR BUFF ADDR 2^6
+ RAM OR BUFF ADDR 2^5
+ RAM OR BUFF ADDR 2^4
+ RAM OR BUFF ADDR 2^3
+ RAM OR BUFF ADDR 2^2
+ RAM OR BUFF ADDR 2^1
+ RAM OR BUFF ADDR 2^0
+BIT 15
+BIT 14
+BIT 13
+BIT 12
+BIT 11
+BIT 10
+BIT 9
+BIT 8
-5.2 V
NOTES:
3 SEE SHEET 1
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 8-15
TYPE: BJ LOC: A24
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET C
3 OF 5
PAGE 5-213
3 ASSY NO. 53371069
ASSY. NO. 52681294


MUX 10174 3817
MUX 10174 4417
MUX 10174 3829
MUX 10174 4429
8 10101 2629
8 10101 1029
8 10101 0429
8 10101 2129
8 10105 0417
2K+1 10160 1005
P2B20 +ROM 15
P2A19 +ROM 14
P2B22 +ROM 13
P2B24 +ROM 12
P1B26 -O BUS ENABLE 9-15
P2B17 +ROM 11
P2A17 +ROM 10
P1B20 -O BUS ENABLE 8
P2A22 +ROM 9
P2A24 +ROM 8
-F3 P2A03 AH
-F2 P1A38 AH
-F1 P1B28 AH
-F0 P2A05 AH
-SIGN BIT P1A28 AH
+DATA 2^8 P1B29 BK
+DATA 2^12 P1B17 BK
+PROGRAM SYNC P1B40 BK
-F5 P1B42 AH
+DATA 2^14 P1B41 BK
-F4 P1B43 AH
+DATA 2^13 P1A26 BK
+PARTIAL PARITY-2 P1A05 BK
B 1,2
D 1,2
NOTES:
3 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 8-15
TYPE : BJ LOC : A24
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET C
4 OF 5
PAGE 5-214
2 3 ASSY NO. 53371069
ASSY NO. 52681294



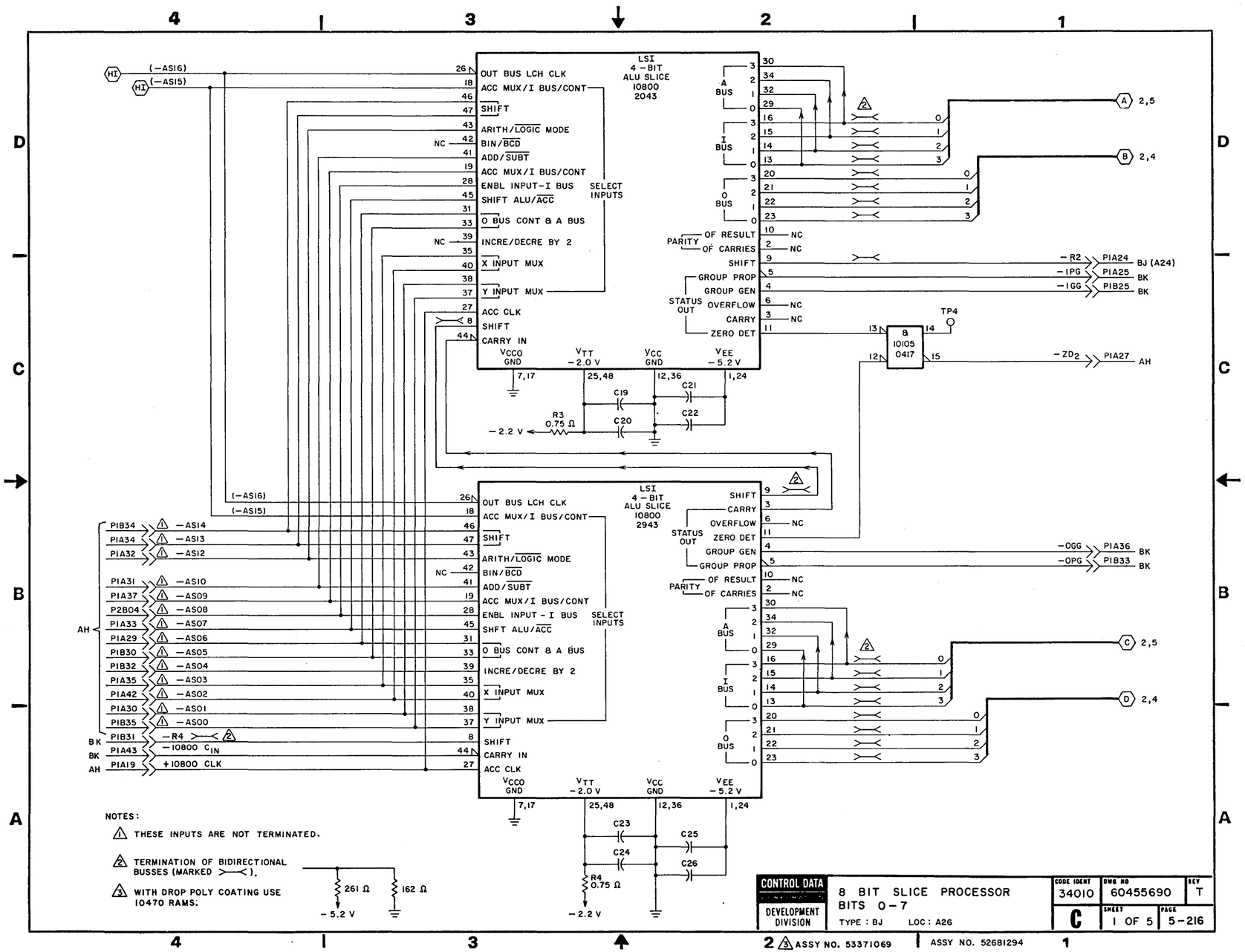
NOTES:

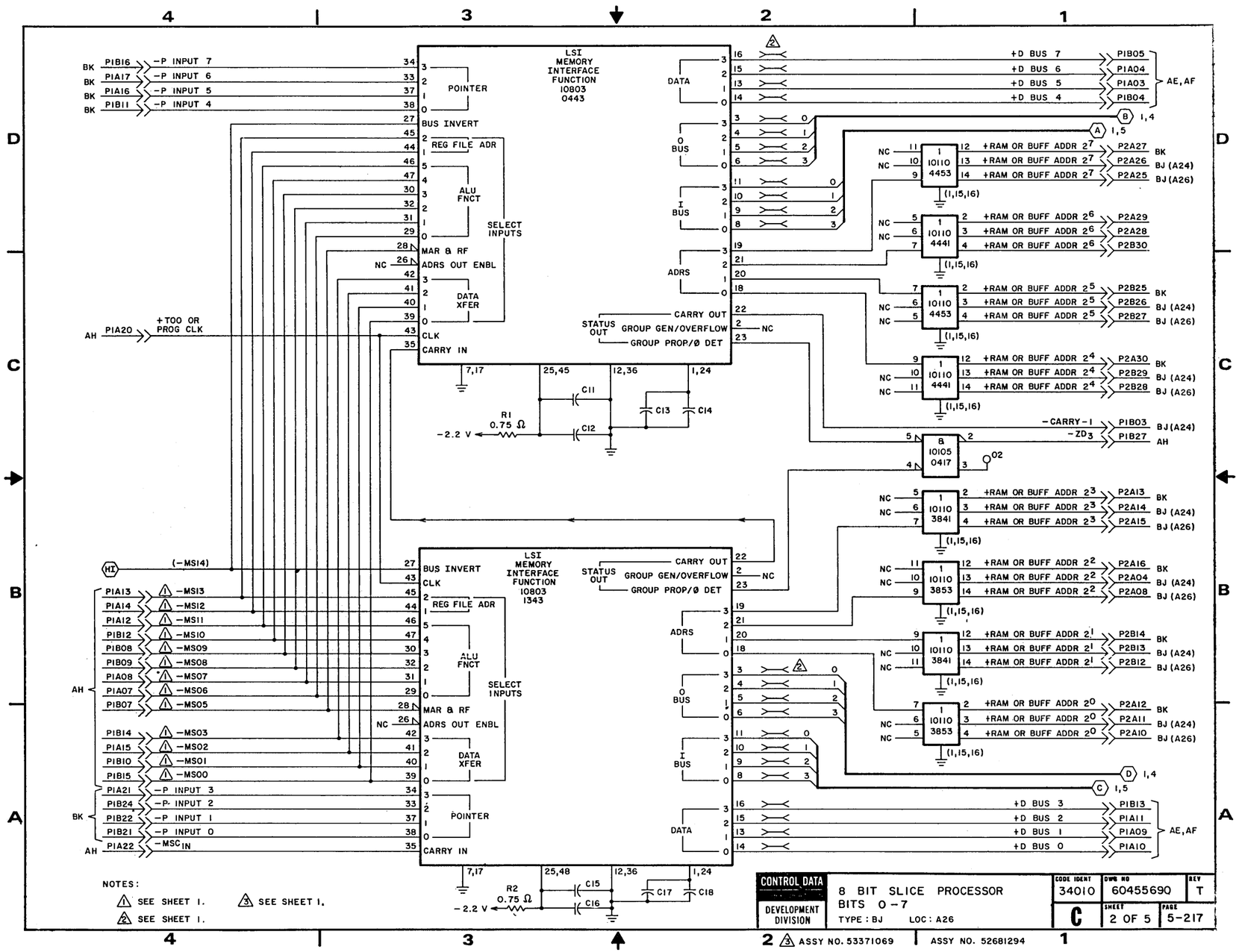
2 SEE SHEET 1.

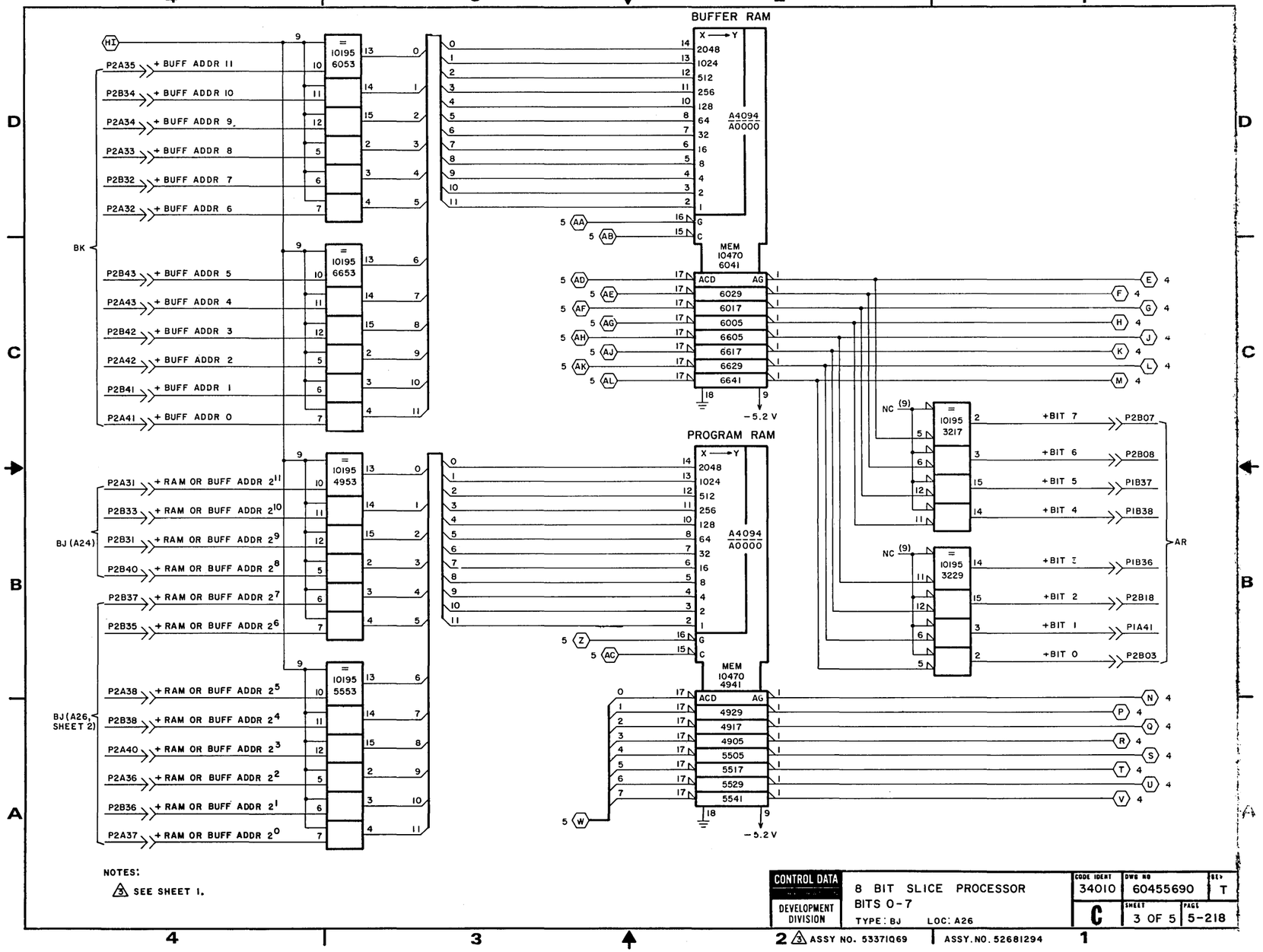
3 SEE SHEET 1.

CONTROL DATA DEVELOPMENT DIVISION	8 BIT SLICE PROCESSOR BITS 8-15 TYPE: BJ LOC: A24	CODE IDENT 34010	DWG NO 60455690	REV T
		C	SHEET 5 OF 5	PAGE 5-215

2 3 ASSY NO. 53371069 | ASSY NO. 52681294


LSI 4-BIT ALU SLICE 10800 2043
OUT BUS LCH CLK
ACC MUX/I BUS/CONT
SHIFT
ARITH/LOGIC MODE
BIN/BCD
ADD/SUBT
ACC MUX/I BUS/CONT
ENBL INPUT-I BUS
SHIFT ALU/ACC
O BUS CONT & A BUS
INCRE/DECRE BY 2
X INPUT MUX
Y INPUT MUX
ACC CLK
SHIFT
CARRY IN
SELECT INPUTS
A BUS
I BUS
O BUS
PARITY OF RESULT
PARITY OF CARRIES
SHIFT
GROUP PROP
GROUP GEN
STATUS OUT OVERFLOW
CARRY
ZERO DET
VCCO GND
VTT -2.0 V
VCC GND
VEE -5.2 V
C19
C20
C21
C22
R3 0.75 Ω
-2.2 V
TP4
10105 0417
-R2 PIA24 BJ (A24)
-IPG PIA25 BK
-IGG PIB25 BK
-ZD2 PIA27 AH
A 2,5
B 2,4
LSI 4-BIT ALU SLICE 10800 2943
-OGG PIA36 BK
-OPG PIB33 BK
C 2,5
D 2,4
C23
C24
C25
C26
R4 0.75 Ω
261 Ω
162 Ω
-5.2 V
(-ASI6)
(-ASI5)
PIB34 -ASI4
PIA34 -ASI3
PIA32 -ASI2
PIA31 -ASI0
PIA37 -ASI09
P2B04 -ASI08
PIA33 -ASI07
PIA29 -ASI06
PIB30 -ASI05
PIB32 -ASI04
PIA35 -ASI03
PIA42 -ASI02
PIA30 -ASI01
PIB35 -ASI00
PIB31 -R4
PIA43 -10800 CIN
PIA19 +10800 CLK
AH
BK
NOTES:
1 THESE INPUTS ARE NOT TERMINATED.
2 TERMINATION OF BIDIRECTIONAL BUSSES (MARKED ><).
3 WITH DROP POLY COATING USE 10470 RAMS.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR BITS 0-7
TYPE : BJ LOC : A26
CODE IDENT 34010
DWG NO 60455690
REV T
SIZE C
SHEET 1 OF 5
PAGE 5-216
ASSY NO. 53371069
ASSY NO. 52681294


LSI MEMORY INTERFACE FUNCTION 10803 0443
POINTER
BUS INVERT
REG FILE ADR
ALU FNCT
SELECT INPUTS
MAR & RF
ADRS OUT ENBL
DATA XFER
CLK
CARRY IN
DATA
O BUS
I BUS
ADRS
CARRY OUT
STATUS OUT
GROUP GEN/OVERFLOW
GROUP PROP/Ø DET
BK P1B16 -P INPUT 7
BK P1A17 -P INPUT 6
BK P1A16 -P INPUT 5
BK P1B11 -P INPUT 4
AH P1A20 +TOO OR PROG CLK
+D BUS 7 P1B05
+D BUS 6 P1A04
+D BUS 5 P1A03
+D BUS 4 P1B04
AE, AF
B 1,4
A 1,5
D 1,4
C 1,5
+RAM OR BUFF ADDR 2^7 P2A27 BK
+RAM OR BUFF ADDR 2^7 P2A26 BJ (A24)
+RAM OR BUFF ADDR 2^7 P2A25 BJ (A26)
+RAM OR BUFF ADDR 2^6 P2A29
+RAM OR BUFF ADDR 2^6 P2A28
+RAM OR BUFF ADDR 2^6 P2B30
+RAM OR BUFF ADDR 2^5 P2B25 BK
+RAM OR BUFF ADDR 2^5 P2B26 BJ (A24)
+RAM OR BUFF ADDR 2^5 P2B27 BJ (A26)
+RAM OR BUFF ADDR 2^4 P2A30 BK
+RAM OR BUFF ADDR 2^4 P2B29 BJ (A24)
+RAM OR BUFF ADDR 2^4 P2B28 BJ (A26)
-CARRY-1 P1B03 BJ (A24)
-ZD3 P1B27 AH
+RAM OR BUFF ADDR 2^3 P2A13 BK
+RAM OR BUFF ADDR 2^3 P2A14 BJ (A24)
+RAM OR BUFF ADDR 2^3 P2A15 BJ (A26)
+RAM OR BUFF ADDR 2^2 P2A16 BK
+RAM OR BUFF ADDR 2^2 P2A04 BJ (A24)
+RAM OR BUFF ADDR 2^2 P2A08 BJ (A26)
+RAM OR BUFF ADDR 2^1 P2B14 BK
+RAM OR BUFF ADDR 2^1 P2B13 BJ (A24)
+RAM OR BUFF ADDR 2^1 P2B12 BJ (A26)
+RAM OR BUFF ADDR 2^0 P2A12 BK
+RAM OR BUFF ADDR 2^0 P2A11 BJ (A24)
+RAM OR BUFF ADDR 2^0 P2A10 BJ (A26)
+D BUS 3 P1B13
+D BUS 2 P1A11
+D BUS 1 P1A09
+D BUS 0 P1A10
AE, AF
10110 4453
10110 4441
10105 0417
10110 3841
10110 3853
(1,15,16)
R1 0.75 Ω
R2 0.75 Ω
-2.2 V
C11
C12
C13
C14
C15
C16
C17
C18
7,17
25,45
12,36
1,24
25,48
NOTES:
1 SEE SHEET 1.
2 SEE SHEET 1.
3 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 0-7
TYPE : BJ LOC : A26
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET 2 OF 5
PAGE 5-217
3 ASSY NO. 53371069
ASSY NO. 52681294

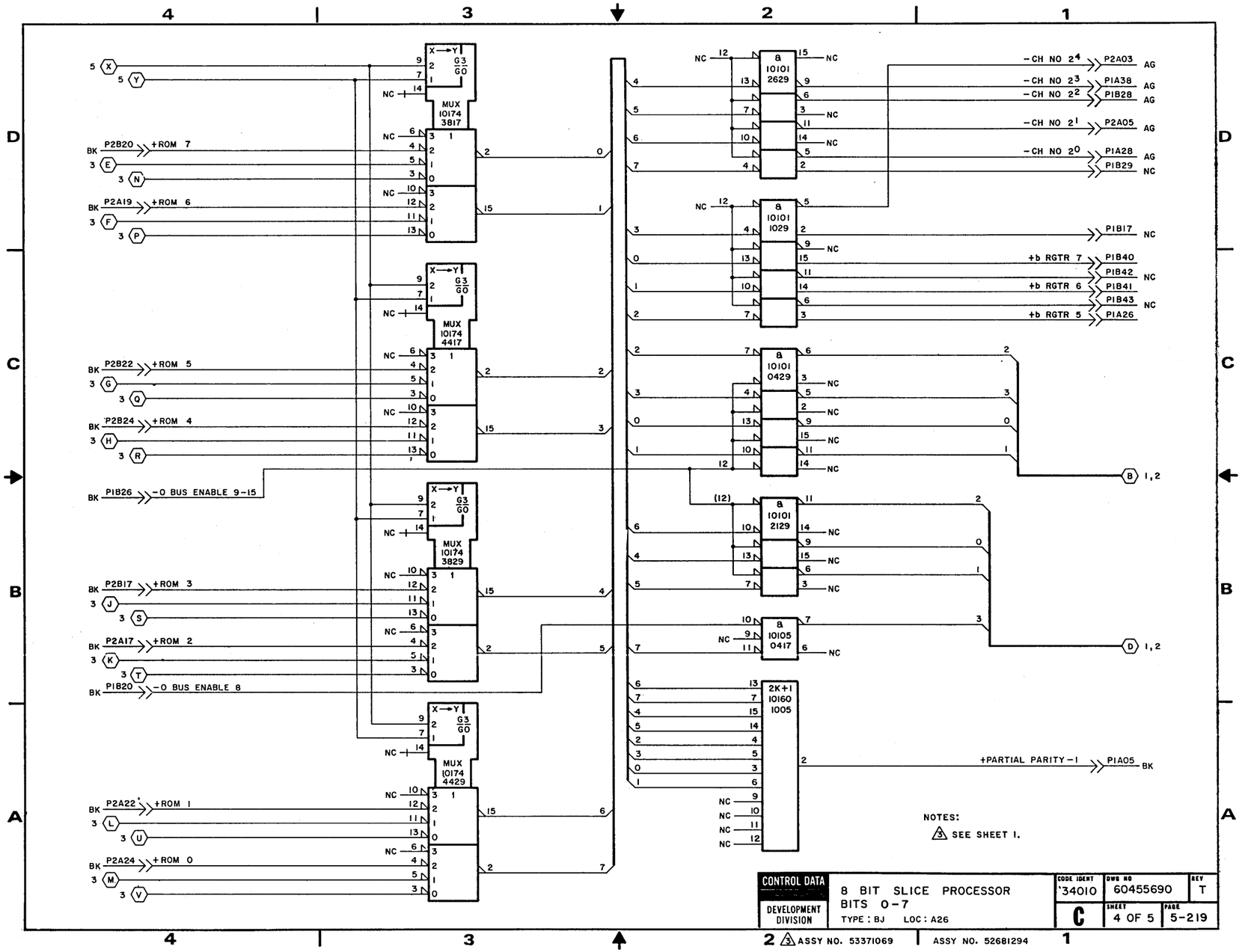


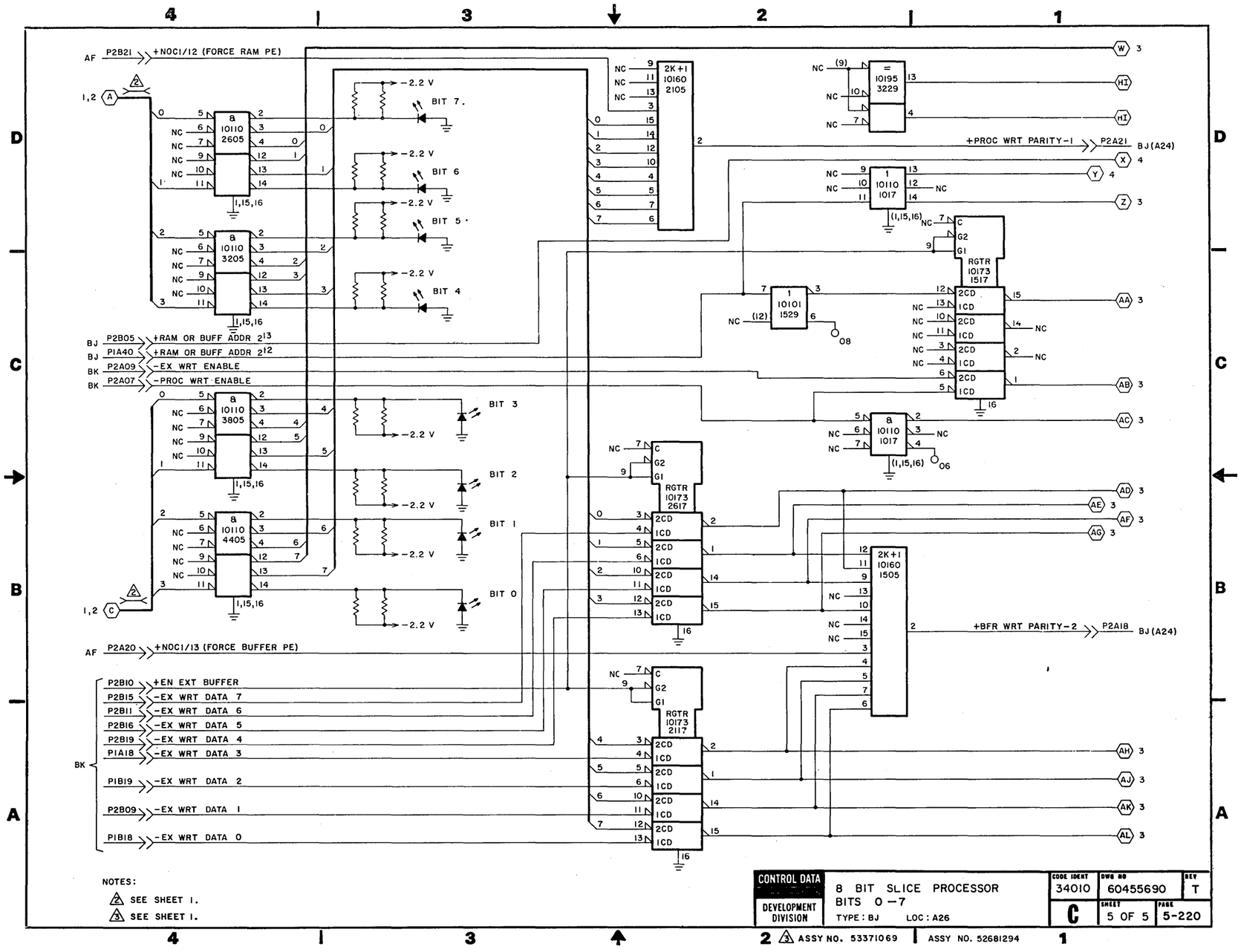
NOTES:

3 SEE SHEET 1.

CONTROL DATA	8 BIT SLICE PROCESSOR	CODE IDENT 34010	DWG NO 60455690	REV T
DEVELOPMENT DIVISION	BITS 0-7	C	SHEET 3 OF 5	PAGE 5-218
	TYPE: BJ LOC: A26			

2 3 ASSY NO. 53371069 | ASSY. NO. 52681294


4
3
2
1
D
C
B
A
MUX 10174 3817
MUX 10174 4417
MUX 10174 3829
MUX 10174 4429
X→Y
G3
GO
P2B20 +ROM 7
P2B22 +ROM 5
P2B24 +ROM 4
P2B17 +ROM 3
P2A17 +ROM 2
P2A19 +ROM 6
P2A22 +ROM 1
P2A24 +ROM 0
P1B26 -O BUS ENABLE 9-15
P1B20 -O BUS ENABLE 8
8 10101 2629
8 10101 0429
8 10101 2129
8 10105 0417
2K+1 10160 1005
-CH NO 2^4
-CH NO 2^3
-CH NO 2^2
-CH NO 2^1
-CH NO 2^0
P2A03
P1A38
P1B28
P2A05
P1A28
P1B29
P1B17
+b RGTR 7
+b RGTR 6
+b RGTR 5
P1B40
P1B42
P1B41
P1B43
P1A26
+PARTIAL PARITY-1
P1A05
B 1,2
D 1,2
NOTES:
3 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
8 BIT SLICE PROCESSOR
BITS 0-7
TYPE : BJ LOC : A26
CODE IDENT '34010
DWG NO 60455690
REV T
SHEET 4 OF 5
PAGE 5-219
C
2 3 ASSY NO. 53371069
ASSY NO. 52681294



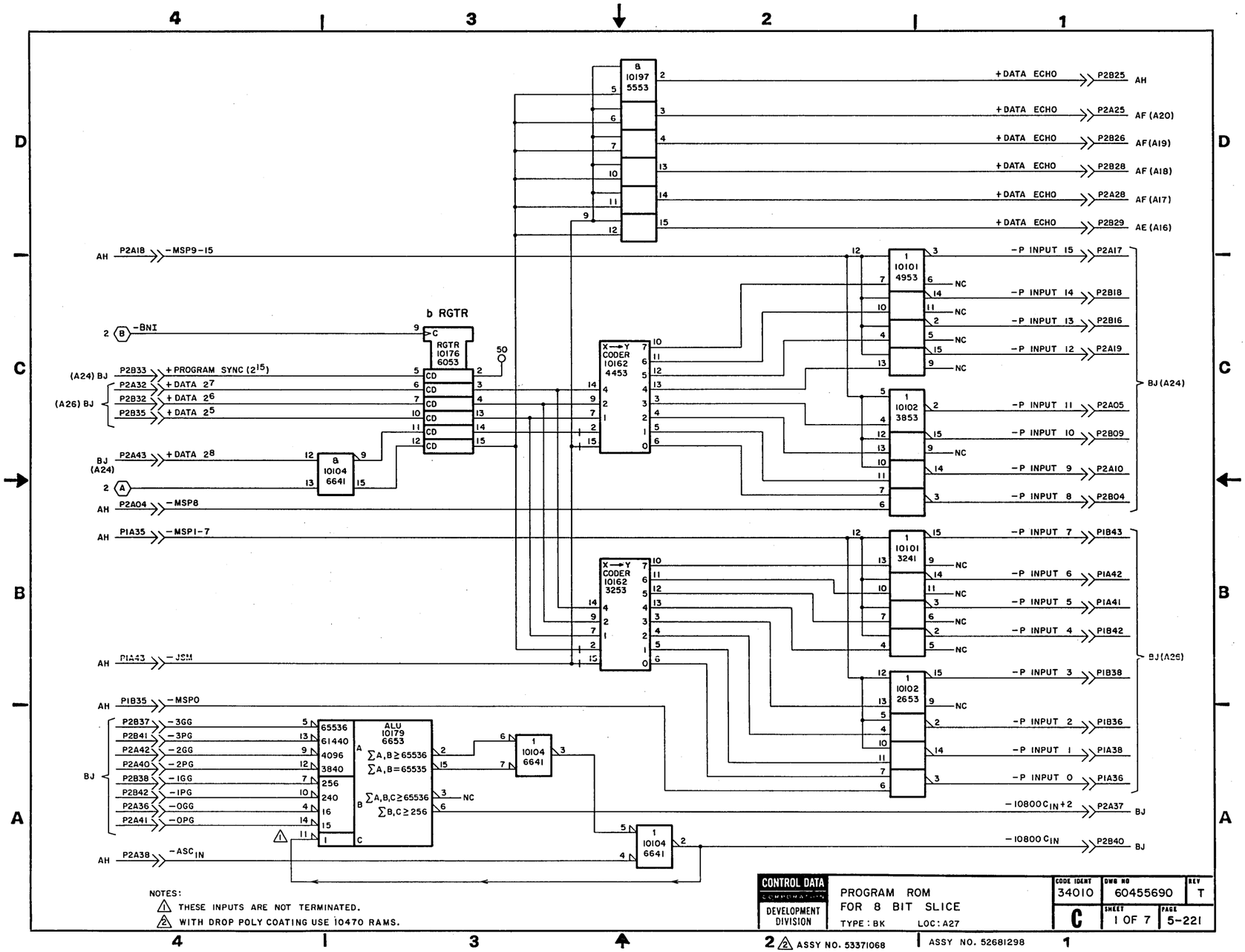
NOTES:

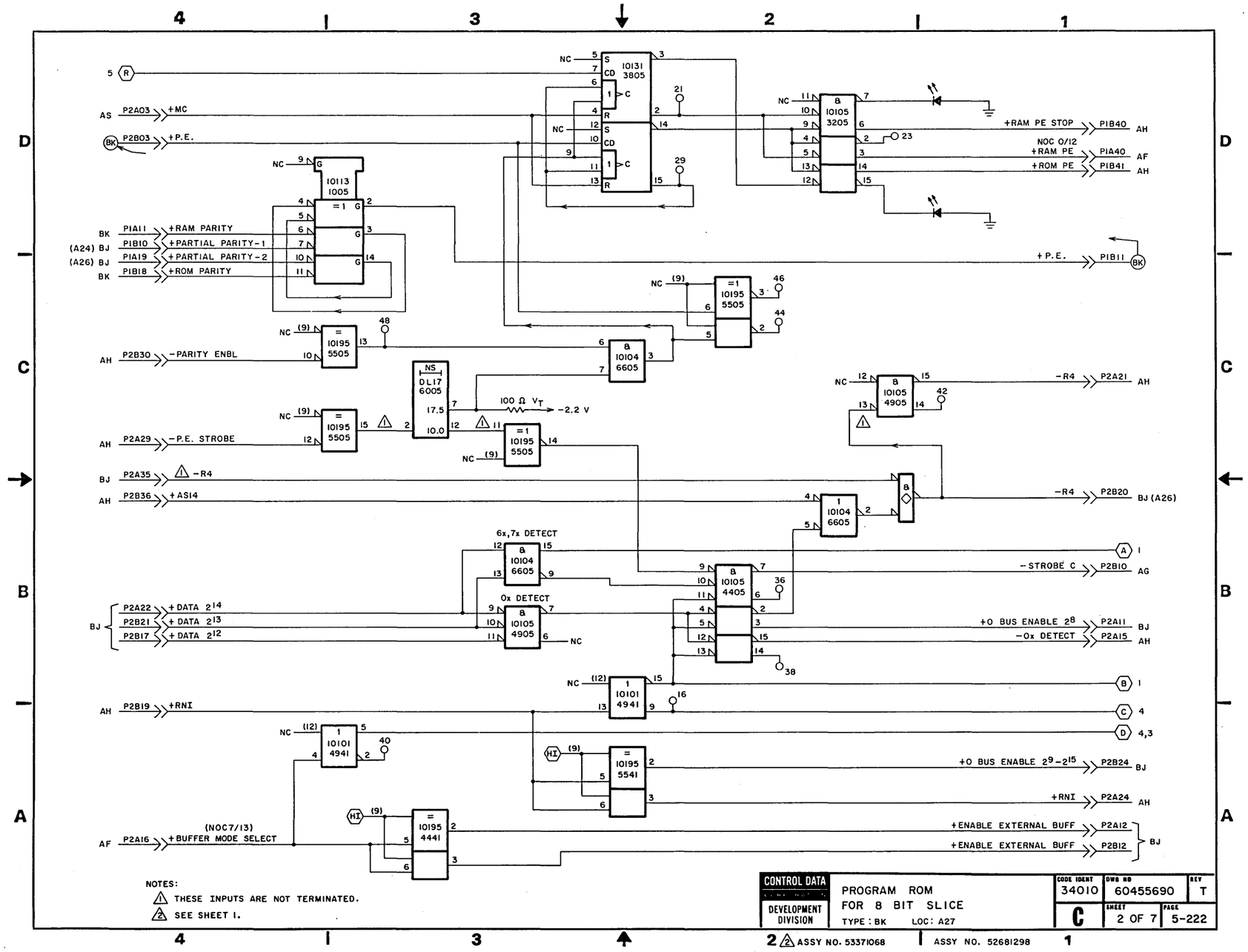
2 SEE SHEET 1.

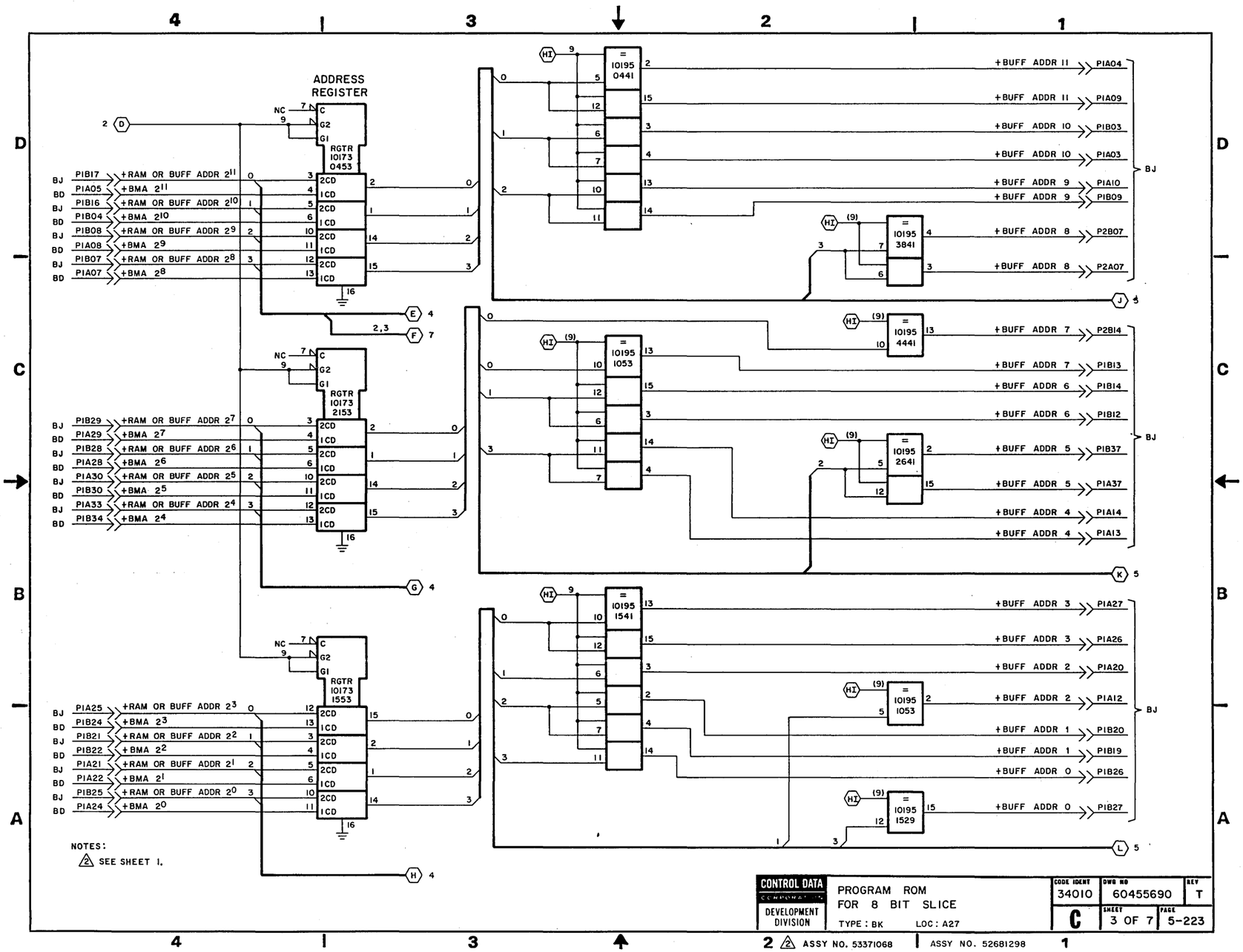
3 SEE SHEET 1.

CONTROL DATA	8 BIT SLICE PROCESSOR BITS 0-7	CODE IDENT 34010	DWG NO 60455690	REV T
DEVELOPMENT DIVISION	TYPE: BJ LOC: A26	C	SHEET 5 OF 5	PAGE 5-220

3 ASSY NO. 53371069 | ASSY NO. 52681294

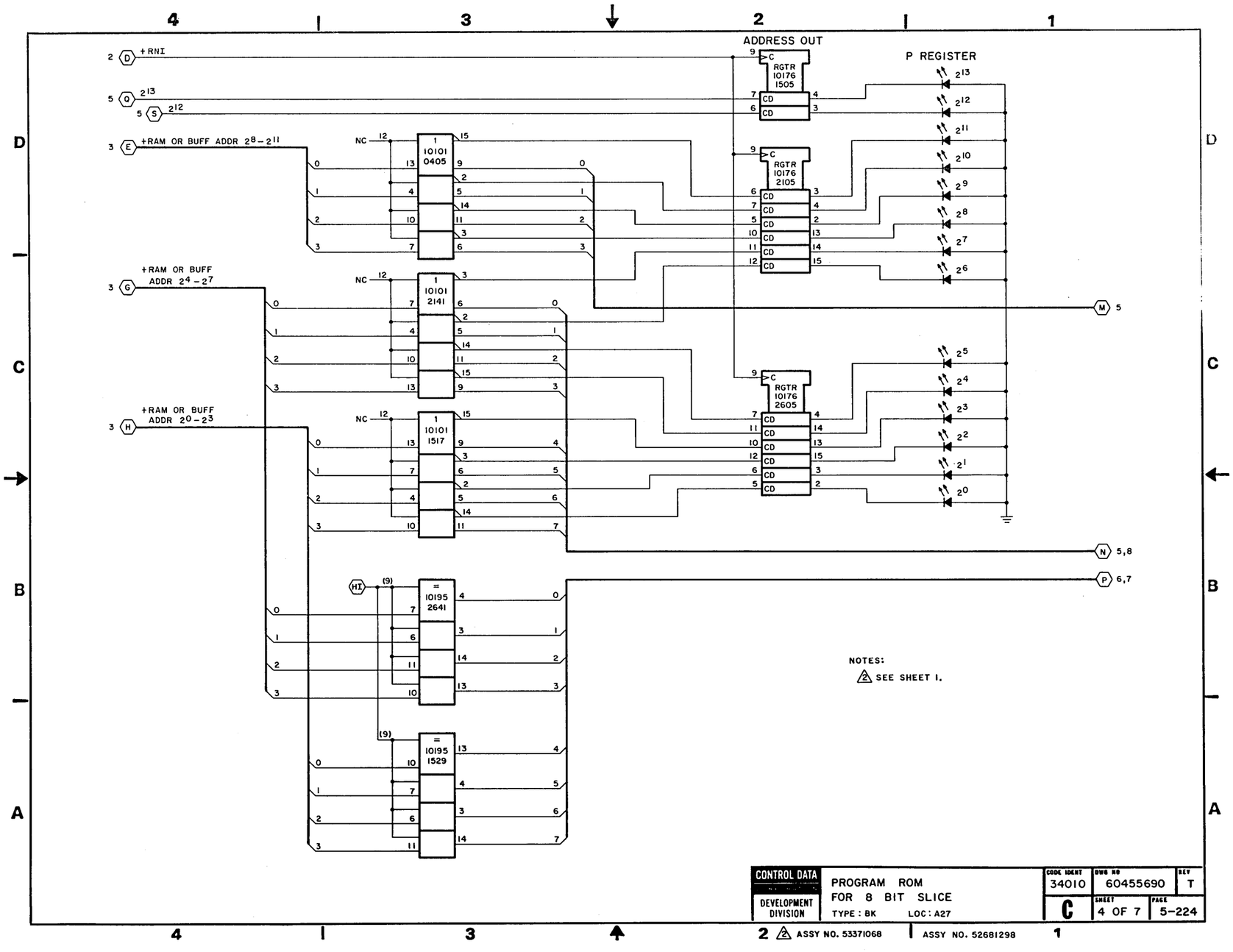

4
3
2
1
D
C
B
A
8 10197 5553
+DATA ECHO P2B25 AH
+DATA ECHO P2A25 AF (A20)
+DATA ECHO P2B26 AF(A19)
+DATA ECHO P2B28 AF (A18)
+DATA ECHO P2A28 AF (A17)
+DATA ECHO P2B29 AE (A16)
AH P2A18 -MSP9-15
b RGTR
RGTR 10176 6053
2 B -BNI
(A24) BJ P2B33 +PROGRAM SYNC (2^15)
P2A32 +DATA 2^7
(A26) BJ P2B32 +DATA 2^6
P2B35 +DATA 2^5
BJ (A24) P2A43 +DATA 2^8
2 A
AH P2A04 -MSP8
AH P1A35 -MSP1-7
AH P1A43 -JSM
AH P1B35 -MSP0
BJ P2B37 -3GG
P2B41 -3PG
P2A42 -2GG
P2A40 -2PG
P2B38 -1GG
P2B42 -1PG
P2A36 -0GG
P2A41 -0PG
AH P2A38 -ASC IN
8 10104 6641
X→Y CODER 10162 4453
X→Y CODER 10162 3253
65536
61440
4096
3840
256
240
16
15
ALU 10179 6653
ΣA,B≥65536
ΣA,B=65535
ΣA,B,C≥65536
ΣB,C≥256
1 10104 6641
1 10101 4953
1 10102 3853
1 10101 3241
1 10102 2653
-P INPUT 15 P2A17
-P INPUT 14 P2B18
-P INPUT 13 P2B16
-P INPUT 12 P2A19
BJ (A24)
-P INPUT 11 P2A05
-P INPUT 10 P2B09
-P INPUT 9 P2A10
-P INPUT 8 P2B04
-P INPUT 7 P1B43
-P INPUT 6 P1A42
-P INPUT 5 P1A41
-P INPUT 4 P1B42
BJ (A26)
-P INPUT 3 P1B38
-P INPUT 2 P1B36
-P INPUT 1 P1A38
-P INPUT 0 P1A36
-10800 C_IN+2 P2A37 BJ
-10800 C_IN P2B40 BJ
NC
50
NOTES:
1 THESE INPUTS ARE NOT TERMINATED.
2 WITH DROP POLY COATING USE 10470 RAMS.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
PROGRAM ROM
FOR 8 BIT SLICE
TYPE: BK LOC: A27
CODE IDENT 34010
DWG NO 60455690
REV T
SIZE C
SHEET 1 OF 7
PAGE 5-221
2 ASSY NO. 53371068
ASSY NO. 52681298 1

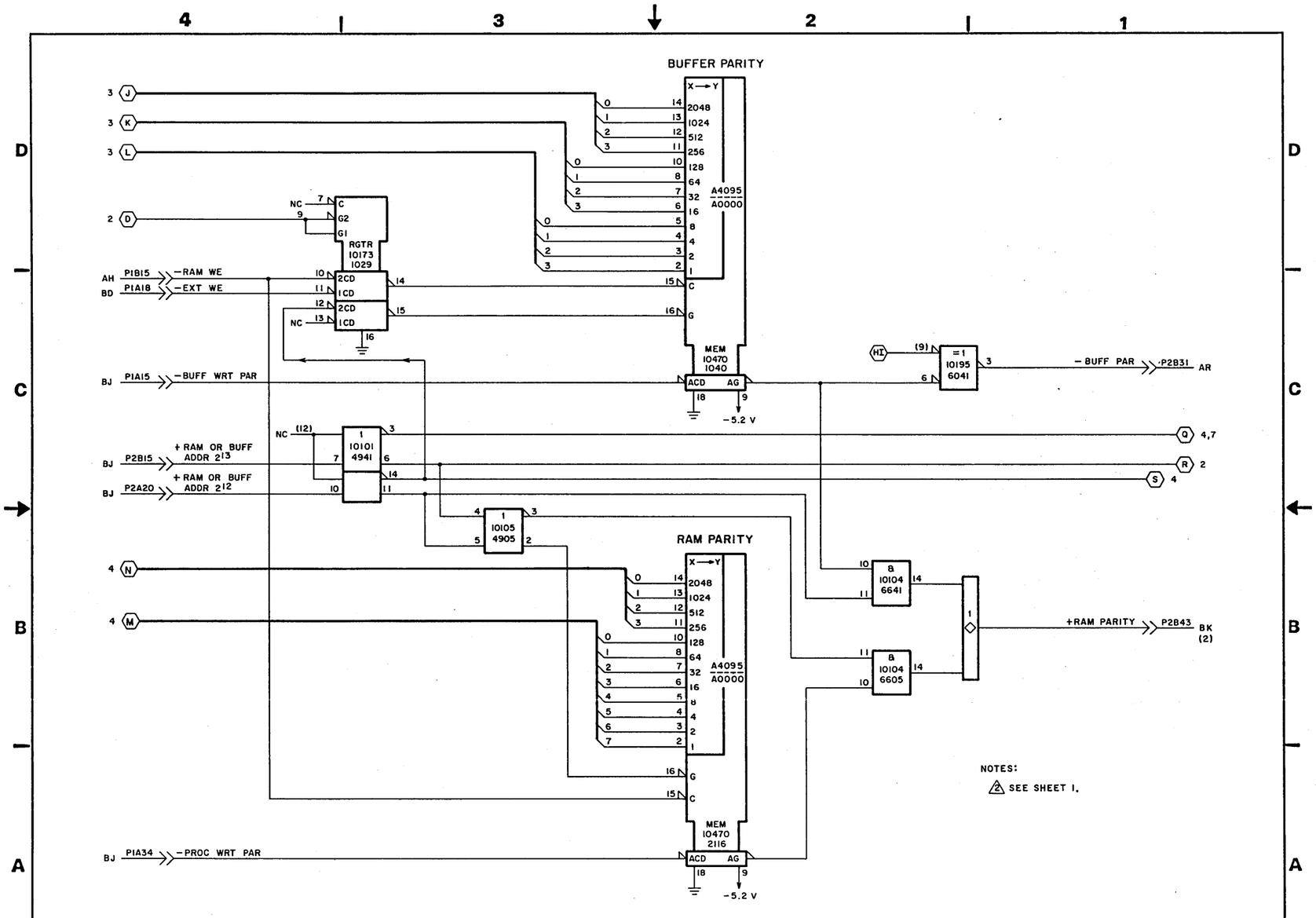

NOTES:
1 THESE INPUTS ARE NOT TERMINATED.
2 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
PROGRAM ROM
FOR 8 BIT SLICE
TYPE : BK LOC : A27
CODE IDENT 34010
DWG NO 60455690
REV T
C
SHEET 2 OF 7
PAGE 5-222
2 ASSY NO. 53371068
ASSY NO. 52681298
+RAM PE STOP
NOC 0/12 +RAM PE
+ROM PE
+P.E.
+RAM PARITY
+PARTIAL PARITY-1
+PARTIAL PARITY-2
+ROM PARITY
-PARITY ENBL
-P.E. STROBE
-R4
+ASI4
6x,7x DETECT
0x DETECT
+DATA 2^14
+DATA 2^13
+DATA 2^12
+RNI
+BUFFER MODE SELECT
(NOC7/13)
-STROBE C
+O BUS ENABLE 2^8
-0x DETECT
+O BUS ENABLE 2^9-2^15
+ENABLE EXTERNAL BUFF
+ENABLE EXTERNAL BUFF
-2.2 V
100 Ω



CONTROL DATA DEVELOPMENT DIVISION	PROGRAM ROM FOR 8 BIT SLICE TYPE : BK LOC : A27	CODE IDENT 34010	DWG NO 60455690	REV T
		C	SHEET 3 OF 7	PAGE 5-223

2 ASSY NO. 53371068 | ASSY NO. 52681298

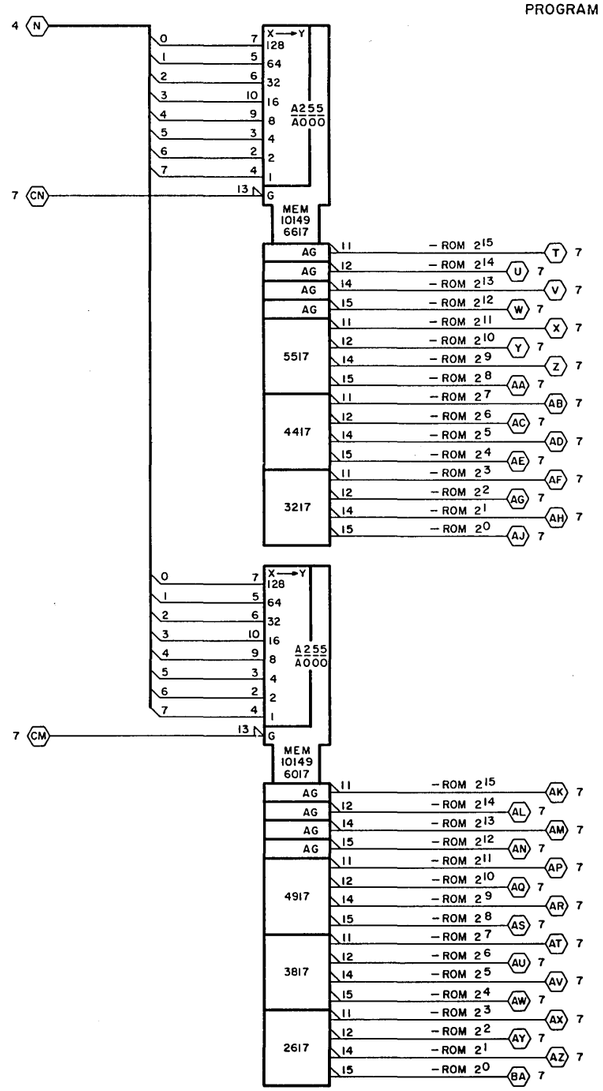

ADDRESS OUT
P REGISTER
+RNI
2^13
2^12
+RAM OR BUFF ADDR 2^8-2^11
+RAM OR BUFF ADDR 2^4-2^7
+RAM OR BUFF ADDR 2^0-2^3
RGTR 10176 1505
RGTR 10176 2105
RGTR 10176 2605
10101 0405
10101 2141
10101 1517
10195 2641
10195 1529
2^13
2^12
2^11
2^10
2^9
2^8
2^7
2^6
2^5
2^4
2^3
2^2
2^1
2^0
M 5
N 5,8
P 6,7
NOTES:
2 SEE SHEET 1.
CONTROL DATA
DEVELOPMENT DIVISION
PROGRAM ROM
FOR 8 BIT SLICE
TYPE : BK LOC : A27
CODE IDENT 34010
DWG NO 60455690
REV T
SHEET 4 OF 7
PAGE 5-224
2 ASSY NO. 53371068
ASSY NO. 52681298

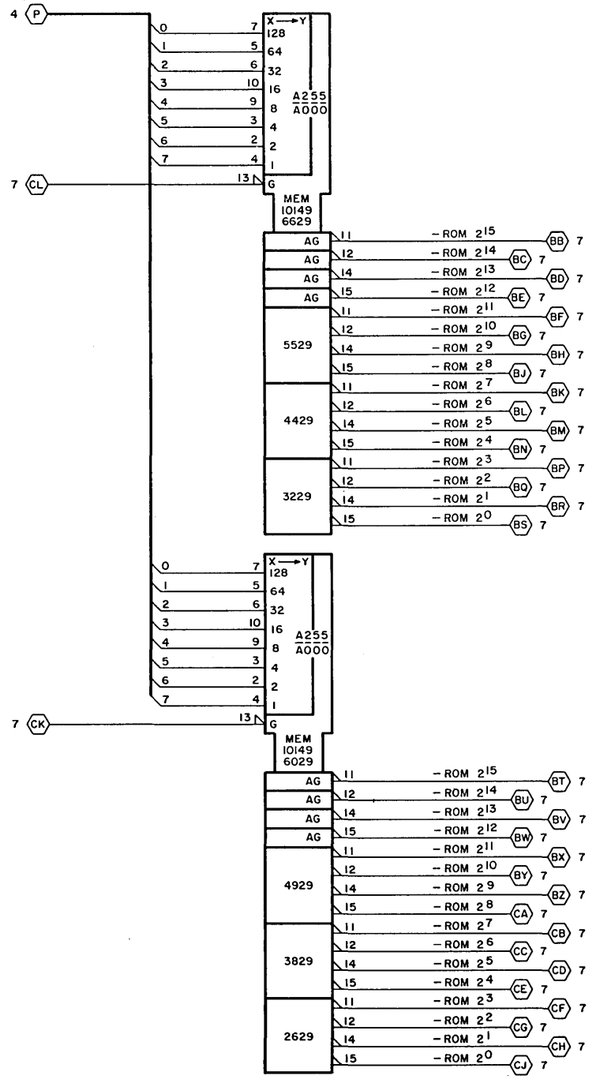


CONTROL DATA	PROGRAM ROM FOR 8 BIT SLICE	CODE IDENT 34010	DWG NO 60455690	REV T
DEVELOPMENT DIVISION	TYPE: BK LOC: A27	C	SHEET 5 OF 7	PAGE 5-225

2 ASSY NO. 53371068 | ASSY NO. 52681298 1

PROGRAM ROM



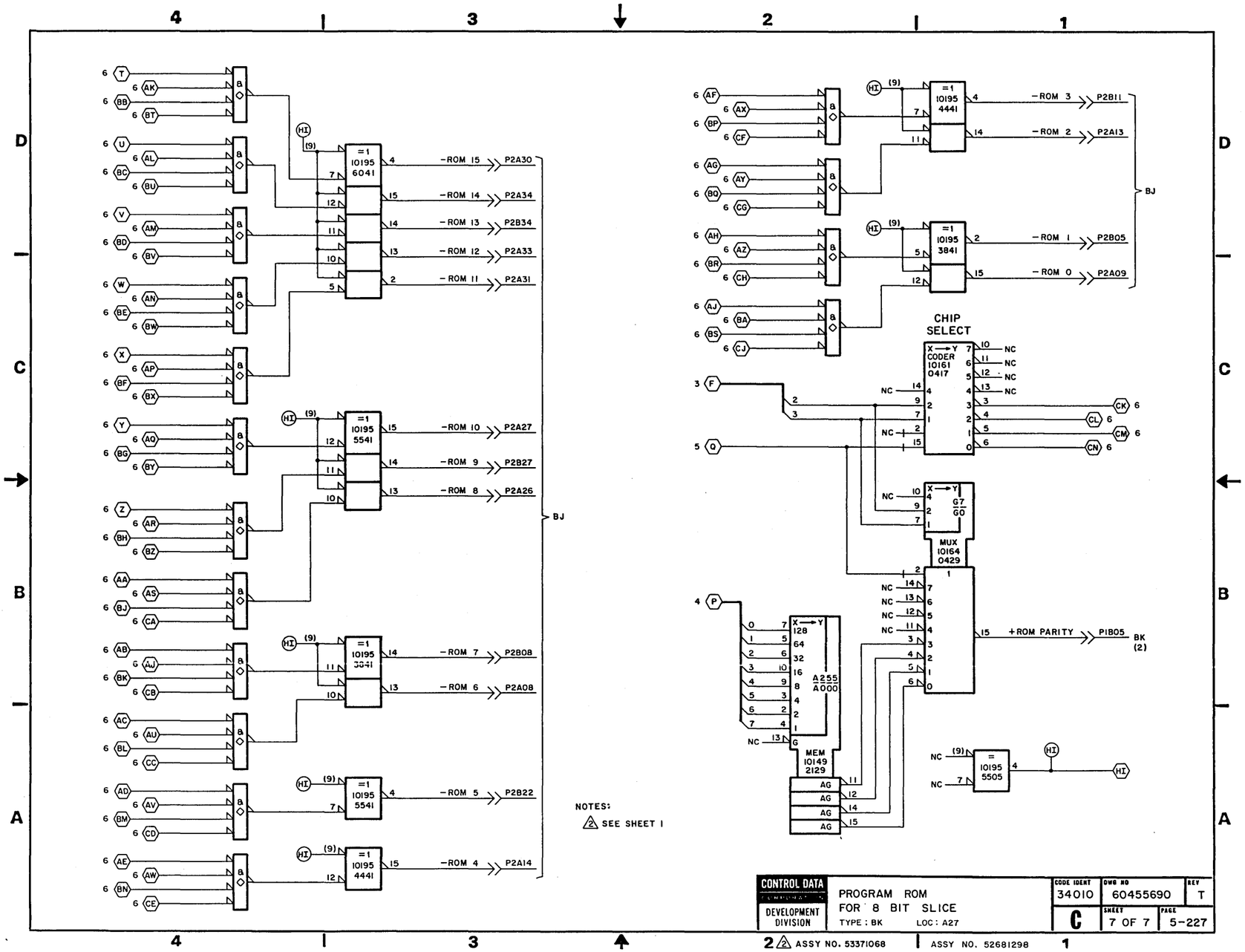


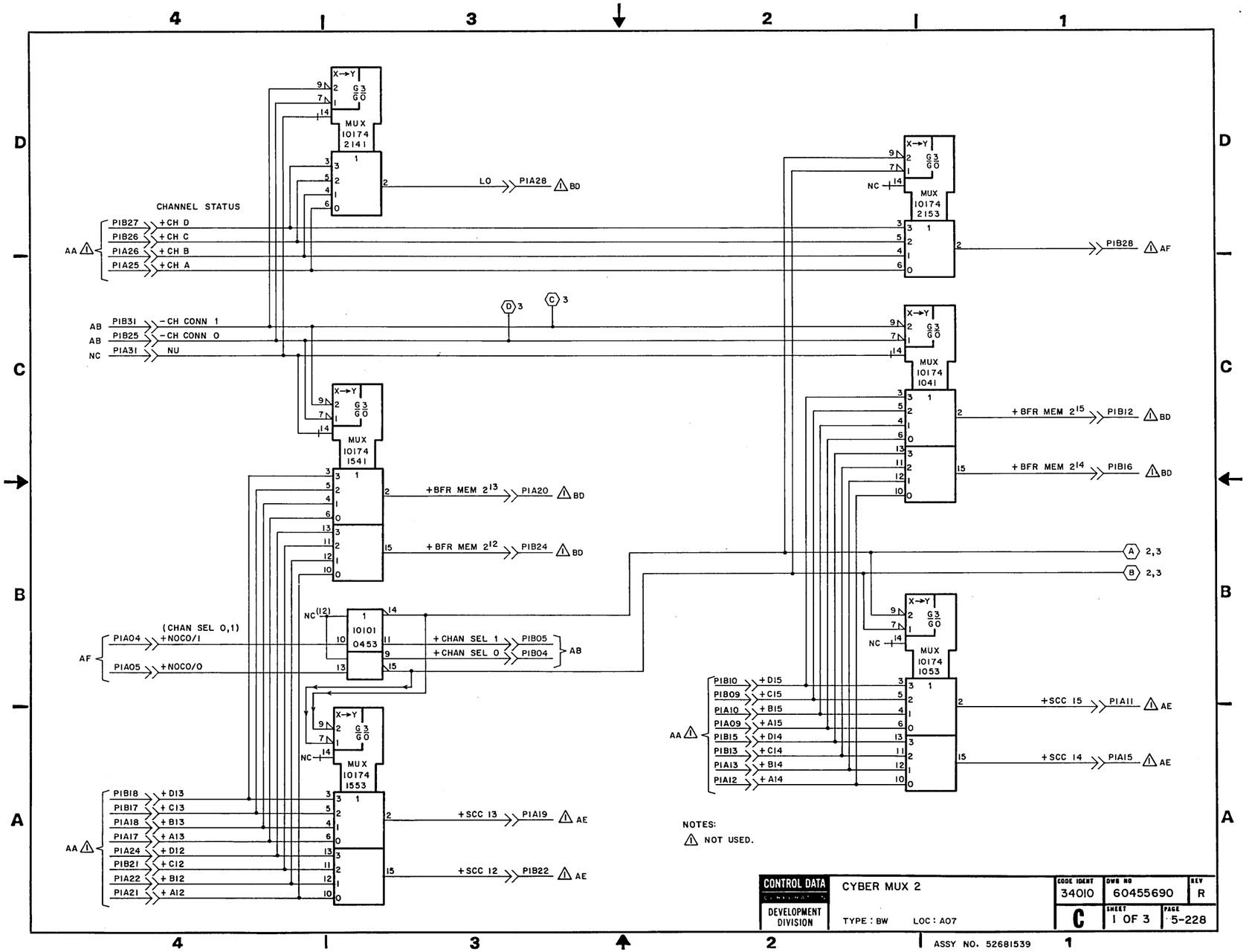
NOTES:

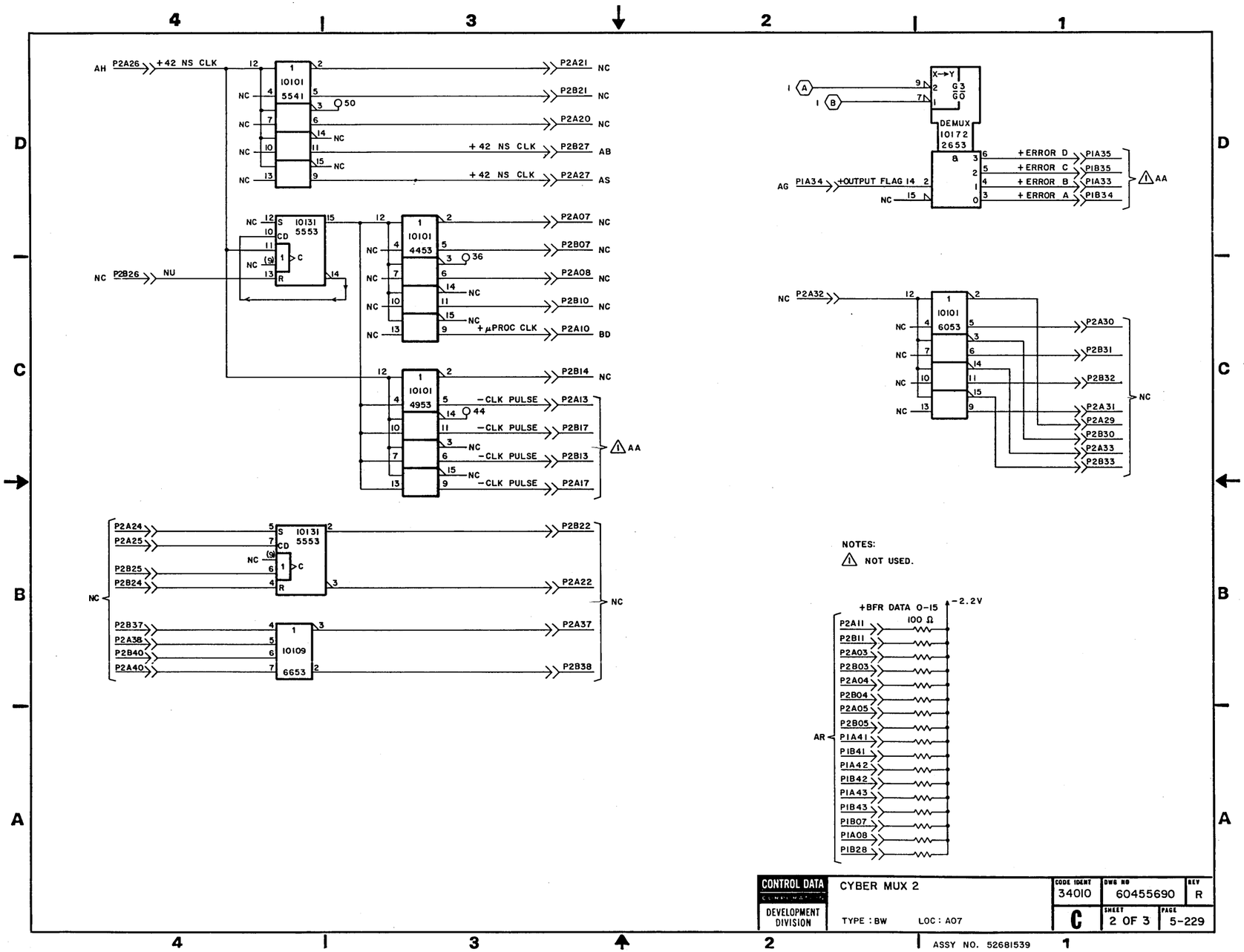
2 SEE SHEET 1

CONTROL DATA	PROGRAM ROM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION	FOR 8 BIT SLICE	34010	60455690	T
	TYPE : BK LOC : A27	C	SHEET 6 OF 7	PAGE 5-226

2 ASSY NO. 53371068 | ASSY NO. 52681298

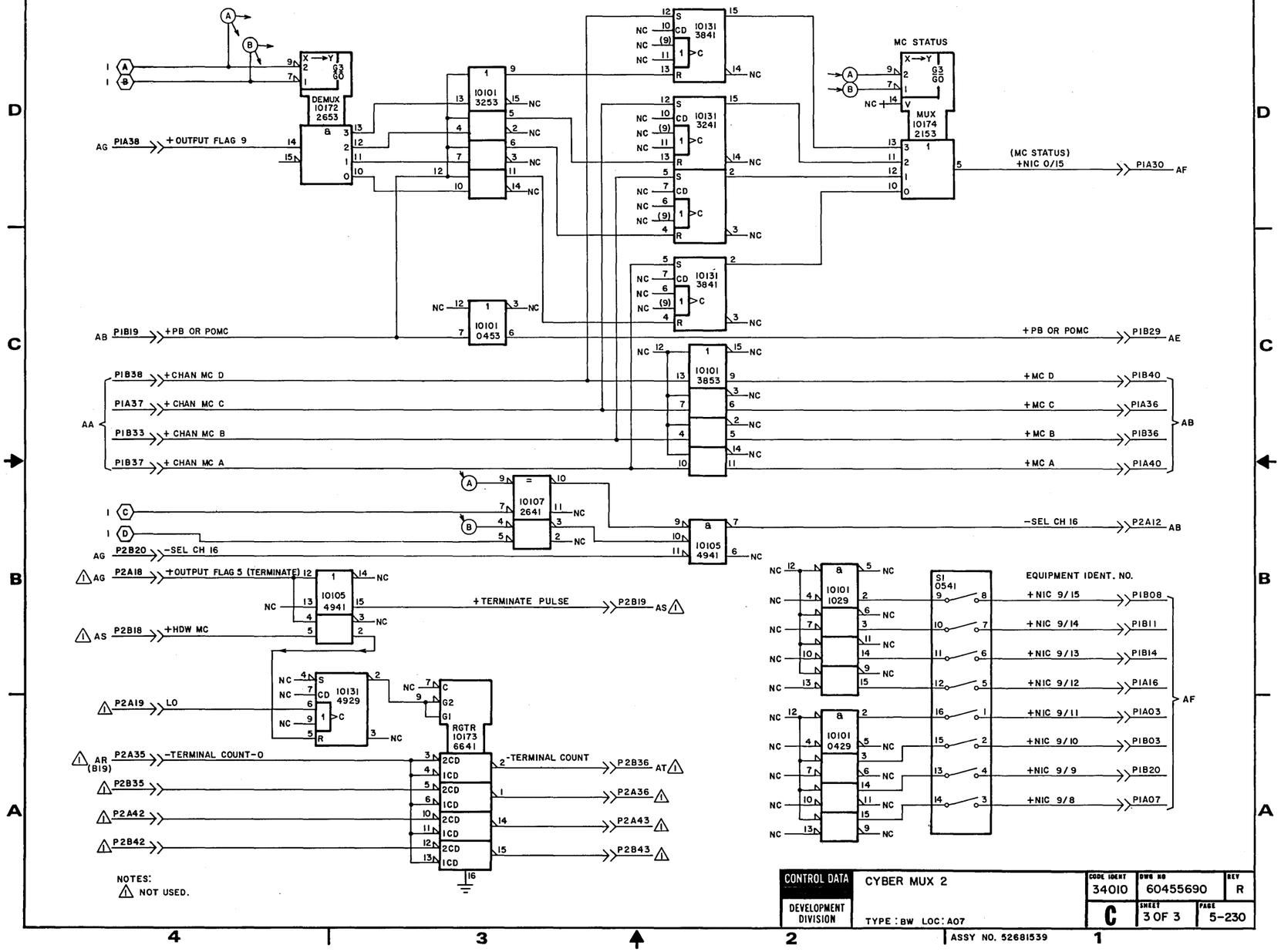

4
3
2
1
D
C
B
A
6 T
6 AK
6 BB
6 BT
6 U
6 AL
6 BC
6 BU
6 V
6 AM
6 BD
6 BV
6 W
6 AN
6 BE
6 BW
6 X
6 AP
6 BF
6 BX
6 Y
6 AQ
6 BG
6 BY
6 Z
6 AR
6 BH
6 BZ
6 AA
6 AS
6 BJ
6 CA
6 AB
6 AJ
6 BK
6 CB
6 AC
6 AU
6 BL
6 CC
6 AD
6 AV
6 BM
6 CD
6 AE
6 AW
6 BN
6 CE
HI
(9)
=1
10195
6041
-ROM 15
P2A30
-ROM 14
P2A34
-ROM 13
P2B34
-ROM 12
P2A33
-ROM 11
P2A31
=1
10195
5541
-ROM 10
P2A27
-ROM 9
P2B27
-ROM 8
P2A26
=1
10195
3841
-ROM 7
P2B08
-ROM 6
P2A08
=1
10195
5541
-ROM 5
P2B22
=1
10195
4441
-ROM 4
P2A14
BJ
6 AF
6 AX
6 BP
6 CF
6 AG
6 AY
6 BQ
6 CG
6 AH
6 AZ
6 BR
6 CH
6 AJ
6 BA
6 BS
6 CJ
=1
10195
4441
-ROM 3
P2B11
-ROM 2
P2A13
=1
10195
3841
-ROM 1
P2B05
-ROM 0
P2A09
BJ
CHIP
SELECT
3 F
5 Q
X → Y
CODER
10161
0417
NC
CK 6
CL 6
CM 6
CN 6
X → Y
G7
G0
MUX
10164
0429
4 P
X → Y
128
64
32
16
8
4
2
1
A255
A000
MEM
10149
2129
AG
+ROM PARITY
P1B05
BK
(2)
=
10195
5505
NOTES:
2 SEE SHEET 1
CONTROL DATA
DEVELOPMENT
DIVISION
PROGRAM ROM
FOR 8 BIT SLICE
TYPE : BK
LOC : A27
CODE IDENT
34010
DWG NO
60455690
REV
T
C
SHEET
7 OF 7
PAGE
5-227
2 ASSY NO. 53371068
ASSY NO. 52681298

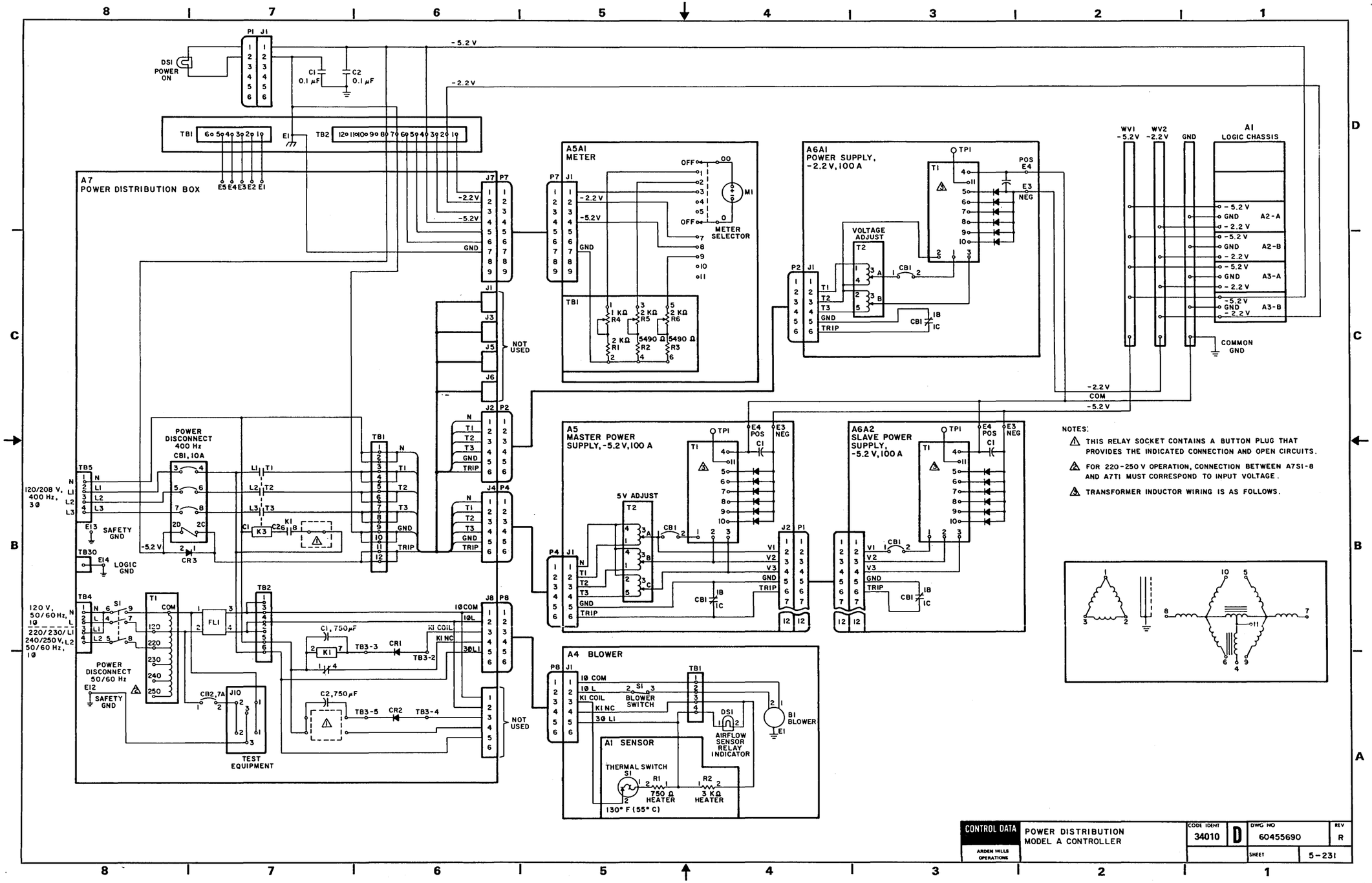

MUX 10174 2141
MUX 10174 2153
MUX 10174 1041
MUX 10174 1541
MUX 10174 1553
MUX 10174 1053
10101 0453
CHANNEL STATUS
(CHAN SEL 0,1)
LO
PIA28
BD
PIB28
AF
PIB31 -CH CONN 1
PIB25 -CH CONN 0
PIA31 NU
+BFR MEM 2^15
PIB12
+BFR MEM 2^14
PIB16
+BFR MEM 2^13
PIA20
+BFR MEM 2^12
PIB24
+CHAN SEL 1
PIB05
+CHAN SEL 0
PIB04
AB
+SCC 13
PIA19
AE
+SCC 12
PIB22
+SCC 15
PIA11
+SCC 14
PIA15
2,3
NOTES:
NOT USED.
CONTROL DATA
DEVELOPMENT DIVISION
CYBER MUX 2
TYPE : BW
LOC : A07
ASSY NO. 52681539
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 1 OF 3
PAGE 5-228



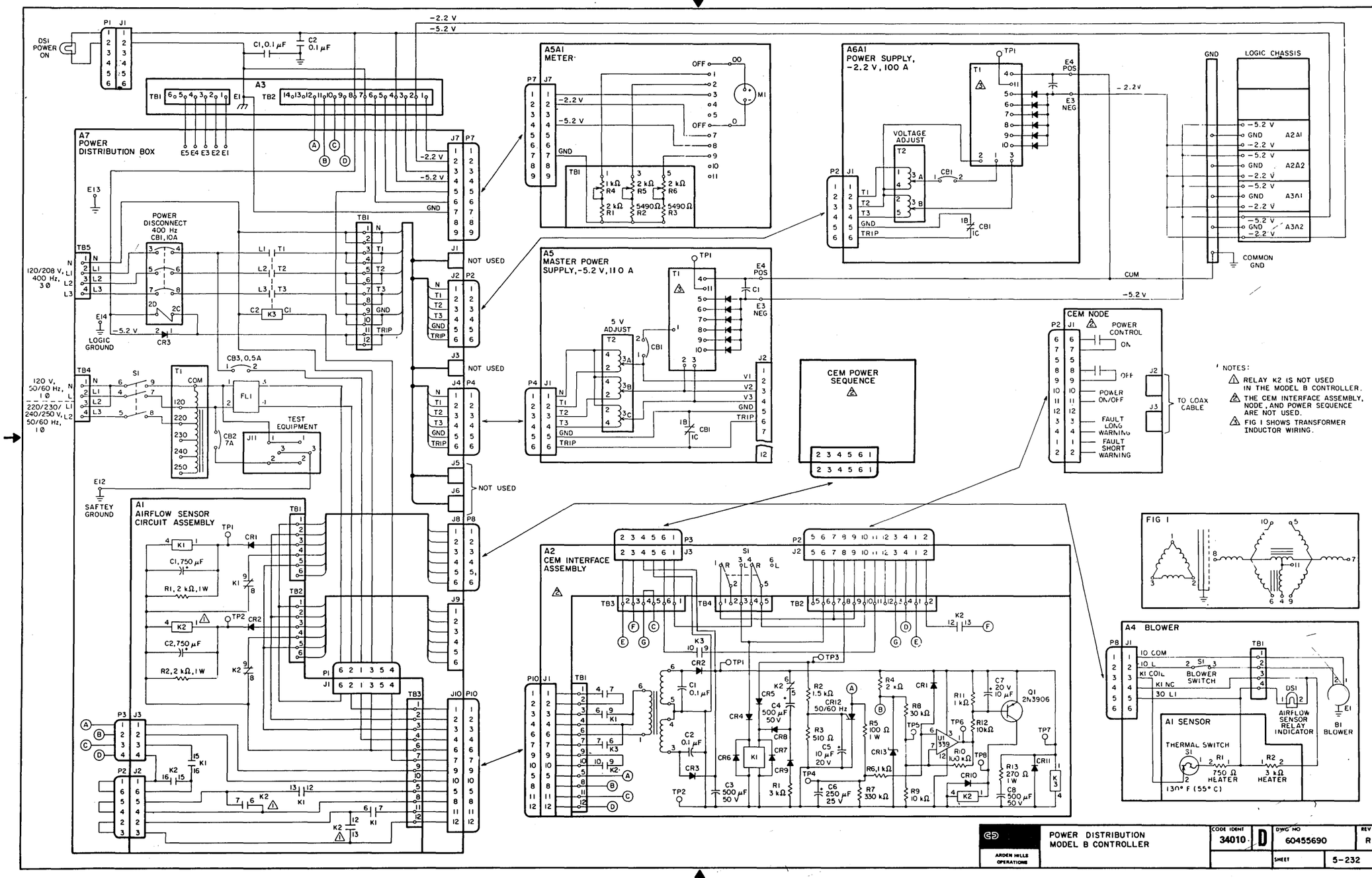
CONTROL DATA	CYBER MUX 2	CODE IDENT 34010	DWG NO 60455690	REV R
DEVELOPMENT DIVISION	TYPE : BW LOC : A07	C	SHEET 2 OF 3	PAGE 5-229

ASSY NO. 52681539


MC STATUS
DEMUX 10172 2653
MUX 10174 2153
10101 3253
10101 0453
10131 3841
10131 3241
10131 3841
10101 3853
10107 2641
10105 4941
10105 4941
10131 4929
RGTR 10173 6641
10101 1029
10101 0429
SI 0541
PIA38 +OUTPUT FLAG 9
(MC STATUS) +NIC 0/15 PIA30 AF
PIB19 +PB OR POMC
+PB OR POMC PIB29 AE
PIB38 +CHAN MC D
PIA37 +CHAN MC C
PIB33 +CHAN MC B
PIB37 +CHAN MC A
+MC D PIB40
+MC C PIA36
+MC B PIB36
+MC A PIA40
AB
AA
P2B20 -SEL CH 16
-SEL CH 16 P2A12 AB
P2A18 +OUTPUT FLAG 5 (TERMINATE)
+TERMINATE PULSE P2B19 AS
P2B18 +HDW MC
P2A19 LO
P2A35 -TERMINAL COUNT-0
-TERMINAL COUNT P2B36 AT
P2B35
P2A42
P2B42
P2A36
P2A43
P2B43
EQUIPMENT IDENT. NO.
+NIC 9/15 PIB08
+NIC 9/14 PIB11
+NIC 9/13 PIB14
+NIC 9/12 PIA16
+NIC 9/11 PIA03
+NIC 9/10 PIB03
+NIC 9/9 PIB20
+NIC 9/8 PIA07
AF
NOTES:
⚠ NOT USED.
CONTROL DATA
DEVELOPMENT DIVISION
CYBER MUX 2
TYPE : BW LOC: A07
ASSY NO. 52681539
CODE IDENT 34010
DWG NO 60455690
REV R
SHEET 3 OF 3
PAGE 5-230
C



CONTROL DATA	POWER DISTRIBUTION MODEL A CONTROLLER	CODE IDENT		DWG NO	REV
ARDEN HILLS OPERATIONS		34010	D	60455690	R
				SHEET	5-231



GD ARDEN HILLS OPERATIONS	POWER DISTRIBUTION MODEL B CONTROLLER	CODE IDENT 34010	D	DWG NO 60455690 REV R
				SHEET 5-232

COMMENT SHEET

MANUAL TITLE: CDC FA211-A/B Fixed Module Drive Controller
Hardware Maintenance Manual, Volume 1 of 2

PUBLICATION NO.: 60455690 **REVISION:** W

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